CSE 341 Assignment-03

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(1) Given that,

Frequency, $f = 8M\ hz$

(a) We know that,

Time period, $T = \frac{1}{f}$

$\Rightarrow T = \frac{1}{8 \times 1000000}$

$\Rightarrow T = 0.000000125\ sec$

$\Rightarrow T = 125\ ns.$

$\therefore$ Time period 125 ns (Ans)

(b) In 8086 microprocessor, it work range is between 5 to 10 Mhz. Also, the duty cycle between the range is 33%.

Given that,

frequency = 8 Mhz.

$\therefore$ Duty cycle time, $d = 33\% \times T$

$= 33\% \times 125$ [from 1(a)]

$= \frac{33}{100} \times 125$

$= 41.25\ ns$

$\therefore$ Duty cycle time 41.25 ns (Ans)

(c) Bus cycle time = $4 \times T$

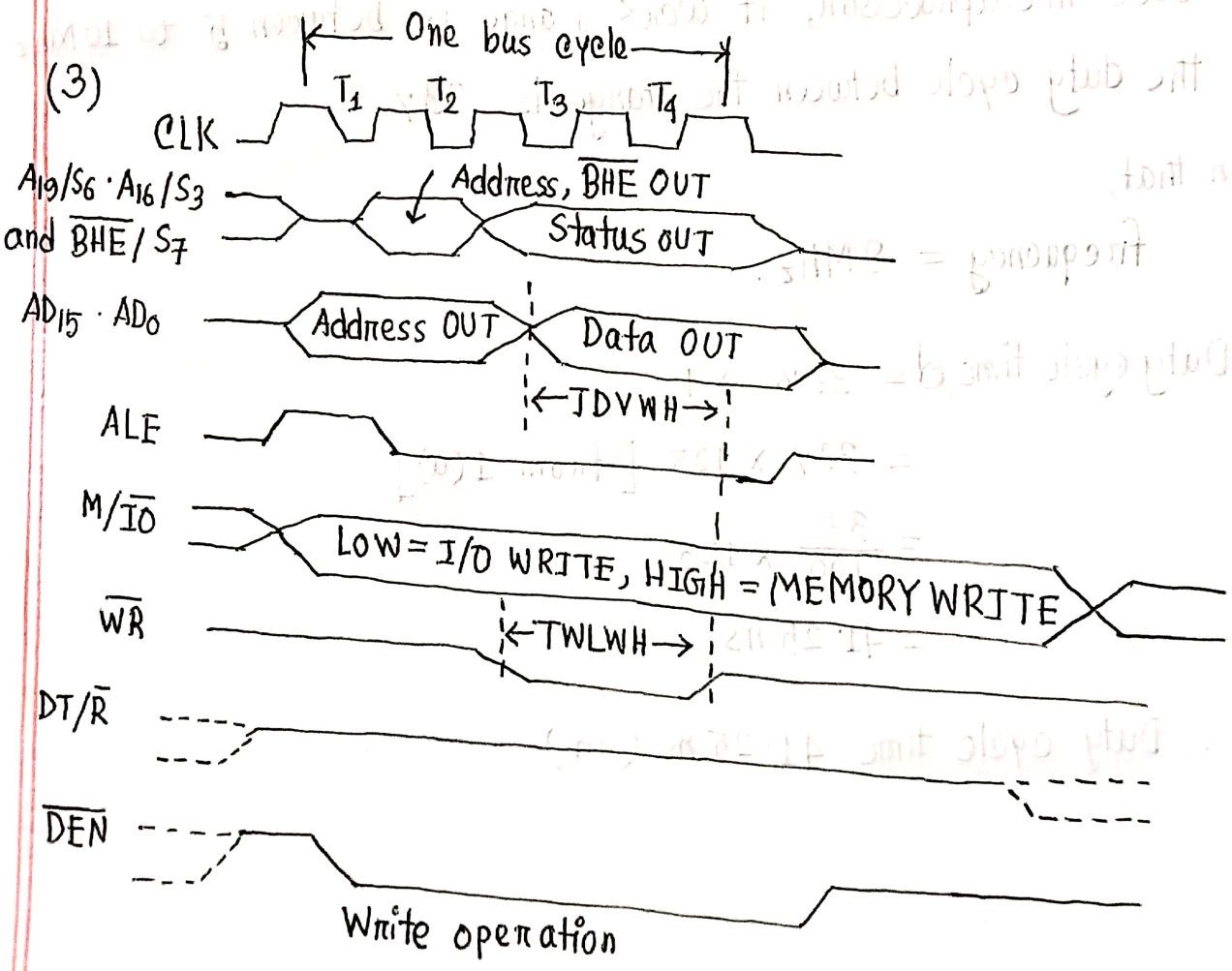
$= (4 \times 125)$ ns [From 1(a)]

$= 500$ ns

(Ans)

(2) In 8086 microprocessor, there are two grounds pins. One is on pin 1 and another is on pin 20th, it is used to ensure the data flow should been in the continuous and inner data and address are move to the chip as an efficient manner in another thing to reduce the heat and safe the components.

(3)



When processor is ready to start the bus cycle, it put a pulse to ALE during T_1. Before the failing edge, the address, BHE, M/IO, DEN and DT/R must be stable, for example, DEN= high and DT/R = ~~low~~ ~~for~~ 0 for input or DT/R = 1 for output. ~~After the failing edge of ALE~~

(4) (a) For MOV AL, [57h] need 1 bus cycle.

Here, $A_0 = 1$, $\overline{BHE} = 0$

(b) For MOV AX, [159h] need 2 bus cycle.

Here, for first bus cycle,

$A_0 = 1$, $\overline{BHE} = 0$

for 2nd bus cycle,

$A_0 = 0$, $\overline{BHE} = 1$

(Ans)

(5) Given that,

the TYPE, nn = 137

∴ To get effective address from IP:CS is:

IP = (nn x 4)

and, CS = (nn x 4)+2

So, IP for TYPE 137, IP = $(137 \times 4) = (548)_{10}$

$= 0224h$

And, CS for TYPE 137, CS = $(137 \times 4)+2 = (550)_{10}$

$= 0226h$

So, the location for IP are 0224h and 0225h

And, the location for CS are 0226h and 0227h

(Ans)

(6) Given that,

Given that, the CS of the ISR is BBH

So, the decimal of BB is 187.

We Know,

CS of ISR of type N = (4n)+2

$\therefore 4n+2 = 187$

$\Rightarrow 4n = 187-2$

$\Rightarrow 4n = 185$

$\Rightarrow n = \frac{185}{4}$

$\Rightarrow n = 46.25$

≈ 46

(Ans)

(07) 8259 combines the multi interrupt input sources into a single interrupt output. This PIC receives an interrupt request from an I/O device and tells the microprocessor.

The interrupt handling capability of processors 8085 and 8086 can be improved till 64 by cascading 8259 PIC. In 8259 PIC, there are 8 interrupt request pins. Interrupts can be cascading by using master-slave configuration.

To handle 36 interrupts we need –

8259 Master - 1

8259 Slaves - 5

So, a total of 6 8259 PICs are needed to handle 36 interrupts. Also, there are no further 8259 PICs are required as using 5 slaves we can manage 5*8 = 40 interrupts.