CSE341 Final

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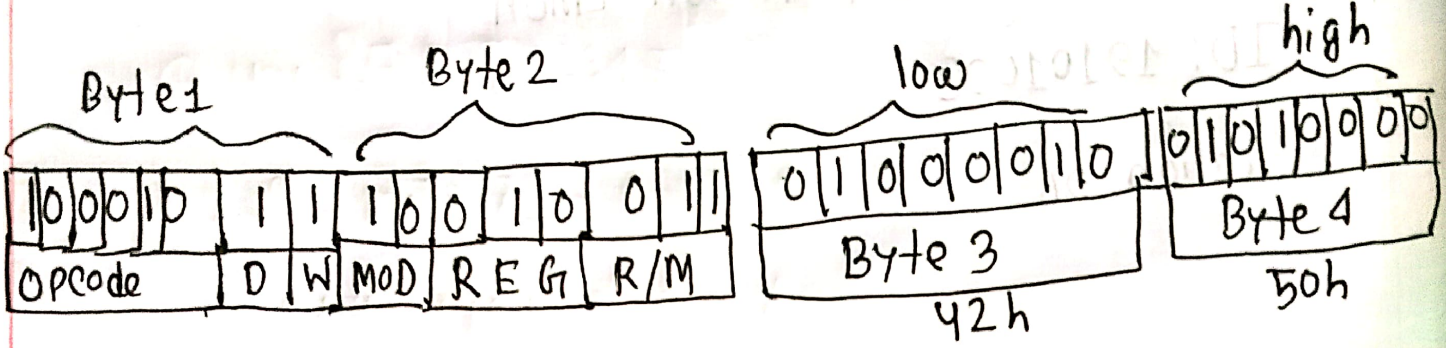
Section: 06

Ans: to the Q. No 1(a)

8B 934250h = 1000 1011 1001 0011 0100 0010 0000 1010 0000



It is 16 bit because it's W = 1

It's 011 shows BP+DI+ 16b address mode

low byte = 42h

high byte = 50h

Answer to the Q. No 1(b)

MOV [BX + 101], DL

1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1
opcode						D	W	MOD		REG			R/M		

$= (1000100010111)_2$

$= (10427)_8$ (Ans)

Answer to the Q. NO 2

(i) MOV DH, [12345 H]

(ii) MOV AH, [12347 H]

$f = 70\ MHz$

duty cycle of 70%.

$T = \frac{1}{70 \times 10^6} = 14.28\ ns$

duty cycle $= 14.28 \times .7 = 9.9\ ns$

bus cycle $= 4 \times 14.28 = 57.12\ ns$

For two move operation total time

$= 2 \times 57.12\ ns$

$= 114.24\ ns$

Stay low clock cycle $= \frac{114.24}{2}$

$= 57.12\ ns$

Ans: to the Q No 3

(b)

$$B7D72 - (B021 \times 10)$$

$$= B7D72 - B0210$$

$$= 7B62$$