CSE460: VLSI Design

Section 04

Assignment 03 (Lab)

Deadline: 16.08.22

Rules:
You need to submit the schematic diagrams drawn on dsch2 window, timing diagrams and screenshots of some simulation results. Write a brief description explaining the results for each of the problems.

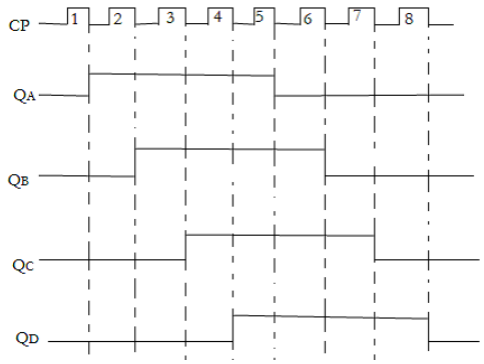
Problems:

1. Consider the following logic function,

   Y = ((A + B) C) + D

   Implement the given function on dsch2 using CMOS logic & show the corresponding timing diagram.
   [Hint: You should use "clock" as input for A, B, C & D.]

2. Refer to your **lab sheet of experiment 5**.
   In class, we have successfully implemented a negative edge-triggered D flip-flop. For this problem, you need to successfully implement the **negative edge-triggered D flip-flop** once again. After that, you need to construct a **controller block** and **connect with the flip-flop** to make a **D flip-flop with set-reset operations**. Finally with the designed block, you need to **implement a 4 bit Johnson counter**.
   [Hint: The controller circuit, the connection between controller & D flip-flop block and the Johnson counter circuit are given on your **lab sheet**.]
   Show the corresponding timing diagram of the Johnson counter. Your output should be something like this.



*****Complete the assignment by yourself. Copying will be strictly dealt with.**