Computer-Aided VLSI System Design
Homework 5: APR

TA: 林祐丞 d10943005@ntu.edu.tw **Due Tuesday, Dec. 6, 14:00**

TA: 羅宇呈 f08943129@ntu.edu.tw

Data Preparation

1. The related files below are needed to finish APR
   (You can find all files under **/home/raid7_4/raid1_1/ PnR/SOCE_Lab/library**)
   - **design**
     A. Your core_syn.v from HW3
     B. Your core_syn.sdc from HW3
   - **celtic**
     A. slow.cdB
   - **Capacitance Table**
     A. tsmc013.capTbl
   - **tsmc13_8lm.cl**
     A. icecaps_8lm.tch
   - **gds**
     A. tsmc13gfsg_fram.gds
     B. sram_*.gds (in sram_lef.zip)
   - **lef**
     A. tsmc13fsg_8lm_cic.lef
     B. antenna_8.lef
     C. sram_*.vclef (in sram_lef.zip)
     D. sram_*_ant.lef (in sram_lef.zip)
   - **lib**
     A. slow.lib
     B. sram_*_slow_syn.lib
   - streamOut.map

Introduction

In this homework, you should use Innovus to do P&R using your design in **HW3**. Note that the .sdc file is not provided. You should create them by yourself.

Specifications

1. Top module name: **core**
2. Use only worst case library for APR.
   - **AV_func_mode_max** for both **Setup Analysis View** and **Hold Analysis View**
3. Generate core_syn.sdc from the synthesis stage by the below command:

```
write_sdc Netlist/core_syn.sdc -version 1.8
```

4. Process related to IO Pad can be skipped if there is no IO Pad in your design.
5. Process related to scan chain can be skip
6. At least one power stripe in your design.
7. Use the below command to analyze the area
   (The command destroys your design. Remember to save your design files first!!)

```
innovus #> analyzeFloorplan
```

Design Description

1. Perform place & route using Innovus.
2. Run simulation after APR.
   - Remember to modify the name of .sdf file in your testbench.

Submission

1. Create a folder named **studentID_hw5**, and put all below files into the folder
   - ***_cts.sdc** (Your sdc file for clock tree synthesis)
   - **core.gds**
   - **core_pr.v**
   - **core_pr.sdf**
   - **mmmc.view**
   - **design.txt**
   - **report.pdf**

   Note: Use **lower case** for the letter in your student ID. (Ex. r07943001_hw1)

2. Compress the folder **studentID_hw5** in a **tar file** named **studentID_hw5_v*k*.tar** (***k* is the number of version, *k* =1,2,…)**

```
tar -cvf studentID_hw5_vk.tar StudentID_hw5
```

TA will only check the last version of your homework.

Note: Use **lower case** for the letter in your student ID. (Ex. d06943027_hw5_v1)

3. Submit to NTU COOL

Grading Policy

TA will test your result using **tb3** with the following command. Remember to make sure your P&R result is correct.

```
ncverilog testbench.v core_pr.v tsmc13_neg.v sram_*.v \
          +ncmaxdelays +define+SDF+tb3 +access+r
```

The testbench can be found in NTU COOL (HW3-二次繳交).

1. Correctness of mmmc.view setting: **10%**
2. Correctness of simulation after APR: **30%**
3. APR report: **60%**