Computer-Aided VLSI System Design
Homework 4 Report

Due Tuesday, Nov. 22, 14:00

Student IDs: r11943124

Student Names: 曾郁瑄

Questions and Discussion

1. Fill in the blanks

Physical category		
Design Stage	Description	Value
Gate-level Simulation	Cycle time for Gate-level Simulation (ex. 10ns)	8
	Area for Synthesis (ex. 50000μm^2)	18352.28862
	Gate-level Simulation Time for f1	14024
	Gate-level Simulation Time for f2	14024
	Gate-level Simulation Time for f3	14608
	Gate-level Simulation Time for f4	13833
	Gate-level Simulation Time for f5	13848
	Gate-level Simulation Time for f6	13857
	Gate-level Simulation Time for f7	13865

2. Specify the methods you adopted for low-power design. (10pts)
   a. 減少運算時的 cycle 數。
   b. 減少判斷式的數量，簡化邏輯。
   c. 接收測資時讓其中一個 register 不變動。
   d. 將收測資與計算的 register 減少，減少面積同時也降低功耗。
   e. Synthesis 時使用 clock gating、max_fanout 節省動態功耗。