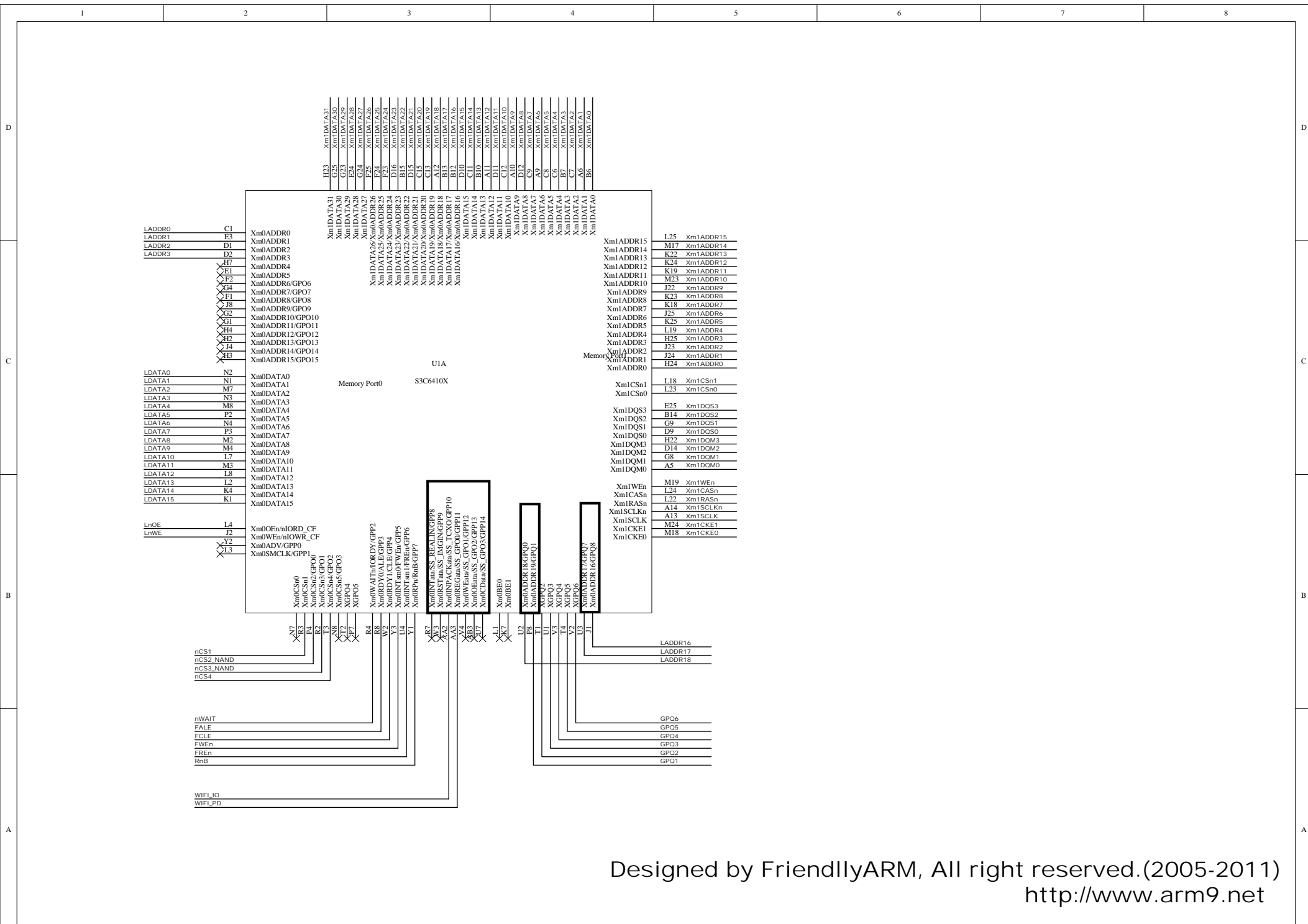
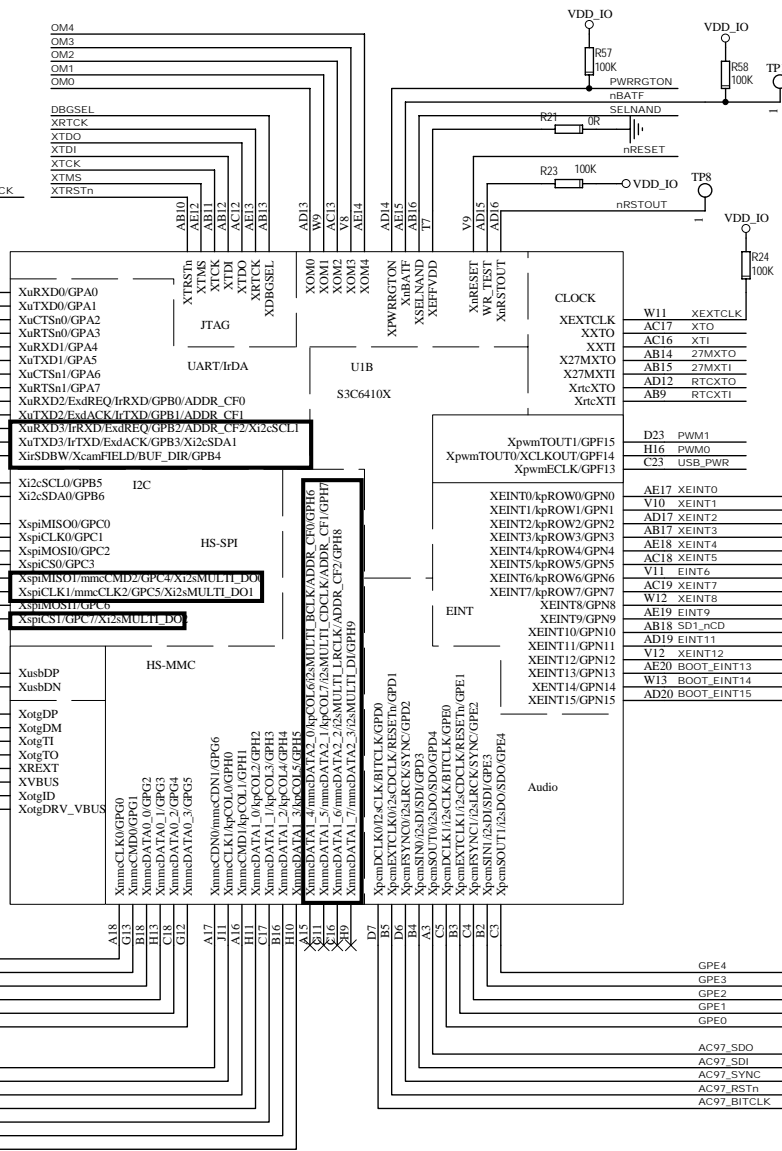
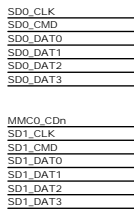
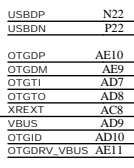
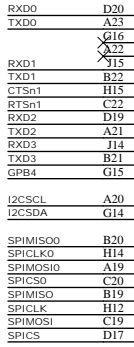
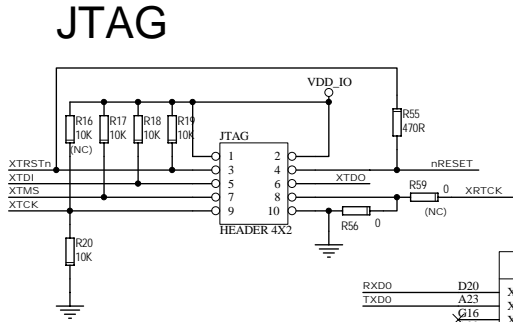


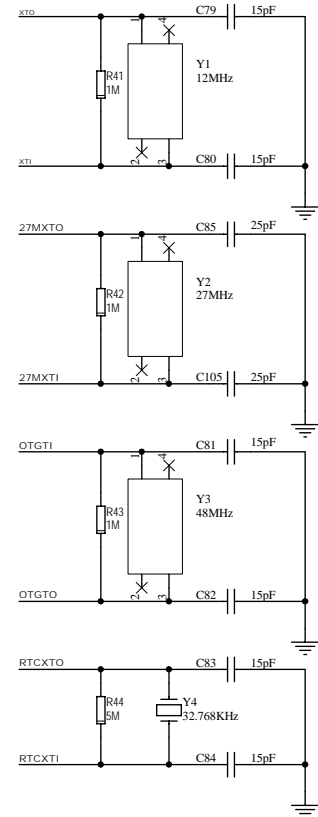
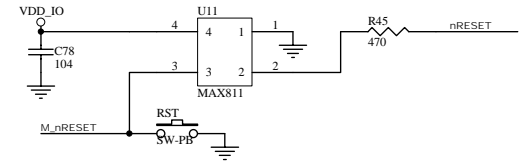
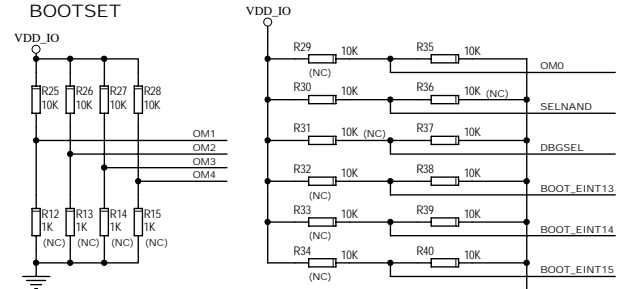
Tiny6410-1107

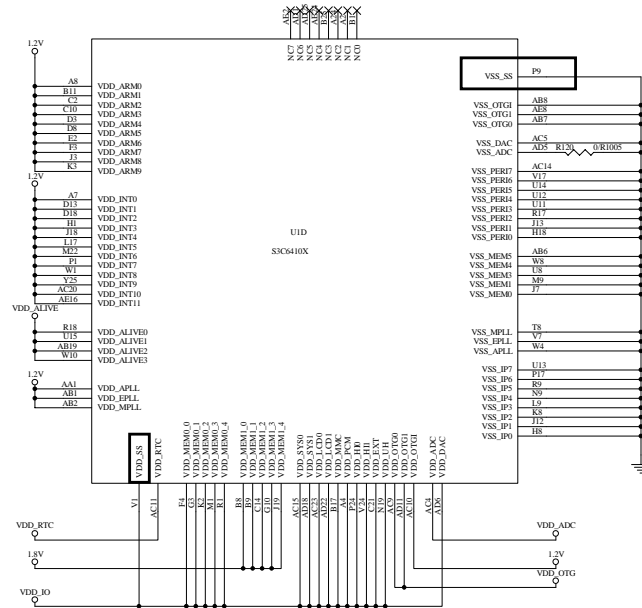


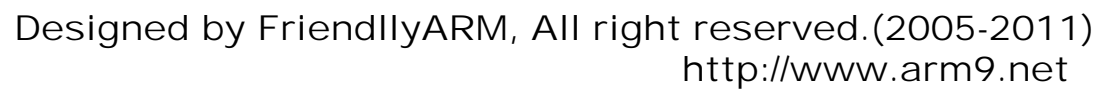
JTAG



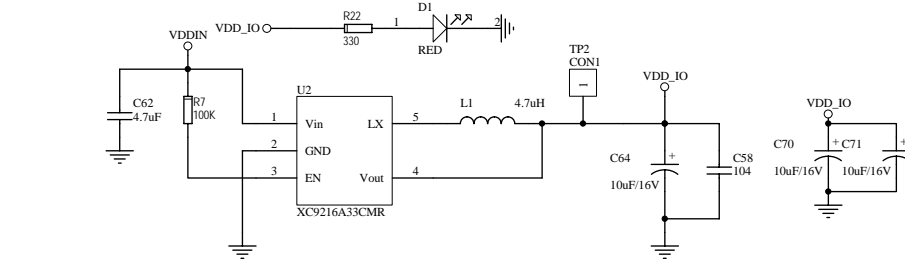
BOOTSET



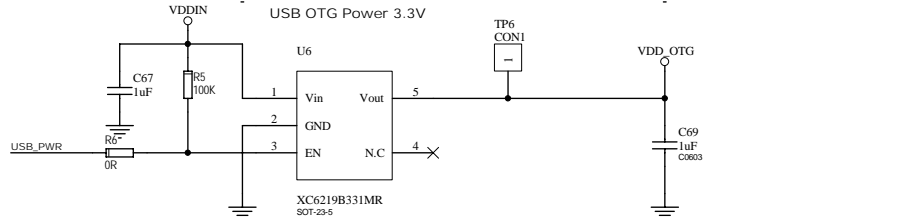
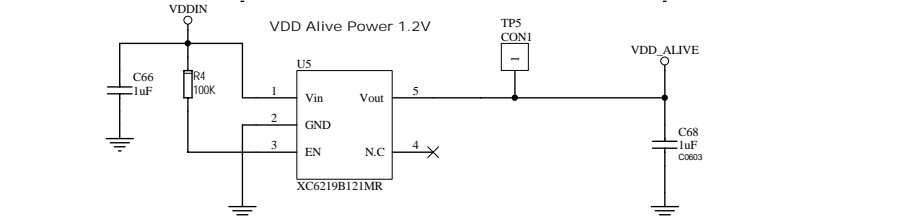
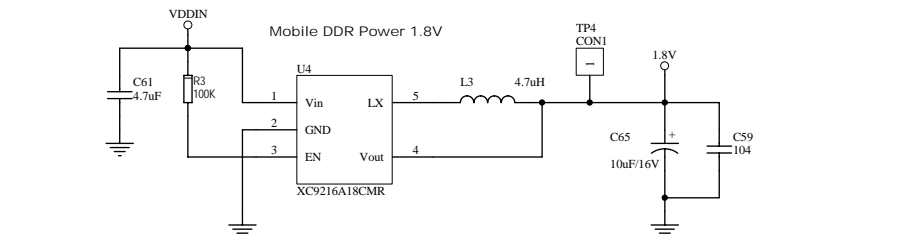
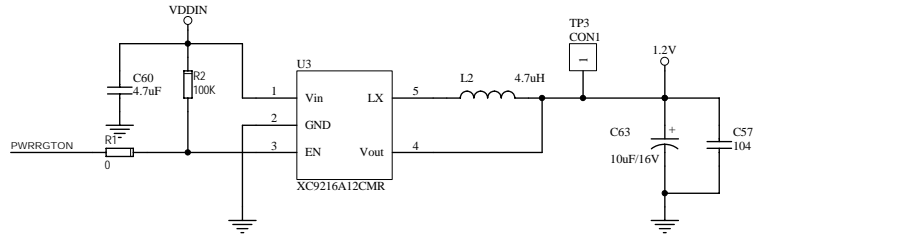




Power Supply



VDD INT Power 1.2V
(ARM Core, Internal block, MPLL, APLL, EPLL, VDD_OTGI)

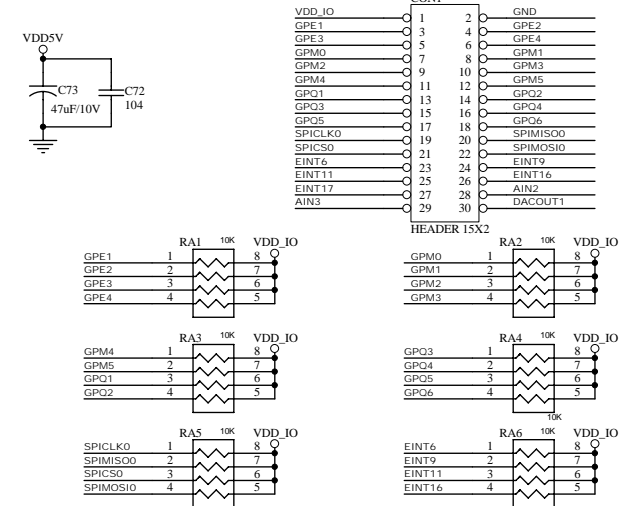


Designed by FriendlyARM, All right reserved.(2005-2011)

P1			
VDDIN	1	2	GND
VD23	3	4	VD22
VD21	5	6	VD20
VD19	7	8	VD18
VD15	9	10	VD14
VD13	11	12	VD12
VD11	13	14	VD10
VD7	15	16	VD6
VD5	17	18	VD4
VD3	19	20	VD2
VDEN	21	22	PWM1
VSYN	23	24	HSYN
VCLK	25	26	OTGDRV_VBUS
VBUS	27	28	XEINT8
OTGID	29	30	USBDN
OTGDM	31	32	USBDP
OTGDP	33	34	TSXP
TSXP	35	36	TSYM
TSYP	37	38	AIN1
AIN0	39	40	WIFI_PD
WIFI_IO	41	42	SD1_CMD
SD1_CLK	43	44	SD1_nCD
SD1_nCD	45	46	SD1_nWP
SD1_DAT0	47	48	SD1_DAT1
SD1_DAT2	49	50	SD1_DAT3
DACOUT0	51	52	PWM0
XEINT0	53	54	XEINT1
XEINT2	55	56	XEINT3
XEINT4	57	58	XEINT5
XEINT19	59	60	XEINT20
HEADER 30X2			

P2			
OM3	1	2	OM4
M_nRESET	3	4	VDD_RTC
RTSn1	5	6	CTSn1
TXD0	7	8	RXD0
TXD1	9	10	RXD1
TXD2	11	12	RXD2
TXD3	13	14	RXD3
SPIMOSI	15	16	SPIMISO
SPICLK	17	18	SPICS
I2CSCL	19	20	I2CSDA
SD0_CLK	21	22	SD0_CMD
MMC0_Cdn	23	24	MMC0_WPn
SD0_DAT0	25	26	SD0_DAT1
SD0_DAT2	27	28	SD0_DAT3
AC97_BITCLK	29	30	AC97_RSTn
AC97_SYNC	31	32	AC97_SDO
AC97_SDI	33	34	XEINT12
LADDR0	35	36	LADDR1
LADDR2	37	38	LADDR3
nCS1	39	40	XEINT7
nWAIT	41	42	nRESET
LnWE	43	44	LnOE
LDATA0	45	46	LDATA1
LDATA2	47	48	LDATA3
LDATA4	49	50	LDATA5
LDATA6	51	52	LDATA7
LDATA8	53	54	LDATA9
LDATA10	55	56	LDATA11
LDATA12	57	58	LDATA13
LDATA14	59	60	LDATA15
HEADER 30X2			

GPIO(兼容Mini6410的GPIO口CON6)



GPIO2(包含CMOS, 中断等)

