```
`timescale 1ns/1ps


module FIFO_EX (
input clk,
input Reset,
input [7:0] Data_IN,
input R,
input W,
output reg [7:0] Data_OUT,
output Empty,
output Full
);

    reg [7:0] wr_pointer;
    reg [7:0] rd_pointer;
    reg [8:0] Status;
    wire [7:0] RAM ;

    assign Full = (Status == 256);
    assign Empty = (Status == 0);

    always @ (posedge clk)
      if (Reset) begin
         wr_pointer <= 0;
         rd_pointer <= 0;
         Data_OUT <= 0;
         Status <= 0;
      end
      else if (W)
         wr_pointer <= wr_pointer + 1;
      else if (R) begin
         rd_pointer <= rd_pointer + 1;
         Data_OUT <= RAM;
      end
      else begin
         wr_pointer <= wr_pointer;
         rd_pointer <= rd_pointer;
         Data_OUT <= Data_OUT;
         Status <= Status;
      end

    always @ (posedge clk)
      if (R && !W && (Status != 0))
         Status <= Status - 1;
      else if (W && !R && (Status != 256))
         Status <= Status + 1;
      else
         Status <= Status;

Endmodule
```

Offset in: $t1 + ts + t_{clk}$

Offset out: $td + t4 + t_{clk}$

Min clock period = $td + \max(t2, t3) + ts + t_{clk}$