------------------------------------------------------------------------------------------------------------

`timescale 1ns**/**1ps

**module** FIFO\_EX **(**

**input** clk**,**

**input** Reset**,**

**input** **[**7**:**0**]** Data\_IN**,**

**input** R**,**

**input** W**,**

**output** **reg** **[**7**:**0**]** Data\_OUT**,**

**output** Empty**,**

**output** Full

**);**

**reg** **[**7**:**0**]** wr\_pointer**;**

**reg** **[**7**:**0**]** rd\_pointer**;**

**reg** **[**8**:**0**]** Status**;**

**wire** **[**7**:**0**]** RAM **;**

**assign** Full **=** **(**Status **==** 256**);**

**assign** Empty **=** **(**Status **==** 0**);**

**always** **@** **(posedge** clk**)**

**if** **(**Reset**)** **begin**

wr\_pointer **<=** 0**;**

rd\_pointer **<=** 0**;**

Data\_OUT **<=** 0**;**

Status **<=** 0**;**

**end**

**else** **if** **(**W**)**

wr\_pointer **<=** wr\_pointer **+** 1**;**

**else** **if** **(**R**)** **begin**

rd\_pointer **<=** rd\_pointer **+** 1**;**

Data\_OUT **<=** RAM**;**

**end**

**else** **begin**

wr\_pointer **<=** wr\_pointer**;**

rd\_pointer **<=** rd\_pointer**;**

Data\_OUT **<=** Data\_OUT**;**

Status **<=** Status**;**

**end**

**always** **@** **(posedge** clk**)**

**if** **(**R **&&** **!**W **&&** **(**Status **!=** 0**))**

Status **<=** Status **-** 1**;**

**else** **if** **(**W **&&** **!**R **&&** **(**Status **!=** 256**))**

Status **<=** Status **+** 1**;**

**else**

Status **<=** Status**;**

**Endmodule**

Offset in: t1 + ts + tclk

Offset out: td + t4 + tclk

Min clock period = td + max (t2, t3) + ts + tclk