Quiz **02/03/24**

Bangladesh University of Engineering and Technology
Department of Computer Science and Engineering
CSE 206 - Digital Logic Design Sessional

Total Marks: 70 **Duration: 60 minutes**

Student Name: **Student ID:**

(For Examiner's Use Only)

1	2	3	4	5	6	7	8

Instructions

1. There are 5 Multiple Choice Questions and 5 True/False questions and 6 short questions in the script. Make sure all the questions are printed clearly before you start writing.

2. You should answer the all of the questions.

True/False Questions. Write T (for True) or F (for False) beside each of the question. [5]

1. a) The master latch of a positive edge-triggered master-slave D flip flop is active only during level 1 of the clock.

T

b) Once an up/down counter begins its count sequence, it cannot be reversed.

F

c) You cannot use Priority Encoder as a normal encoder.

F

d) You will need at least two 8x1 multiplexer and two 2x1 multiplexer to build a 16x1 multiplexer.

F

e) The product-of-sums (POS) is basically the OR-ing of AND-ed terms.

F

Multiple Choice Questions. Mark (√) beside the answer which suits best. **[5]**

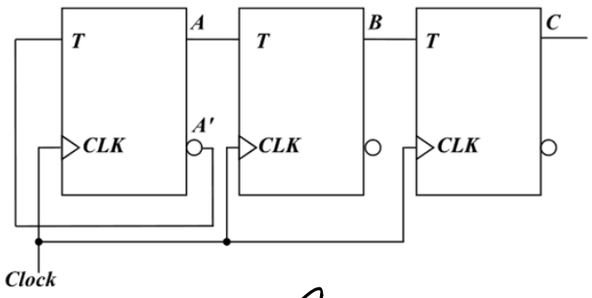
2. a) You have the following chips: 7404, 7408, 7432, 74138. What are the minimum chips required to solve: $\sum (8,11,13,15)$?

   i. 1x74138, 1x7408 ii. 1x74138, 1x7432
   iii. 2x74138, 1x7408 iv. 2x74138, 1x7432

   b) A MOD M and a MOD N up-counter when cascaded together results in a MOD _____ counter.

   i. M+N ii. M-N
   iii. M/N iv. M*N

   c) Assuming that the current state of the circuit (ABC) is 000, what will be the state of the circuit after 3 clock cycles?



   i. 111 ii. 101
   iii. 001 iv. 000

   d) If the number of n selected input lines is equal to 2^m then it requires _____ select lines.

   i. 2 ii. n
   iii. m iv. 2^n

   e) How many gates would be required to implement the following Boolean expression after simplification?

$$XY + X(X + Z) + Y(X + Z)$$

   i. 1 ii. 2
   iii. 3 iv. 4

(Idea from Zubayer kayes Rafid) Boss

Short Questions

3. Suppose you only have some 2 to 4 decoders and some 4 to 2 priority encoders with priority $0 < 1 < 2 < 3$. Now, you need a priority encoder with priority $3 < 2 < 1 < 0$. How would you implement this? **[10]**

$\Rightarrow$ $0<1<2<3$ → Given

I_3	I_2	I_1	I_0	Y_1	Y_0	V
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

Required $3<2<1<0$

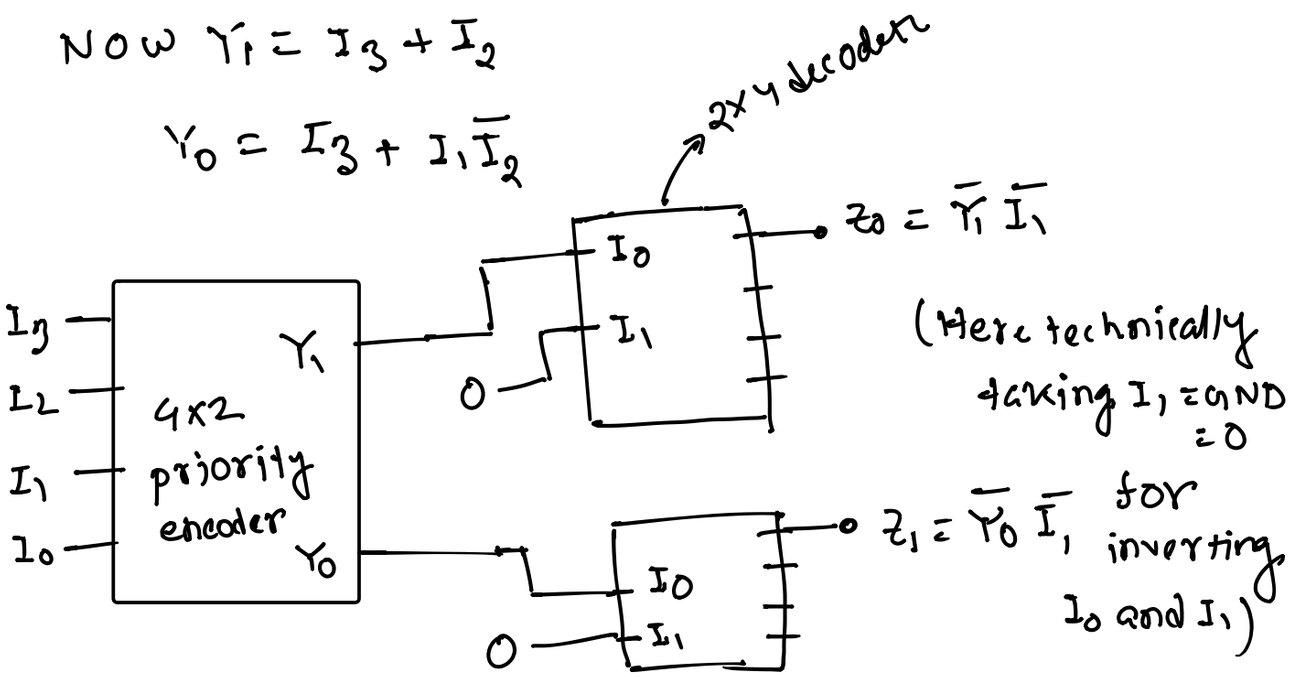
I_0	I_1	I_2	I_3	Z_1	Z_0	V
0	0	0	0	X	X	0
0	0	0	1	1	1	1
0	0	1	X	1	0	1
0	1	X	X	0	1	1
1	X	X	X	0	0	1

We see to get the required priority encoder

$Z_1 = \bar{Y}_1 \quad Z_0 = \bar{Y}_0$

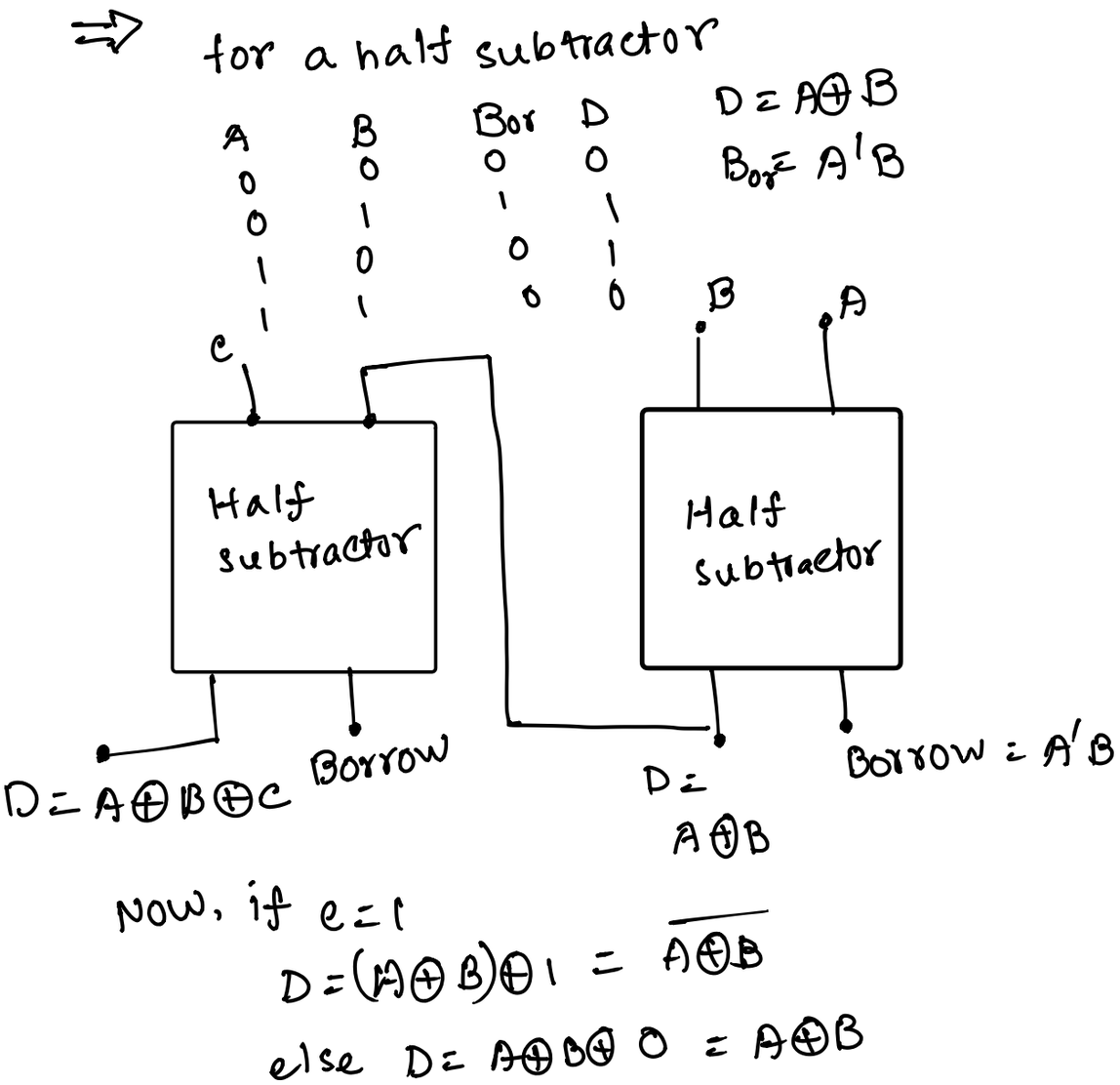
Now $Y_1 = I_3 + I_2$

$Y_0 = I_3 + I_1\bar{I}_2$



(Here technically taking I_1 = GND = 0 for inverting I_0 and I_1)

4. Suppose you have two 2-bit numbers A and B and an additional input bit C. When C is 0, you have to output the bitwise XOR of A and B. When C is 1, you have to output the bitwise XNOR of A and B. Design a combinatorial circuit using only half subtractors. You can assume to have access to VCC and GND. **[10]**



Now, if $e = 1$

$D = (A \oplus B) \oplus 1 = \overline{A \oplus B}$

else $D = A \oplus B \oplus 0 = A \oplus B$

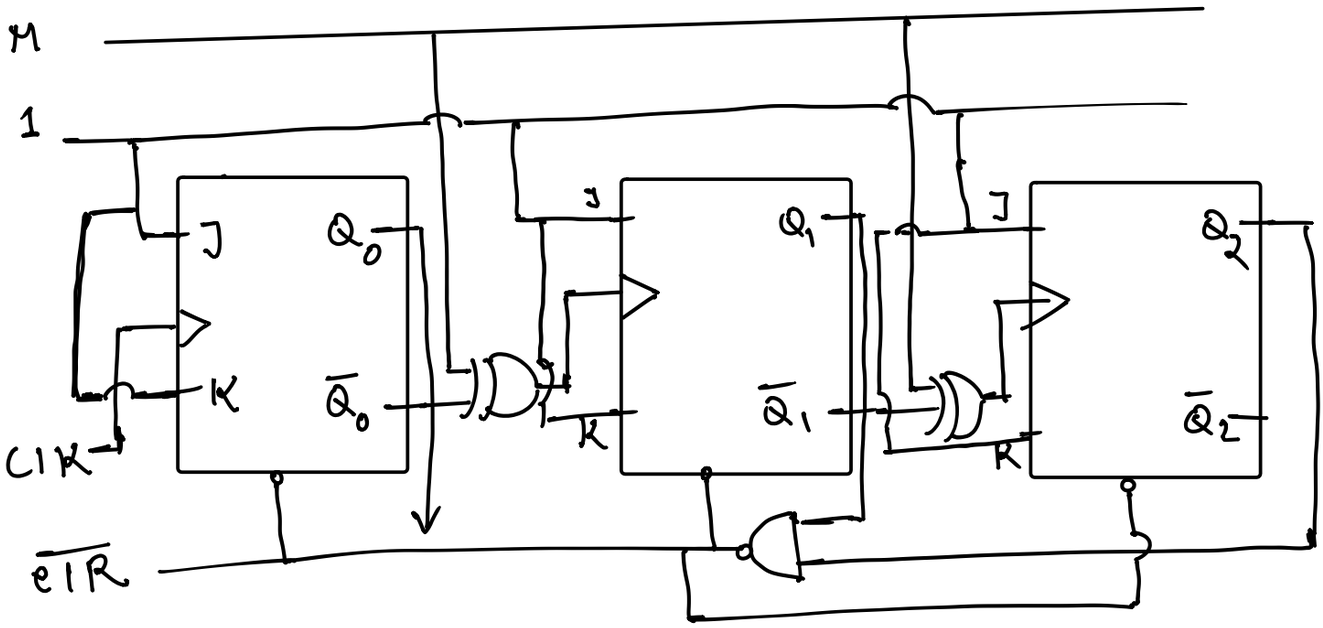
5. Design an asynchronous MOD - 6 up/down counter using positive edge-triggered J-K flip-flops. The counter should have two modes of operation: down-counting when the mode bit M is set to 1, and up-counting when M is set to 0. **[10]**

M = 0 → up counter

M = 1 → down counter

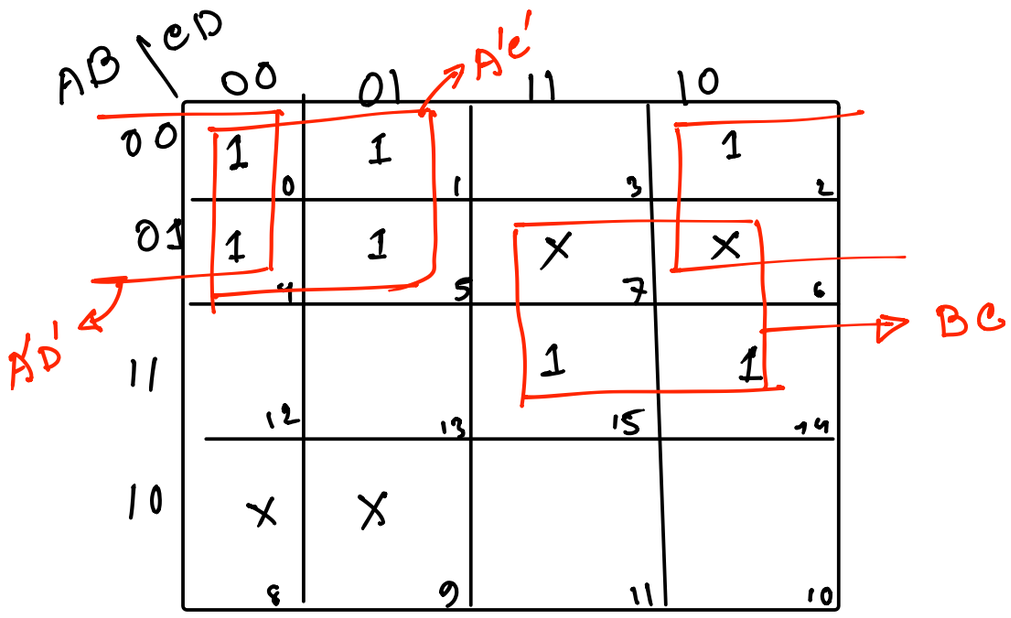
reset when output is 6 = 110 (Hint XOR Q_2Q_1)

for mod -6 up/down counter, no of ff = $\lceil \log_2 6 \rceil = 3$



6. Simplify the function into the minimal SOP form using K-Map. **[10]**

$\sum(0,1,2,4,5,14,15) + d(6,7,8,9)$



$S = A'D' + A'C' + BC$

7 A sequential circuit has two T flip-flops A and B, and an input x. The circuit can be described by the following input equations: **[10]**

$$T_A = Bx,$$
$$T_B = A'x$$

Derive the next state equations $A_{(t+1)}$ and $B_{(t+1)}$. Also, draw the state diagram of this circuit.

$A_{t+1} = T_A \oplus Q_A$
$B_{t+1} = T_B \oplus Q_B$
} Because in the next state toggling will occur if the input i.e, T_A and $T_B = 1$

$A_{t+1} = Bx \oplus Q_A$
$B_{t+1} = A'x \oplus Q_B$

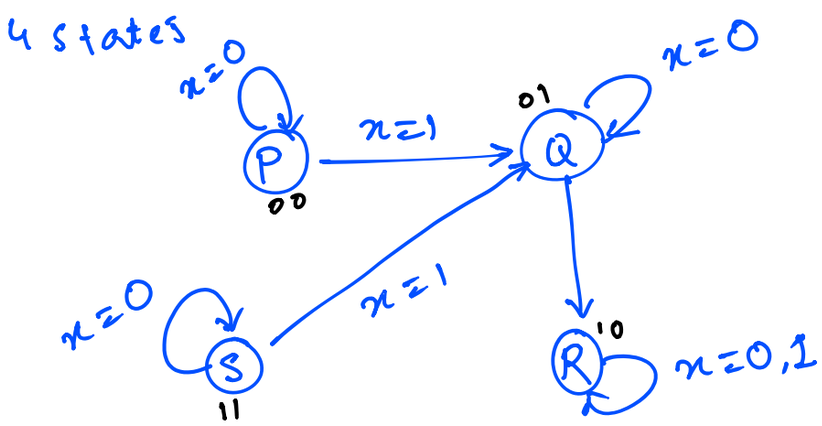
if $x = 0$; $A_{t+1} = Q_A$; $B_{t+1} = Q_B$
toggling will not occur

else, $x = 1$; $A_{t+1} = B \oplus Q_A = Q_B \oplus Q_A$

$B_{t+1} = A' \oplus Q_B = Q_A' \oplus Q_B$

PS		NS					
		$x=0$		$x=1$			
Q_A	Q_B	A_{t+1}	B_{t+1}	A_{t+1}	B_{t+1}		
P = 0	0	0	0	0	1		
Q = 0	1	0	1	1	0		
R = 1	0	1	0	1	0		
S = 1	1	1	1	0	1		

(Here $A = Q_A$; $B = Q_B$ present state of the flipflop)

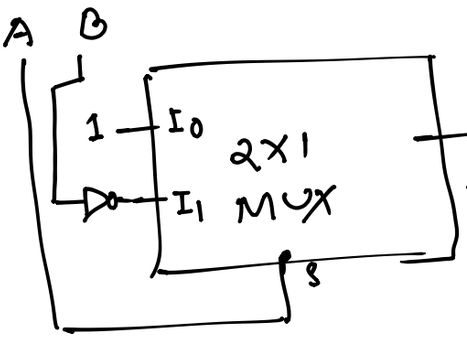


8. Desing NAND, NOR, XOR and XNOR Gates using minimum numbers of 2x1 multiplexers only. **[10]**

A	B	$(A \cdot B)'$	$(A+B)'$	$A \oplus B$	$\overline{A \oplus B}$
0	0	1	1	0	1
0	1	1	0	1	0
1	0	1	0	1	0
1	1	0	0	0	1

2x1 mux : A – selection bit

NAND:



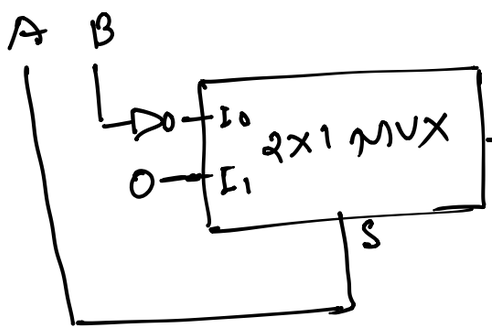
if A = S = 0; I_0 will activate and output is always 1

A = S = 1 ; I_1 " " " "

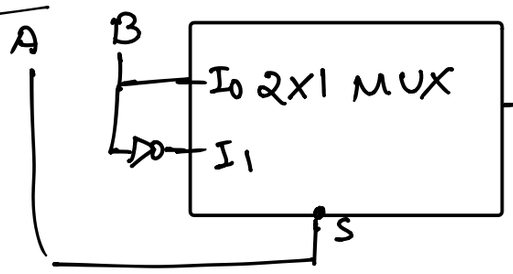
$I_0S' + I_1S$ = output

I_0 & I_1 $\overline{B}$

NOR:



XOR:



XNOR: