Synthesis Report

Wed Apr 15 23:09:50 2020

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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Reading design: KSA16.prj
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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "KSA16.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "KSA16"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : KSA16
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v" into library work
Parsing module .
Parsing module .
```

```
Parsing module .
Parsing module .
Parsing module .
=========================================================================
*                          HDL Elaboration                              *
=========================================================================
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
WARNING:HDLCompiler:1127 - "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v" Line 65: Assignment to A5 ignored, since the identifier i
Elaborating module .
=========================================================================
*                           HDL Synthesis                               *
=========================================================================
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v".
INFO:Xst:3210 - "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v" line 60: Output port  of the instance > is unconnected or connected
INFO:Xst:3210 - "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v" line 60: Output port  of the instance > is unconnected or connected
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INFO:Xst:3210 - "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v" line 65: Output port  of the instance  is unconnected or connected t
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v".
    Summary:
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v".
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v".
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/KoggeStoneAdder.v".
    Summary:
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Xors                                                 : 32
 1-bit xor2                                            : 32
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Xors                                                 : 32
 1-bit xor2                                            : 32
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block KSA16, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                           Partition Report                            *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                            Design Summary                             *
=========================================================================
Top Level Output File Name         : KSA16.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 54
#      LUT2                        : 6
#      LUT3                        : 8
#      LUT4                        : 17
#      LUT5                        : 12
#      LUT6                        : 11
# IO Buffers                       : 49
#      IBUF                        : 32
#      OBUF                        : 17
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice LUTs:                   54  out of  63400     0%
```

```
    Number used as Logic:                54  out of  63400     0%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     54
   Number with an unused Flip Flop:      54  out of     54   100%
   Number with an unused LUT:             0  out of     54     0%
   Number of fully used LUT-FF pairs:     0  out of     54     0%
   Number of unique control sets:         0
IO Utilization:
 Number of IOs:                         49
 Number of bonded IOBs:                 49  out of    210    23%
Specific Feature Utilization:
-------------------------
Partition Resource Summary:
-------------------------
  No Partitions were found in this design.
-------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
No clock signals found in this design
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 3.651ns
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 304 / 17
-------------------------------------------------------------------------
Delay:               3.651ns (Levels of Logic = 9)
  Source:            a<1> (PAD)
  Destination:       cout (PAD)
  Data Path: a<1> to cout
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   0.001   0.575  a_1_IBUF (a_1_IBUF)
     LUT4:I0->O            1   0.097   0.379  bc1<3>/G_SW0 (N8)
     LUT5:I3->O            2   0.097   0.383  bc1<3>/G (g3<3>)
     LUT6:I4->O            2   0.097   0.299  bc2<7>/G1 (bc2<7>/G)
     LUT5:I4->O            1   0.097   0.379  bc2<7>/G2 (g4<7>)
     LUT6:I4->O            1   0.097   0.295  bc3_15/G3 (bc3_15/G2)
     LUT5:I4->O            1   0.097   0.379  bc3_15/G4_SW0 (N12)
     LUT5:I3->O            1   0.097   0.279  bc3_15/G4 (g5)
     OBUF:I->O                 0.000          cout_OBUF (cout)
    ----------------------------------------
    Total                      3.651ns (0.680ns logic, 2.971ns route)
                               (18.6% logic, 81.4% route)
=========================================================================
Cross Clock Domains Report:
--------------------------
=========================================================================
Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.75 secs

-->
Total memory usage is 4625492 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    1 (   0 filtered)
Number of infos    :    8 (   0 filtered)
```