Synthesis Report

Wed Apr 15 23:01:49 2020

```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Reading design: CSA.prj
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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "CSA.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "CSA"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : CSA
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:/Users/ALI/Desktop/New folder (2)/CSA .v" into library work
Parsing module .
Parsing module .
```

```
WARNING:HDLCompiler:936 - "C:/Users/ALI/Desktop/New folder (2)/CSA .v" Line 11: Keyword 'unsigned' is not allowed here in this mode of veril
Parsing module .
WARNING:HDLCompiler:936 - "C:/Users/ALI/Desktop/New folder (2)/CSA .v" Line 15: Keyword 'unsigned' is not allowed here in this mode of veril
=========================================================================
*                            HDL Elaboration                            *
=========================================================================
Elaborating module .
Elaborating module .
Elaborating module .
=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/CSA .v".
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/CSA .v".
    Found 5-bit adder for signal  created at line 12.
    Found 5-bit adder for signal  created at line 12.
    Summary:
        inferred   2 Adder/Subtractor(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/CSA .v".
    Summary:
        inferred   1 Multiplexer(s).
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 14
 5-bit adder                                          : 14
# Multiplexers                                         : 3
 5-bit 2-to-1 multiplexer                             : 3
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 7
 5-bit adder carry in                                 : 7
# Multiplexers                                         : 3
 5-bit 2-to-1 multiplexer                             : 3
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block CSA, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                            Partition Report                           *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                            Design Summary                             *
=========================================================================
Top Level Output File Name         : CSA.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 36
#      LUT2                        : 10
#      LUT3                        : 6
#      LUT5                        : 16
#      LUT6                        : 4
# IO Buffers                       : 50
#      IBUF                        : 33
#      OBUF                        : 17
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice LUTs:                  36  out of  63400     0%
    Number used as Logic:               36  out of  63400     0%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    36
   Number with an unused Flip Flop:     36  out of     36   100%
   Number with an unused LUT:            0  out of     36     0%
   Number of fully used LUT-FF pairs:    0  out of     36     0%
   Number of unique control sets:        0
IO Utilization:
 Number of IOs:                         50
 Number of bonded IOBs:                 50  out of    210    23%
Specific Feature Utilization:
---------------------------
Partition Resource Summary:
---------------------------
```

```
  No Partitions were found in this design.
--------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
No clock signals found in this design
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 4.912ns
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 327 / 17
-------------------------------------------------------------------------
Delay:               4.912ns (Levels of Logic = 12)
  Source:            x<1> (PAD)
  Destination:       s<15> (PAD)
  Data Path: x<1> to s<15>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   0.001   0.693  x_1_IBUF (x_1_IBUF)
     LUT5:I0->O            2   0.097   0.299  adder1/Madd_out_Madd_xor<3>121 (adder1/Madd_out_Madd_xor<3>121)
     LUT3:I2->O            3   0.097   0.305  adder1/Madd_out_Madd_xor<3>122 (adder1/Madd_out_Madd_xor<3>12)
     LUT5:I4->O            2   0.097   0.384  m1/Mmux_out511 (m1/Mmux_out511)
     LUT3:I1->O            3   0.097   0.305  m1/Mmux_out512 (m1/Mmux_out51)
     LUT5:I4->O            2   0.097   0.384  m2/Mmux_out511 (m2/Mmux_out511)
     LUT3:I1->O            2   0.097   0.299  m2/Mmux_out512 (m2/Mmux_out51)
     LUT5:I4->O            4   0.097   0.309  m2/Mmux_out321 (m2/Mmux_out32)
     LUT5:I4->O            2   0.097   0.383  m3/Mmux_out511 (m3/Mmux_out511)
     LUT3:I1->O            2   0.097   0.299  m3/Mmux_out512 (m3/Mmux_out51)
     LUT5:I4->O            1   0.097   0.279  m3/Mmux_out11 (c_out_OBUF)
     OBUF:I->O                 0.000          c_out_OBUF (c_out)
    ----------------------------------------
    Total                      4.912ns (0.971ns logic, 3.941ns route)
                                       (19.8% logic, 80.2% route)
=========================================================================
Cross Clock Domains Report:
---------------------------
=========================================================================
Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.71 secs

-->
Total memory usage is 4625452 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    2 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```