Synthesis Report

Wed Apr 15 23:12:13 2020

```
Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Reading design: pervious_info.prj
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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "pervious_info.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "pervious_info"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : pervious_info
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v" into library work
Parsing module .
Parsing module .
```

```
Parsing module .
=========================================================================
*                            HDL Elaboration                            *
=========================================================================
Elaborating module .
Elaborating module .
WARNING:HDLCompiler:1127 - "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v" Line 138: Assignment to P4 ignored, since the ident
Elaborating module .
WARNING:HDLCompiler:1127 - "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v" Line 147: Assignment to T0 ignored, since the ident
WARNING:HDLCompiler:413 - "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v" Line 148: Result of 2-bit expression is truncated to
WARNING:Xst:2972 - "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v" line 138. All outputs of instance  of block  are unconnecte
=========================================================================
*                           HDL Synthesis                               *
=========================================================================
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v".
WARNING:Xst:647 - Input  is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to
INFO:Xst:3210 - "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v" line 138: Output port
 of the instance  is unconnected or connected to loadless signal.
    Found 2-bit adder for signal  created at line 150.
    Found 2-bit adder for signal  created at line 151.
    Found 2-bit adder for signal  created at line 152.
    Summary:
        inferred   3 Adder/Subtractor(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v".
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs t
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs t
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/New folder (2)/using pervious digit .v".
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the us
    Summary:
        inferred   4 Latch(s).
        inferred  30 Multiplexer(s).
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 3
 2-bit adder                                           : 3
# Latches                                              : 16
 1-bit latch                                           : 16
# Multiplexers                                         : 120
 1-bit 2-to-1 multiplexer                              : 120
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Adders/Subtractors                                   : 3
 2-bit adder                                           : 3
# Multiplexers                                         : 120
 1-bit 2-to-1 multiplexer                              : 120
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
WARNING:Xst:3001 - This design contains one or more registers or latches with an active
   asynchronous set and asynchronous reset. While this circuit can be built,
   it creates a sub-optimal implementation in terms of area, power and
   performance. For a more optimal implementation Xilinx highly recommends
   one of the following:
          1) Remove either the set or reset from all registers and latches if
             not needed for required functionality
          2) Modify the code in order to produce a synchronous set
             and/or reset (both is preferred)
          3) Use the -async_to_sync option to transform the asynchronous
             set/reset to synchronous operation
             (timing simulation highly recommended when using this option)
  Please refer to http://www.xilinx.com search string "Artix7 asynchronous set/reset" for more details.
  List of register instances with asynchronous set and reset:
    T_1 in unit
    W_0 in unit
    W_1 in unit
    T_0 in unit
Optimizing unit  ...
Optimizing unit  ...
WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
Mapping all equations...
Building and optimizing final netlist ...
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
Found area constraint ratio of 100 (+ 5) on block pervious_info, actual ratio is 0.
Latch TW0/W_0 has been replicated 1 time(s) to handle iob=true attribute.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                           Partition Report                            *
=========================================================================
```

```
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                          Design Summary                               *
=========================================================================
Top Level Output File Name         : pervious_info.ngc
Primitive and Black Box Usage:
-------------------------------
# BELS                             : 63
#      GND                         : 1
#      LUT2                        : 3
#      LUT3                        : 28
#      LUT4                        : 15
#      LUT6                        : 16
# FlipFlops/Latches                : 15
#      LD                          : 15
# IO Buffers                       : 25
#      IBUF                        : 16
#      OBUF                        : 9
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice Registers:              12  out of  126800     0%
 Number of Slice LUTs:                   62  out of  63400     0%
    Number used as Logic:                62  out of  63400     0%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     62
   Number with an unused Flip Flop:      50  out of     62    80%
   Number with an unused LUT:             0  out of     62     0%
   Number of fully used LUT-FF pairs:    12  out of     62    19%
   Number of unique control sets:        14
IO Utilization:
 Number of IOs:                          26
 Number of bonded IOBs:                  25  out of    210    11%
    IOB Flip Flops/Latches:               3
Specific Feature Utilization:
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
-----------------------------------+-------------------------+-------+
Clock Signal                       | Clock buffer(FF name)   | Load  |
-----------------------------------+-------------------------+-------+
TW3/W_0_G(TW3/W_0_G:O)             | NONE(*)(TW3/W_0)        | 1     |
TW3/W_1_G(TW3/W_1_G:O)             | NONE(*)(TW3/W_1)        | 1     |
TW3/T_0_G(TW3/T_0_G:O)             | NONE(*)(TW3/T_0)        | 1     |
TW2/T_1_G(TW2/T_1_G:O)             | NONE(*)(TW2/T_1)        | 1     |
TW2/W_0_G(TW2/W_0_G:O)             | NONE(*)(TW2/W_0)        | 1     |
TW2/W_1_G(TW2/W_1_G:O)             | NONE(*)(TW2/W_1)        | 1     |
TW2/T_0_G(TW2/T_0_G:O)             | NONE(*)(TW2/T_0)        | 1     |
TW1/T_1_G(TW1/T_1_G:O)             | NONE(*)(TW1/T_1)        | 1     |
TW1/W_0_G(TW1/W_0_G:O)             | NONE(*)(TW1/W_0)        | 1     |
TW1/W_1_G(TW1/W_1_G:O)             | NONE(*)(TW1/W_1)        | 1     |
TW1/T_0_G(TW1/T_0_G:O)             | NONE(*)(TW1/T_0)        | 1     |
TW0/T_1_G(TW0/T_1_G:O)             | NONE(*)(TW0/T_1)        | 1     |
TW0/W_0_G(TW0/W_0_G:O)             | NONE(*)(TW0/W_0)        | 2     |
TW0/T_0_G(TW0/T_0_G:O)             | NONE(*)(TW0/T_0)        | 1     |
-----------------------------------+-------------------------+-------+
(*) These 14 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer_type
Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: 1.463ns
   Maximum output required time after clock: 1.409ns
   Maximum combinational path delay: No path found
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW3/W_0_G'
  Total number of paths / destination ports: 8 / 1
-------------------------------------------------------------------------
Offset:              1.290ns (Levels of Logic = 3)
  Source:            A<6> (PAD)
  Destination:       TW3/W_0 (LATCH)
  Destination Clock: TW3/W_0_G falling
  Data Path: A<6> to TW3/W_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.579  A_6_IBUF (A_6_IBUF)
```

```
     LUT4:I0->O            2   0.097   0.515  TW3/concatanate[3]_GND_3_o_AND_17_o1 (TW3/concatanate[3]_GND_3_o_AND_17_o)
     LUT3:I0->O            1   0.097   0.000  TW3/W_0_D (TW3/W_0_D)
     LD:D                     -0.028          TW3/W_0
    ----------------------------------------
    Total                      1.290ns (0.195ns logic, 1.095ns route)
                                       (15.1% logic, 84.9% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW3/W_1_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.427ns (Levels of Logic = 3)
  Source:            A<6> (PAD)
  Destination:       TW3/W_1 (LATCH)
  Destination Clock: TW3/W_1_G falling
  Data Path: A<6> to TW3/W_1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.716  A_6_IBUF (A_6_IBUF)
     LUT6:I0->O            2   0.097   0.515  TW3/concatanate[3]_GND_3_o_AND_15_o1 (TW3/concatanate[3]_GND_3_o_AND_15_o)
     LUT3:I0->O            1   0.097   0.000  TW3/W_1_D (TW3/W_1_D)
     LD:D                     -0.028          TW3/W_1
    ----------------------------------------
    Total                      1.427ns (0.195ns logic, 1.232ns route)
                                       (13.7% logic, 86.3% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW3/T_0_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.427ns (Levels of Logic = 3)
  Source:            A<7> (PAD)
  Destination:       TW3/T_0 (LATCH)
  Destination Clock: TW3/T_0_G falling
  Data Path: A<7> to TW3/T_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.716  A_7_IBUF (A_7_IBUF)
     LUT6:I0->O            2   0.097   0.515  TW3/concatanate[3]_GND_3_o_AND_13_o1 (TW3/concatanate[3]_GND_3_o_AND_13_o)
     LUT3:I0->O            1   0.097   0.000  TW3/T_0_D (TW3/T_0_D)
     LD:D                     -0.028          TW3/T_0
    ----------------------------------------
    Total                      1.427ns (0.195ns logic, 1.232ns route)
                                       (13.7% logic, 86.3% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW2/T_1_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.454ns (Levels of Logic = 3)
  Source:            A<5> (PAD)
  Destination:       TW2/T_1 (LATCH)
  Destination Clock: TW2/T_1_G falling
  Data Path: A<5> to TW2/T_1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            12   0.001   0.744  A_5_IBUF (A_5_IBUF)
     LUT6:I0->O            2   0.097   0.515  TW2/concatanate[3]_GND_3_o_AND_11_o1 (TW2/concatanate[3]_GND_3_o_AND_11_o)
     LUT3:I0->O            1   0.097   0.000  TW2/T_1_D (TW2/T_1_D)
     LD:D                     -0.028          TW2/T_1
    ----------------------------------------
    Total                      1.454ns (0.195ns logic, 1.259ns route)
                                       (13.4% logic, 86.6% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW2/W_0_G'
  Total number of paths / destination ports: 8 / 1
-------------------------------------------------------------------------
Offset:              1.299ns (Levels of Logic = 3)
  Source:            A<4> (PAD)
  Destination:       TW2/W_0 (LATCH)
  Destination Clock: TW2/W_0_G falling
  Data Path: A<4> to TW2/W_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             8   0.001   0.589  A_4_IBUF (A_4_IBUF)
     LUT4:I0->O            2   0.097   0.515  TW2/concatanate[3]_GND_3_o_AND_17_o1 (TW2/concatanate[3]_GND_3_o_AND_17_o)
     LUT3:I0->O            1   0.097   0.000  TW2/W_0_D (TW2/W_0_D)
     LD:D                     -0.028          TW2/W_0
    ----------------------------------------
    Total                      1.299ns (0.195ns logic, 1.104ns route)
                                       (15.0% logic, 85.0% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW2/W_1_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.444ns (Levels of Logic = 3)
  Source:            B<5> (PAD)
  Destination:       TW2/W_1 (LATCH)
  Destination Clock: TW2/W_1_G falling
  Data Path: B<5> to TW2/W_1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            12   0.001   0.734  B_5_IBUF (B_5_IBUF)
     LUT6:I1->O            2   0.097   0.515  TW2/concatanate[3]_GND_3_o_AND_15_o1 (TW2/concatanate[3]_GND_3_o_AND_15_o)
     LUT3:I0->O            1   0.097   0.000  TW2/W_1_D (TW2/W_1_D)
     LD:D                     -0.028          TW2/W_1
    ----------------------------------------
    Total                      1.444ns (0.195ns logic, 1.249ns route)
```

```
                                  (13.5% logic, 86.5% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW2/T_0_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.454ns (Levels of Logic = 3)
  Source:            A<5> (PAD)
  Destination:       TW2/T_0 (LATCH)
  Destination Clock: TW2/T_0_G falling
  Data Path: A<5> to TW2/T_0
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            12   0.001   0.744  A_5_IBUF (A_5_IBUF)
     LUT6:I0->O            2   0.097   0.515  TW2/concatanate[3]_GND_3_o_AND_13_o1 (TW2/concatanate[3]_GND_3_o_AND_13_o)
     LUT3:I0->O            1   0.097   0.000  TW2/T_0_D (TW2/T_0_D)
     LD:D                     -0.028          TW2/T_0
    ----------------------------------------
    Total                      1.454ns (0.195ns logic, 1.259ns route)
                                  (13.4% logic, 86.6% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW1/T_1_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.463ns (Levels of Logic = 3)
  Source:            A<3> (PAD)
  Destination:       TW1/T_1 (LATCH)
  Destination Clock: TW1/T_1_G falling
  Data Path: A<3> to TW1/T_1
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            14   0.001   0.753  A_3_IBUF (A_3_IBUF)
     LUT6:I0->O            2   0.097   0.515  TW1/concatanate[3]_GND_3_o_AND_11_o1 (TW1/concatanate[3]_GND_3_o_AND_11_o)
     LUT3:I0->O            1   0.097   0.000  TW1/T_1_D (TW1/T_1_D)
     LD:D                     -0.028          TW1/T_1
    ----------------------------------------
    Total                      1.463ns (0.195ns logic, 1.268ns route)
                                  (13.3% logic, 86.7% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW1/W_0_G'
  Total number of paths / destination ports: 8 / 1
-------------------------------------------------------------------------
Offset:              1.299ns (Levels of Logic = 3)
  Source:            A<2> (PAD)
  Destination:       TW1/W_0 (LATCH)
  Destination Clock: TW1/W_0_G falling
  Data Path: A<2> to TW1/W_0
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             8   0.001   0.589  A_2_IBUF (A_2_IBUF)
     LUT4:I0->O            2   0.097   0.515  TW1/concatanate[3]_GND_3_o_AND_17_o1 (TW1/concatanate[3]_GND_3_o_AND_17_o)
     LUT3:I0->O            1   0.097   0.000  TW1/W_0_D (TW1/W_0_D)
     LD:D                     -0.028          TW1/W_0
    ----------------------------------------
    Total                      1.299ns (0.195ns logic, 1.104ns route)
                                  (15.0% logic, 85.0% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW1/W_1_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.453ns (Levels of Logic = 3)
  Source:            B<3> (PAD)
  Destination:       TW1/W_1 (LATCH)
  Destination Clock: TW1/W_1_G falling
  Data Path: B<3> to TW1/W_1
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            14   0.001   0.743  B_3_IBUF (B_3_IBUF)
     LUT6:I1->O            2   0.097   0.515  TW1/concatanate[3]_GND_3_o_AND_15_o1 (TW1/concatanate[3]_GND_3_o_AND_15_o)
     LUT3:I0->O            1   0.097   0.000  TW1/W_1_D (TW1/W_1_D)
     LD:D                     -0.028          TW1/W_1
    ----------------------------------------
    Total                      1.453ns (0.195ns logic, 1.258ns route)
                                  (13.4% logic, 86.6% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW1/T_0_G'
  Total number of paths / destination ports: 12 / 1
-------------------------------------------------------------------------
Offset:              1.463ns (Levels of Logic = 3)
  Source:            A<3> (PAD)
  Destination:       TW1/T_0 (LATCH)
  Destination Clock: TW1/T_0_G falling
  Data Path: A<3> to TW1/T_0
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            14   0.001   0.753  A_3_IBUF (A_3_IBUF)
     LUT6:I0->O            2   0.097   0.515  TW1/concatanate[3]_GND_3_o_AND_13_o1 (TW1/concatanate[3]_GND_3_o_AND_13_o)
     LUT3:I0->O            1   0.097   0.000  TW1/T_0_D (TW1/T_0_D)
     LD:D                     -0.028          TW1/T_0
    ----------------------------------------
    Total                      1.463ns (0.195ns logic, 1.268ns route)
                                  (13.3% logic, 86.7% route)
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW0/T_1_G'
  Total number of paths / destination ports: 8 / 1
-------------------------------------------------------------------------
```

```
Offset:              1.317ns (Levels of Logic = 3)
  Source:            A<1> (PAD)
  Destination:       TW0/T_1 (LATCH)
  Destination Clock: TW0/T_1_G falling
  Data Path: A<1> to TW0/T_1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            12   0.001   0.607  A_1_IBUF (A_1_IBUF)
     LUT4:I0->O            2   0.097   0.515  TW0/concatanate[3]_GND_3_o_AND_11_o1 (TW0/concatanate[3]_GND_3_o_AND_11_o)
     LUT3:I0->O            1   0.097   0.000  TW0/T_1_D (TW0/T_1_D)
     LD:D                     -0.028          TW0/T_1
    ----------------------------------------
    Total                     1.317ns (0.195ns logic, 1.122ns route)
                                      (14.8% logic, 85.2% route)
==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW0/W_0_G'
  Total number of paths / destination ports: 16 / 2
--------------------------------------------------------------------------
Offset:              1.290ns (Levels of Logic = 3)
  Source:            B<0> (PAD)
  Destination:       TW0/W_0 (LATCH)
  Destination Clock: TW0/W_0_G falling
  Data Path: B<0> to TW0/W_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.579  B_0_IBUF (B_0_IBUF)
     LUT4:I0->O            2   0.097   0.515  TW0/concatanate[3]_GND_3_o_AND_15_o1 (TW0/concatanate[3]_GND_3_o_AND_15_o)
     LUT3:I0->O            2   0.097   0.000  TW0/W_0_D (TW0/W_0_D)
     LD:D                     -0.028          TW0/W_0
    ----------------------------------------
    Total                     1.290ns (0.195ns logic, 1.095ns route)
                                      (15.1% logic, 84.9% route)
==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'TW0/T_0_G'
  Total number of paths / destination ports: 8 / 1
--------------------------------------------------------------------------
Offset:              1.317ns (Levels of Logic = 3)
  Source:            A<1> (PAD)
  Destination:       TW0/T_0 (LATCH)
  Destination Clock: TW0/T_0_G falling
  Data Path: A<1> to TW0/T_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            12   0.001   0.607  A_1_IBUF (A_1_IBUF)
     LUT4:I0->O            2   0.097   0.515  TW0/concatanate[3]_GND_3_o_AND_13_o1 (TW0/concatanate[3]_GND_3_o_AND_13_o)
     LUT3:I0->O            1   0.097   0.000  TW0/T_0_D (TW0/T_0_D)
     LD:D                     -0.028          TW0/T_0
    ----------------------------------------
    Total                     1.317ns (0.195ns logic, 1.122ns route)
                                      (14.8% logic, 85.2% route)
==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW2/T_0_G'
  Total number of paths / destination ports: 2 / 2
--------------------------------------------------------------------------
Offset:              1.409ns (Levels of Logic = 2)
  Source:            TW2/T_0 (LATCH)
  Destination:       result<7> (PAD)
  Source Clock:      TW2/T_0_G falling
  Data Path: TW2/T_0 to result<7>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               2   0.472   0.561  TW2/T_0 (TW2/T_0)
     LUT4:I0->O            1   0.097   0.279  result<7>1 (result_7_OBUF)
     OBUF:I->O                 0.000          result_7_OBUF (result<7>)
    ----------------------------------------
    Total                     1.409ns (0.569ns logic, 0.840ns route)
                                      (40.4% logic, 59.6% route)
==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW2/T_1_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              1.360ns (Levels of Logic = 2)
  Source:            TW2/T_1 (LATCH)
  Destination:       result<7> (PAD)
  Source Clock:      TW2/T_1_G falling
  Data Path: TW2/T_1 to result<7>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.511  TW2/T_1 (TW2/T_1)
     LUT4:I1->O            1   0.097   0.279  result<7>1 (result_7_OBUF)
     OBUF:I->O                 0.000          result_7_OBUF (result<7>)
    ----------------------------------------
    Total                     1.360ns (0.569ns logic, 0.791ns route)
                                      (41.9% logic, 58.1% route)
==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW3/W_1_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              1.228ns (Levels of Logic = 2)
  Source:            TW3/W_1 (LATCH)
  Destination:       result<7> (PAD)
  Source Clock:      TW3/W_1_G falling
  Data Path: TW3/W_1 to result<7>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

```
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.379  TW3/W_1 (TW3/W_1)
     LUT4:I2->O            1   0.097   0.279  result<7>1 (result_7_OBUF)
     OBUF:I->O                 0.000          result_7_OBUF (result<7>)
    ----------------------------------------
    Total                      1.228ns (0.569ns logic, 0.659ns route)
                                       (46.4% logic, 53.6% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW3/W_0_G'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              1.148ns (Levels of Logic = 2)
  Source:            TW3/W_0 (LATCH)
  Destination:       result<7> (PAD)
  Source Clock:      TW3/W_0_G falling
  Data Path: TW3/W_0 to result<7>
                             Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               2   0.472   0.299  TW3/W_0 (TW3/W_0)
     LUT4:I3->O            1   0.097   0.279  result<7>1 (result_7_OBUF)
     OBUF:I->O                 0.000          result_7_OBUF (result<7>)
    ----------------------------------------
    Total                      1.148ns (0.569ns logic, 0.579ns route)
                                       (49.6% logic, 50.4% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW1/T_0_G'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              1.409ns (Levels of Logic = 2)
  Source:            TW1/T_0 (LATCH)
  Destination:       result<5> (PAD)
  Source Clock:      TW1/T_0_G falling
  Data Path: TW1/T_0 to result<5>
                             Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               2   0.472   0.561  TW1/T_0 (TW1/T_0)
     LUT4:I0->O            1   0.097   0.279  result<5>1 (result_5_OBUF)
     OBUF:I->O                 0.000          result_5_OBUF (result<5>)
    ----------------------------------------
    Total                      1.409ns (0.569ns logic, 0.840ns route)
                                       (40.4% logic, 59.6% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW1/T_1_G'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              1.360ns (Levels of Logic = 2)
  Source:            TW1/T_1 (LATCH)
  Destination:       result<5> (PAD)
  Source Clock:      TW1/T_1_G falling
  Data Path: TW1/T_1 to result<5>
                             Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.511  TW1/T_1 (TW1/T_1)
     LUT4:I1->O            1   0.097   0.279  result<5>1 (result_5_OBUF)
     OBUF:I->O                 0.000          result_5_OBUF (result<5>)
    ----------------------------------------
    Total                      1.360ns (0.569ns logic, 0.791ns route)
                                       (41.9% logic, 58.1% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW2/W_1_G'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              1.228ns (Levels of Logic = 2)
  Source:            TW2/W_1 (LATCH)
  Destination:       result<5> (PAD)
  Source Clock:      TW2/W_1_G falling
  Data Path: TW2/W_1 to result<5>
                             Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.379  TW2/W_1 (TW2/W_1)
     LUT4:I2->O            1   0.097   0.279  result<5>1 (result_5_OBUF)
     OBUF:I->O                 0.000          result_5_OBUF (result<5>)
    ----------------------------------------
    Total                      1.228ns (0.569ns logic, 0.659ns route)
                                       (46.4% logic, 53.6% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW2/W_0_G'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              1.148ns (Levels of Logic = 2)
  Source:            TW2/W_0 (LATCH)
  Destination:       result<5> (PAD)
  Source Clock:      TW2/W_0_G falling
  Data Path: TW2/W_0 to result<5>
                             Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               2   0.472   0.299  TW2/W_0 (TW2/W_0)
     LUT4:I3->O            1   0.097   0.279  result<5>1 (result_5_OBUF)
     OBUF:I->O                 0.000          result_5_OBUF (result<5>)
    ----------------------------------------
    Total                      1.148ns (0.569ns logic, 0.579ns route)
                                       (49.6% logic, 50.4% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW0/T_0_G'
  Total number of paths / destination ports: 2 / 2
```

```
--------------------------------------------------------------------------------
Offset:              1.409ns (Levels of Logic = 2)
  Source:            TW0/T_0 (LATCH)
  Destination:       result<3> (PAD)
  Source Clock:      TW0/T_0_G falling
  Data Path: TW0/T_0 to result<3>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               2   0.472   0.561  TW0/T_0 (TW0/T_0)
     LUT4:I0->O            1   0.097   0.279  result<3>1 (result_3_OBUF)
     OBUF:I->O                 0.000          result_3_OBUF (result<3>)
    ----------------------------------------
    Total                      1.409ns (0.569ns logic, 0.840ns route)
                               (40.4% logic, 59.6% route)
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW0/T_1_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:              1.360ns (Levels of Logic = 2)
  Source:            TW0/T_1 (LATCH)
  Destination:       result<3> (PAD)
  Source Clock:      TW0/T_1_G falling
  Data Path: TW0/T_1 to result<3>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.511  TW0/T_1 (TW0/T_1)
     LUT4:I1->O            1   0.097   0.279  result<3>1 (result_3_OBUF)
     OBUF:I->O                 0.000          result_3_OBUF (result<3>)
    ----------------------------------------
    Total                      1.360ns (0.569ns logic, 0.791ns route)
                               (41.9% logic, 58.1% route)
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW1/W_1_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:              1.228ns (Levels of Logic = 2)
  Source:            TW1/W_1 (LATCH)
  Destination:       result<3> (PAD)
  Source Clock:      TW1/W_1_G falling
  Data Path: TW1/W_1 to result<3>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.379  TW1/W_1 (TW1/W_1)
     LUT4:I2->O            1   0.097   0.279  result<3>1 (result_3_OBUF)
     OBUF:I->O                 0.000          result_3_OBUF (result<3>)
    ----------------------------------------
    Total                      1.228ns (0.569ns logic, 0.659ns route)
                               (46.4% logic, 53.6% route)
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW1/W_0_G'
  Total number of paths / destination ports: 2 / 2
--------------------------------------------------------------------------------
Offset:              1.148ns (Levels of Logic = 2)
  Source:            TW1/W_0 (LATCH)
  Destination:       result<3> (PAD)
  Source Clock:      TW1/W_0_G falling
  Data Path: TW1/W_0 to result<3>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               2   0.472   0.299  TW1/W_0 (TW1/W_0)
     LUT4:I3->O            1   0.097   0.279  result<3>1 (result_3_OBUF)
     OBUF:I->O                 0.000          result_3_OBUF (result<3>)
    ----------------------------------------
    Total                      1.148ns (0.569ns logic, 0.579ns route)
                               (49.6% logic, 50.4% route)
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW0/W_0_G'
  Total number of paths / destination ports: 2 / 2
--------------------------------------------------------------------------------
Offset:              0.751ns (Levels of Logic = 1)
  Source:            TW0/W_0_1 (LATCH)
  Destination:       result<1> (PAD)
  Source Clock:      TW0/W_0_G falling
  Data Path: TW0/W_0_1 to result<1>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.279  TW0/W_0_1 (TW0/W_0_1)
     OBUF:I->O                 0.000          result_1_OBUF (result<1>)
    ----------------------------------------
    Total                      0.751ns (0.472ns logic, 0.279ns route)
                               (62.8% logic, 37.2% route)
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'TW3/T_0_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:              0.751ns (Levels of Logic = 1)
  Source:            TW3/T_0 (LATCH)
  Destination:       carryout (PAD)
  Source Clock:      TW3/T_0_G falling
  Data Path: TW3/T_0 to carryout
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.279  TW3/T_0 (TW3/T_0)
     OBUF:I->O                 0.000          carryout_OBUF (carryout)
```

```
    ----------------------------------------
    Total                     0.751ns (0.472ns logic, 0.279ns route)
                                      (62.8% logic, 37.2% route)
=========================================================================
Cross Clock Domains Report:
--------------------------
=========================================================================
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 8.62 secs

-->
Total memory usage is 4625480 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :   13 (   0 filtered)
Number of infos    :    3 (   0 filtered)
```