Synthesis Report

Wed Apr 15 23:14:42 2020

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Release 14.7 - xst P.20131013 (nt64)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.09 secs

--> Reading design: CLA16.prj
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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "CLA16.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "CLA16"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : CLA16
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:/Users/ALI/Desktop/CLA (2).v" into library work
```

```
Parsing module .
Parsing module .
Parsing module .
Parsing module .
=========================================================================
*                           HDL Elaboration                             *
=========================================================================
Elaborating module .
Elaborating module .
Elaborating module .
WARNING:HDLCompiler:1127 - "C:/Users/ALI/Desktop/CLA (2).v" Line 25: Assignment to Cout ignored, since the identifier is never used
Elaborating module .
WARNING:HDLCompiler:1127 - "C:/Users/ALI/Desktop/CLA (2).v" Line 54: Assignment to P ignored, since the identifier is never used
=========================================================================
*                           HDL Synthesis                               *
=========================================================================
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/CLA (2).v".
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/CLA (2).v".
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/CLA (2).v".
INFO:Xst:3210 - "C:/Users/ALI/Desktop/CLA (2).v" line 25: Output port  of the instance  is unconnected or connected to loadless signal.
    Summary:
        no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:/Users/ALI/Desktop/CLA (2).v".
    Summary:
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Xors                                                  : 32
 1-bit xor2                                            : 32
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Xors                                                  : 32
 1-bit xor2                                            : 32
=========================================================================
=========================================================================
*                         Low Level Synthesis                           *
=========================================================================
Optimizing unit  ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block CLA16, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Found no macro
=========================================================================
=========================================================================
*                          Partition Report                             *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                           Design Summary                              *
=========================================================================
Top Level Output File Name         : CLA16.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 42
#      LUT3                        : 9
#      LUT4                        : 6
#      LUT5                        : 23
#      LUT6                        : 4
# IO Buffers                       : 52
#      IBUF                        : 33
#      OBUF                        : 19
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
Slice Logic Utilization:
 Number of Slice LUTs:                   42  out of  63400     0%
    Number used as Logic:                42  out of  63400     0%
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     42
   Number with an unused Flip Flop:      42  out of     42   100%
   Number with an unused LUT:             0  out of     42     0%
   Number of fully used LUT-FF pairs:     0  out of     42     0%
   Number of unique control sets:         0
IO Utilization:
 Number of IOs:                          52
 Number of bonded IOBs:                  52  out of    210    24%
```

```
Specific Feature Utilization:
-------------------------
Partition Resource Summary:
-------------------------
  No Partitions were found in this design.
-------------------------
=====================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
No clock signals found in this design
Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 3.920ns
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=====================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 621 / 19
---------------------------------------------------------------------
Delay:               3.920ns (Levels of Logic = 7)
  Source:            b<5> (PAD)
  Destination:       Cout (PAD)
  Data Path: b<5> to Cout
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   0.001   0.570  b_5_IBUF (b_5_IBUF)
     LUT4:I0->O            1   0.097   0.683  u1/CarryLogic/AG_int_SW0 (N4)
     LUT5:I0->O            5   0.097   0.702  u1/CarryLogic/AG_int (AG<1>)
     LUT5:I0->O            1   0.097   0.683  CarryLogic_2/AG_int_SW0 (N8)
     LUT6:I1->O            2   0.097   0.515  CarryLogic_2/AG_int (AG1_OBUF)
     LUT3:I0->O            1   0.097   0.279  CarryLogic_2/Cout1 (Cout_OBUF)
     OBUF:I->O                 0.000          Cout_OBUF (Cout)
    ----------------------------------------
    Total                      3.920ns (0.486ns logic, 3.434ns route)
                                       (12.4% logic, 87.6% route)
=====================================================================
Cross Clock Domains Report:
--------------------------
=====================================================================
Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.79 secs

-->
Total memory usage is 4625436 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :    2 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```