# Miniweather Application GPU Acceleration

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Differences between CPU and GPU Architecture

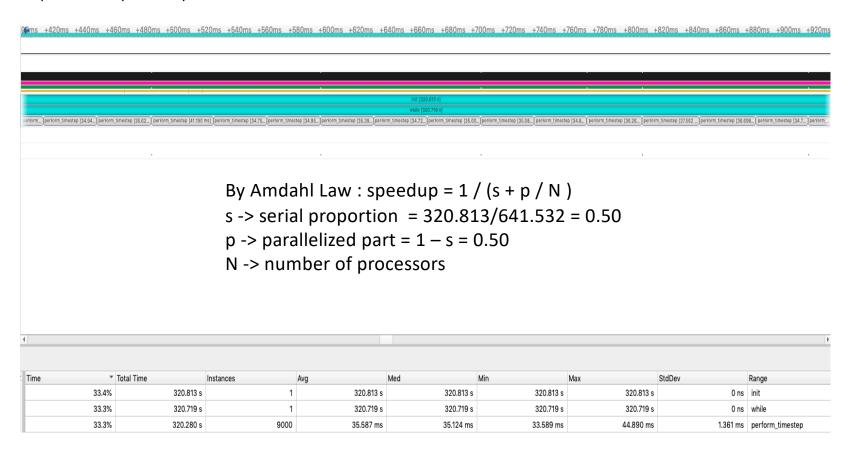
#### **CPU Architecture**

- Designed for Latency workloads
- Lower density of cores concentrations inside the CPU die
- Faster processors speed
- Large Main Memory Capacity and larges L2/L1 Caches
- Complex hardware with Branch Predictor
- Data Parallel Execution using SIMD AVX-512

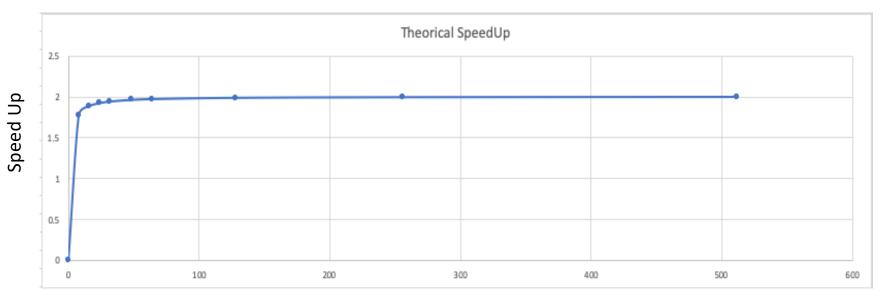
#### **NVIDIA GPU Architecture**

- Designed for high throughput workloads
- High density of cores concentrations inside the GPU die (thousands)
- Slower processors speed
- High Bandwidth Memory Access
- GPU Memory is not integrated in the Host and requires data transfer
- Data Parallel Execution using SIMT Warp Size 32

#### Expected speedup



Expected speedup



**Number of Processors** 

The expected speed up of MiniWeather application is limited to 2x no matter how many processors (N) are used to run the parallelized proportion.

Is the problem Memory Bound or Compute Bound?

The compute-to-global-memory-access-ratio allow us determine if the application in memory bound or compute bound

compute-to-global-memory-access-ratio = # floating point operations / memory access

The dominant kernel in the Miniweather application parallelized fraction is:

compute\_tendencies\_x

```
//Fourth-order-accurate interpolation of the state
vals[ll] = -stencil[0] / 12 + 7 * stencil[1] / 12 + 7 * stencil[2] / 12 - stencil[3] / 12;
//First-order-accurate interpolation of the third spatial derivative of the state (for artificial viscosity)
d3_vals[ll] = -stencil[0] + 3 * stencil[1] - 3 * stencil[2] + stencil[3];
```

stencil[] is a local array variable but it's value is first loaded from memory before usage

compute-to-global-memory-access-ratio for compute\_tendencies\_x kernel is 10/(4.0 \* 2) -> 1.25

## GPU Computing (V100)

Is the problem Memory Bound or Compute Bound?

Miniweather compute\_tendencies\_x

Compute-Global-Memory-Access-Ratio: 1.25

Applications uses Double precision

**NVIDIA GPU V100** 

Global Memory Bandwidth: 900 GB/s

Double Precision: 7 TFLOPS

Peak Compute-To-Global-Memory-Access-Ratio: 7.7

With a Compute-To-Global-Memory-Access-Ratio of 1.25 the kernel **compute\_tendencies\_x** throughput will be limited on how fast operands are fetched from memory. This make the dominant kernel **compute\_tendencies\_x** /application memory-bound. In fact the kernel when ported to GPU V100 will not achieve more than 112.5 GFLOPS.

#### Multicore Parallelization Results

Application	target	hardware	Time (s)	Speedup	
Serial		intel	307.842808		
OpenACC	multicore	Intel 8 cores	82.222548	3.74	

Using default values

nx\_glob, nz\_glob: 400 200 dx,dz: 50.000000 50.000000

dt: 0.166667

# Flags to Compile the Code

Application Code Sample

```
420
        #pragma acc parallel loop private(indt, indf1, indf2, inds)
        for (11 = 0; 11 < NUM VARS; 11++)
421
422
423
            #pragma acc loop vector collapse(2)
424
            for (k = 0; k < nz; k++)
425
426
                for (i = 0; i < nx; i++)
427
428
                     indt = 11 * nz * nx + k * nx + i;
429
                     indf1 = 11 * (nz + 1) * (nx + 1) + (k) * (nx + 1) + i;
                     indf2 = 11 * (nz + 1) * (nx + 1) + (k + 1) * (nx + 1) + i;
430
431
                     tend(indt) = -(flux[indf2] - flux[indf1]) / dz;
432
                     if (ll == ID WMOM)
433
                         inds = ID DENS * (nz + 2 * hs) * (nx + 2 * hs) + (k + hs) * (nx + 2 * hs) + i + hs;
434
435
                         tend[indt] = tend[indt] - state[inds] * grav;
436
437
438
439
```

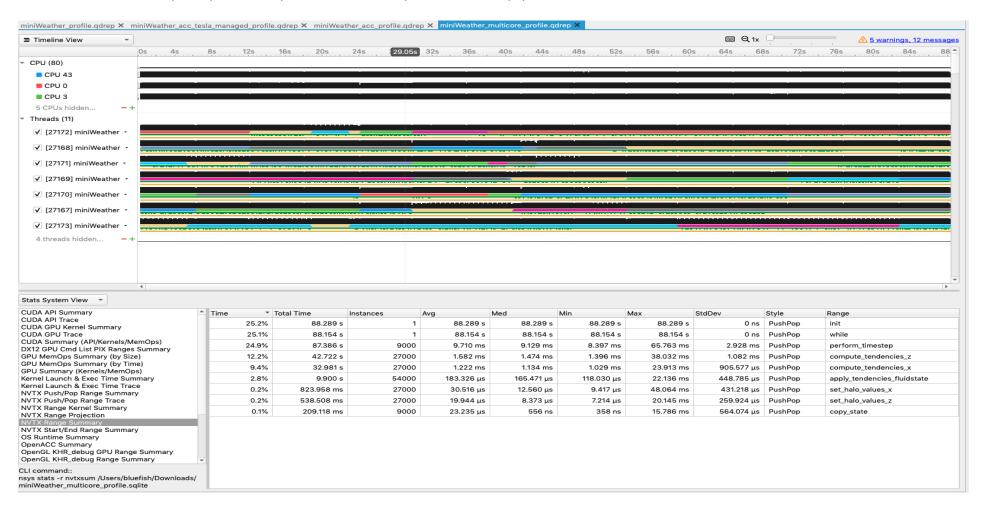
Application Code Sample Description

External loop in line 421 is parallelized and distributed among a gang of threads. This is done using the openacc directive #pragma acc parallel loop.

Variables that could be potentially shared by multiples threads are declared private and local to each thread in the gang. Line 420

Inner loops at line 424 and 426 are collapsed in one loop and vectorized.

Multicore nsys system profiler output and application timeline



#### **GPU Parallelization Results**

Application	target	hardware	Time (s)	Speedup	
Serial		intel	307.842808		
OpenACC	multicore	Intel 8 cores	82.222548	3.74	
OpenACC	tesla:managed	GPU V100	11.630973	26.46	
OpenACC	tesla	GPU V100	12.010639	25.63	

Using default values

nx\_glob, nz\_glob: 400 200 dx,dz: 50.000000 50.000000

dt: 0.166667

# Flags to Compile the Code

Data Optimization directives to minimize data transfer between host and device when not using managed memory. CUDA kernels don't need to wait for data transfer during their execution. Present clause using must of the time.

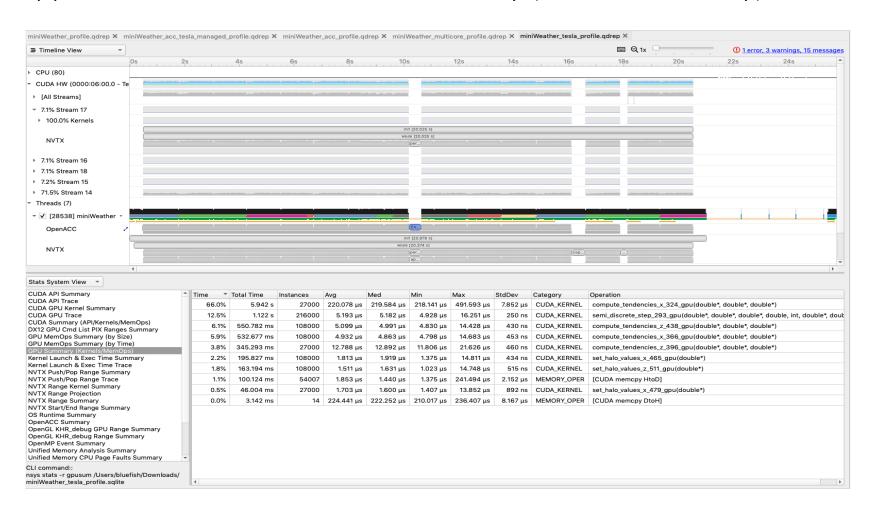
Parallel Loop optimizations and vector size adjusted to 32.

Variables that could potentially be shared among multiples threads are declared private and local to each thread in the gang.

Inner loops are collapsed in one loop and vectorized.

Independent Loop iterations are parallelized using asynchronous cuda streams.

Application Timeline and GPU summary (Kernels/Memory).



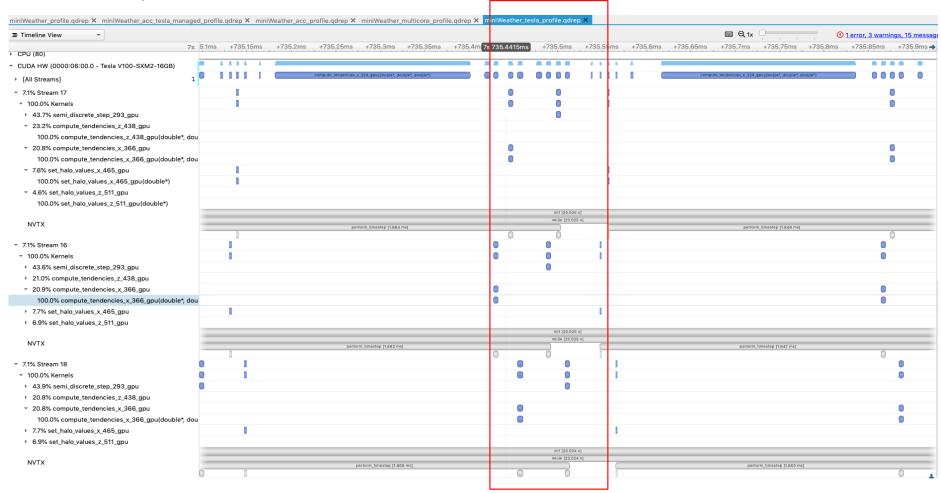
Private variables definition per thread to avoid race conditions

```
287
        //Apply the tendencies to the fluid state
        nvtxRangePushA("apply tendencies fluidstate");
288
                                                                                           Data already on device (present)
289
        for (11 = 0; 11 < NUM VARS; 11++)
290
291
292
            #pragma acc parallel loop collapse(2) private(indt, inds) present( state init[0:(nx + 2 * hs) * (nz + 2 * hs) * NUM VARS],
    state out[0:(nx + 2 * hs) * (n^2 + 2 * hs) * NUM VARS], tend[0:nx * nz * NUM VARS]) vector length(32) async(11)
            for (k = 0; k < nz; k++)
293
294
295
                for (i = 0; i < nx; i++)
296
                    inds = /11 * (nz + 2 * hs) * (nx + 2 * hs) + (k + hs) * (nx + 2 * hs) + i + hs;
297
298
                    indt \neq 11 * nz * nx + k * nx + i;
                    state out[inds] = state init[inds] + dt * tend[indt];
299
300
301
302
303
        #pragma acc wait
304
        nvtxRangePop();
305
306 }
                                       Independent loop iterations are parallelized using asynchronous CUDA
```

Parallel loop optimization collapse and vectorization

streams.

Example of Compiler messages.



Kernel compute\_tendencies\_x\_366\_gpu is launched across multiples streams

Data Optimization directives to minimize data transfer between host and device when not using managed memory. Creation of a data region

```
164
        nvtxRangePushA("while");
165
166
        #pragma acc data copyin(state[0:(nx + 2 * hs) * (nz + 2 * hs) * NUM VARS ], state tmp[0:(nx + 2 * hs) * (nz + 2 * hs) *
    NUM VARS ], flux[0:(nx + 1) * (nz + 1) * NUM VARS], tend[0:nx * nz * NUM VARS ], hy dens theta cell[0:nz + 2 * hs],
    hy_pressure_int[0:nz + 1], hy_dens_cell[0:nz + 2 * hs])
167
            while (etime < sim_time)
168
169
170
                //If the time step leads to exceeding the simulation time, shorten it for the last step
171
                if (etime + dt > sim time)
172
                                                                                                         Must of data is copied to the gpu only once
173
                    dt = sim time - etime;
174
175
176
                //Perform a single time step
177
                nvtxRangePushA("perform_timestep");
178
                perform timestep(state, state tmp, flux, tend, dt);
179
                nvtxRangePop();
180
181
                //Inform the user
182
183
                printf("Elapsed Time: %lf / %lf\n", etime, sim time);
                                                                                                                                Dominant DtoH memory transfers
184
185
                //Update the elapsed time and output counter
186
                etime = etime + dt;
187
                output_counter = output_counter + dt;
188
                //If it's time for output, reset the counter, and do output
189
190
                nvtxRangePushA("copy state");
191
                if (output counter >= output freq)
192
193
                    output_counter = output_counter - output_freq;
194
195
                    #pragma acc update self(state[: (nx+2*hs) * (nz+2*hs) * NUM_VARS ])
196
                    output(state, etime);
197
198
                nvtxRangePop();
199
200
```

201

Data Optimization directives to minimize data transfer between host and device when not using managed memory.

Time	*	Total Time	Count		Avg		Med	М	fin	Max	StdDev	Operation	
	97.0%	100.124 m	3	54007	1.853 µs		1.440 µs		1.375 µs	241.494 μs	2.152 μs	[CUDA memcpy HtoD]	
	3.0%	3.142 m	6	14	224	.441 µs	222.252	μs	210.017 μs	236.407 μs	8.167 μs	[CUDA memcpy DtoH]	
Total		▼ Count		Avg		Med		Min		Max	StdDev		Operation
	92.75	MiB	54007		1.76 KiB		1.57 KiB		1.57 KiB	2.52 M	iB 2	1.87 KiB	[CUDA memcpy HtoD]
	35.21	MiB	14		2.52 MiB		2.52 MiB		2.52 MiB	2.52 M	iB	0 B	[CUDA memcpy DtoH]

Must of the memory transfer occurred when data generated in the device was copied to variable state

#### Code available at:

<a href="https://github.com/mahsanchez/mw\_openacc/blob/main/miniweather\_openacc.cpp">https://github.com/mahsanchez/mw\_openacc/blob/main/miniweather\_openacc.cpp</a>

https://github.com/mahsanchez/mw\_openacc/blob/main/miniweather\_multicore.cpp