# L1 Cache Block Size Simulation

Definition: During the lecture, we studied caches. In this homework, you are asked to simulate L1 block size in a hardware simulator and measure its effect on L1 cache hit rate for the matrix multiplication benchmark. The average L1 hit rate is defined as the ratio of the memory operations which hit in L1 cache.

For this task, you need to use gem5 simulators.

Gem5 is a full system simulator and you can simulate Alpha, ARM, SPARC, MIPS, POWER, RISC-V and x86 ISAs. For this homework, it is enough for you to simulate X86 ISA so that you can compile matrix multiplication application in your host computer.

Although ge5 supports a full system (meaning all the disk access operations and the operating system) you are suggested to use only the standard edition (i.e. referenced as SE).

You can see the link below.

<http://gem5.org/Main_Page>

The simulator is working on the linux/unix environment and most probably Windows is not supported in it. For the installation, you can start from the following page: <http://gem5.org/Introduction>

Submission:

* You need to simulate 64KB L1 Instruction Cache and 64KB L1 Data cache for this homework. As the benchmark application you need to use Matrix Multiplication (i.e. Matmul) that you already have used for the second homework. You need to repeat the simulation for different block sizes of L1 caches and measure the hit rate for both L1 Data and L1 Instruction caches. Finally, you need to put those hit rates in a table and draw the hit rate vs block size graph for both caches.
* For the submission, in a report you are asked to fill the following information
  + Which files in the simulator you mainly changed?
  + What is the main code you added into the simulator (not all the lines, just your main change is enough)
  + Tables showing the L1 hit rate for different block sizes for both data and instruction caches
  + Graphs showing the changes in the hit rate according to the block size for both data and instruction caches.