Experiment 1 - Clock and Periodic Signal Generation

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***Abstract*:** This experiment taught us how to generate clock and the advantages and disadvantages of each way. Also, we learned how to work with the 7400 IC series.

***Keywords*:** *clock generation - digital logic gates – counter – frequency divider – duty cycle – IC*

Introduction

This experiment introduced participants to digital logic gates' static characteristics, delay times, clock frequency generation, and digital system design using schematic diagrams. It covered tools like power supply, function generator, and oscilloscope, along with concepts such as 74 Series Basic Logic Gates, oscillator circuits (including the LM555 timer IC and Schmitt trigger oscillator), and sequential circuits with clocks and counters. Through hands-on exploration and theory, participants gained insights into digital electronics and system design principles.

I. Experiments

A. Ring Oscillator

74HCT04 is an IC that has 6 inverters inside and by connecting an odd number of inverters together the output of each inverter will oscillate.

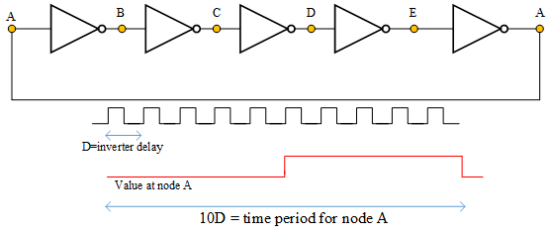

Figure 1: Ring Oscillator Circuit

By connecting 5 terminals of the IC (5 inverters) we will have a ring oscillator with a frequency of about 18.72 MHz (as shown below).

Figure 2: Ring Oscillator Output

We know that $T_{ring\ oscillator}=2ND$ where N is the number of the inverters used and D is the delay of each inverter. Thereby we can see T=53.42ns.

Using the ring oscillator period time formula, we can have the delay of a single inverter:

$T_{ring\ oscillator}$ = 2ND
D: $Inverter\ delay$
53.42 ns=2*5* $D \rightarrow$ D $\simeq$ 5 ns

B. LM555 Timer

This IC operates in three modes: Monostable, Bistable and Astable. And can be used for generating clock signal or delays. In Astable mode it operates as an oscillator and in this experiment, we will use Astable mode. This allows the timer to operate as an oscillator that outputs a continuous rectangular pulse of a required frequency.

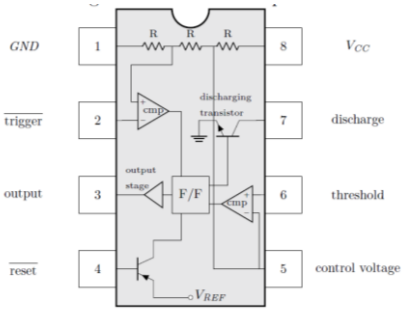

Figure 3: LM555 timer pin-out

At first capacitors are not charged and VCC is not connected. Then as when we start, C1 starts to charge through R_1+ R_2. In this state the FF reset to 0, Then output is 1 (duo to inverter at FF output). When C1 charges until %66 of VCC, FF sets to 1 and output is 0 (because of the resistance dividing on top of the circuit). C1 discharges through R_2. When the charge period is more than discharge period we will have a duty cycle above %50.

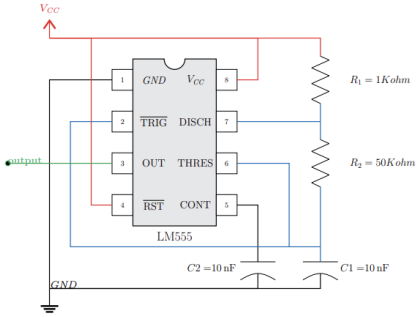

Figure 4: LM555 in Astable Mode

We changed R_2 resistor to observe how frequency and duty cycle changes.

1. R_2 = 1 KΩ

Figure 5: LMM555 Output Waveform with 1KΩ Resistor

Based on the observation:
f = 46.07KHz, T = 21.7us, T_1=13.8us
Duty Cycle = T_1/T=13.8/21.7= 64%
Theoretical:
T = 0.693 * (1 + 2) *10^3 * 10*10^-9 = 20.79us
Duty Cycle = 2/3 = 66.6%

2. R_2 = 10 KΩ

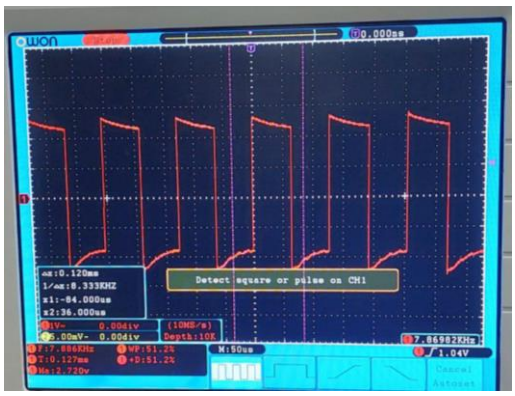

Figure 6: LMM555 Output Waveform with 10KΩ Resistor

Based on the observation:
f = 7.87KHz, T = 127.1us, T_1=64.5us
Duty Cycle = T_1/T=64.5/127= 51%
Theoretical:
T = 0.693 * (1 + 20) *10^3 * 10*10^-9 = 145.5us
Duty Cycle = 11/21 = 52.3%

3. R_2 = 100 KΩ

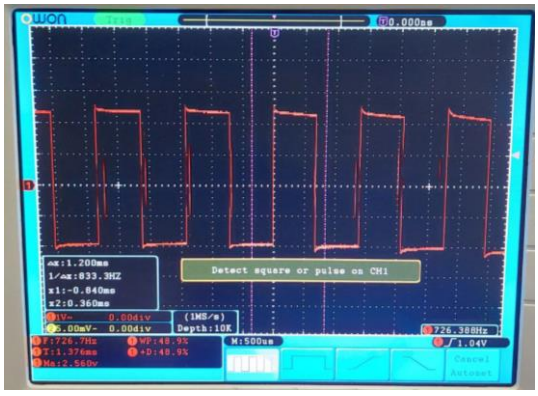

Figure 7: LMM555 Output Waveform with 100KΩ Resistor

Based on the observation:
f = 726.39Hz, T = 1377us, T_1=688us
Duty Cycle = T_1/T=688/1377= 50%
Theoretical:
T = 0.693 * (1 + 400) *10^3 * 10*10^-9 = 2.78ms
Duty Cycle = 201/401 = 50.1%

As we experimented, increasing the value of resistor R_2 resulted in a decrease in the frequency of the output waveform. Moreover, utilizing the LM555 timer, the default resistance value for R_1 in this setup stands at 1 KΩ, thus preventing the attainment of a perfect 50% duty cycle. However, by significantly exceeding the value of R_1 with R_2, we got close to approach this ideal duty cycle.

C. *Schmitt Triger Oscillator*

By using one inverter of 74HCT14, we made a Schmitt Trigger Oscillator. If we connect the output and the input of the Schmitt trigger by a resistor and its input to the ground, using a capacitor, the output will oscillate.

Let's consider the capacitor has no charge at first. Vin should be zero and $Vout$ must be equal to Vcc. Then the capacitor starts to charge until its voltage becomes $VTh+$. At this point $Vout$ will become zero and the capacitor starts to discharge. It will continue till its charge gets to $VTh-$. This process would repeat and repeat and as we expected, we'll see a square wave at $Vout$.

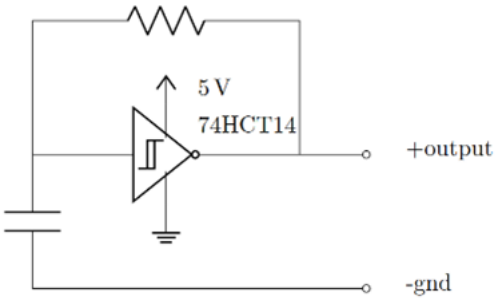

Figure 8: Schmitt Inventor Oscillator Circuit

In the Schmitt inverter oscillator, f = α/RC, where α is a constant. This circuit works by charging and discharging a capacitor. When the time constant (τ) is higher, it takes more time for the circuit to complete one oscillation cycle.

We changed R resistor to observe how frequency and duty cycle changes.

1. R = 470 Ω

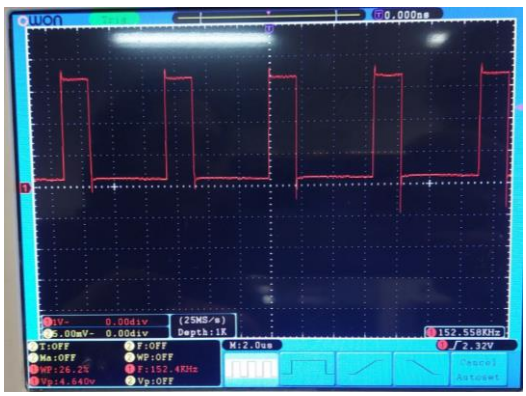

Figure 9: Schmitt Triger Output Waveform with 470Ω Resistor

Based on our observation:
f = 152.558 KHz
α = R*C*f = 0.71

2. R = 1 KΩ

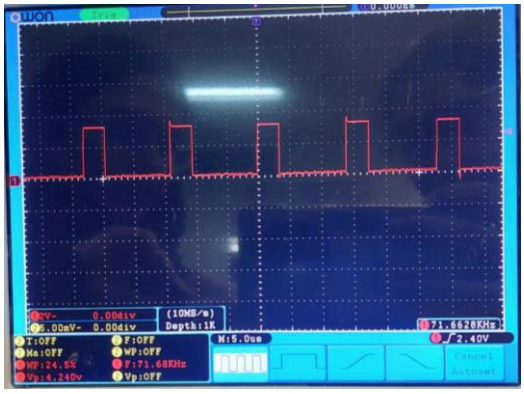

Figure 10: Schmitt Triger Output Waveform with 1 KΩ Resistor

Based on our observation:
f = 71.662 KHz
α = R*C*f = 0.72

3. R = 2.2 KΩ

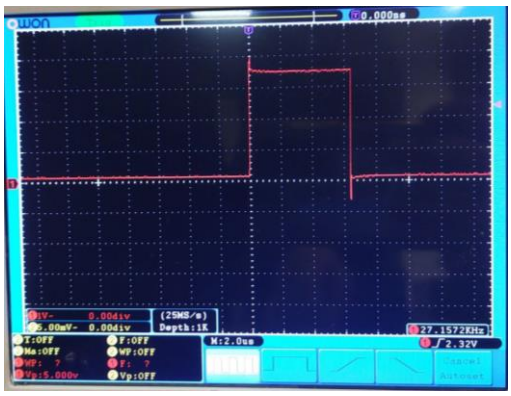

Figure 11: Schmitt Trigger Output Waveform with 2.2 KΩ Resistor

Based on our observation:
f = 27.157 KHz
α = R*C*f = 0.6

The average α is about 0.67.

D. Synchronous Counter as a Frequency Divider

To build this counter first, we should decide how many clock cycles we want and by that, we choose the number of 4-bit counters that in this case we had two of them so the maximum value could reach 256 (2^8).

To divide the frequency by 200 we should have 256-200=56 which is 00111000 on the parallel input of the IC. After that, we needed a primary initialization, so we added an AND gate (74HC08) to the load pin to have a preset pin.

To have the 8 bits together we had to connect the carry-out pin of the LSB IC to the input of MSB to have them both load together.

As we saw in the first part, the frequency of the Ring Oscillator was about 18.72MHz. The output frequency is about 70.18KHz. As we expected the frequency was divided by 200 (somehow different because of the circuit disturbance and oscilloscope accuracy.) So, this is a better device to generate lower frequency clock cycles.

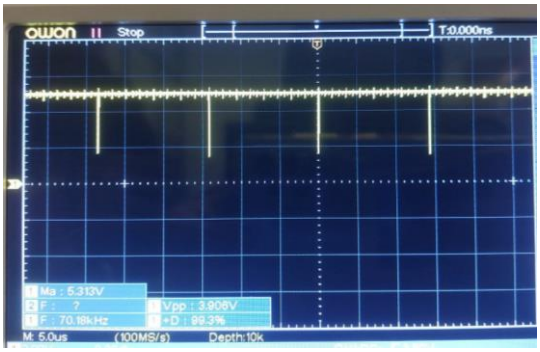

Figure 12: Waveform of Carry-Out Pin of the MSB Counter

E. T Flip-Flop

So we had to change a D flip-flop to a T flip-flop by removing the set and reset and connecting data input to q output we would have a T flip-flop.

Furthermore, if we connect the frequency divider output to the T flip-flop we built, we will have a 50% duty cycle in the output.

Using a 74HC74 and wire pin2 and pin6 we will have TFF operation via DFF. At the positive edge of the clock, the Q1bar toggles until the next edge. Therefore, we have a %50 duty cycle at the output.

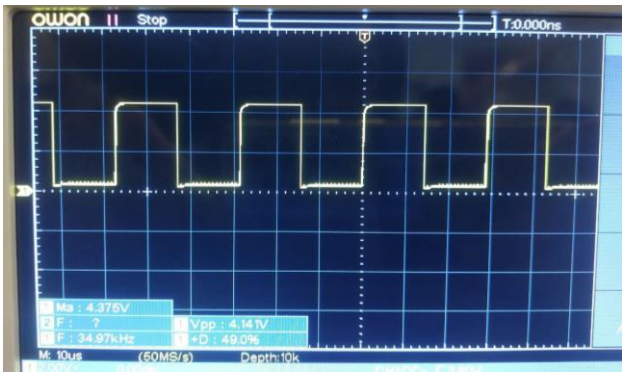

Figure 13: TFF Output with 50% Duty Cycle

Using a TFF will reduce the frequency up to 50% from 70.18 KHz to 34.97KHz.
Compared with the Ring Osc., the frequency which was 18.7KHz, has been doubled.

F. References

[1] Katayoon Basharkhah and Zahra Jahanpeima and Prof. Zain Navabi, *Digital Logic Laboratory*, University of Tehran, Spring 1403.