James Madison University

Information Technology Program

**IT 212: Digital Electronics**

**Instructor:** Ahmad A. Salman

**Class:**

TT 1:00 – 2:15 PM

**Class Location:**

EnGeo 2209

**Lab Location:**

EnGeo 009

**Phone:** (540) 568 - 7751

**Office Hours:**

Wednesdays 11:00 AM – 1:00 PM

**E-mail:** [salmanaa@jmu.edu](mailto:salmanaa@jmu.edu)

**Prerequisite:** Grade of C or better in MATH 220, MATH 112 or permission from instructor

**Course Materials:** Fundamentals of Digital Logic with VHDL Design, 3rd Edition by Stephen Brown and Zvonko Vranesic

ISBN-13:

978-0-07-722143-0

Course Description

Introduces digital systems, circuits, and computers. Topics include binary systems and codes, digital logic gates and circuits, microelectronics and integrated circuits, coding and multiplexing, multivibrators, shift registers, counters, A/D converters, and elementary computer architecture.

Learning Objectives

Students who successfully complete this course will achieve the following learning objectives:

* Student will be able to analyze combinational logic circuits.
* Student will be able to minimize Boolean expressions using Boolean algebra and Karnaugh maps.
* Student will be able to specify a Boolean expression in either of the standard forms, and design the associated two-level combinational logic circuits.
* Student will be able to design a minimum-cost combinational logic circuit, given the circuit specifications. Student will be able to design complex digital logic circuits and systems from simple logic circuits.
* Student will be able to design a 1-bit adder circuit.
* Student will be able to design a multiple-bit adder/subtractor circuit.
* Student will be able to analyze sequential logic circuits.
* Student will be able to design a 1-bit memory element from basic logic gates.
* Student will be able to design registers and shift-registers from 1-bit memory elements.
* Student will be able to design counters from 1-bit memory elements.
* Student will be able to design a minimum-cost sequential logic circuit, given the circuit specifications.

Laboratory

Lab Policy

The laboratory experiments complement the material covered in the lectures and in the assigned readings. They focus on the historical design methodology, making use of discrete components, a breadboard, and circuit wiring to realize combinational and sequential logic circuits. Each experiment will provide hands-on experience with one or more of the concepts covered in class. The labs will be performed in-person using lab components in EnGeo 0009 and using EasyEDA online tool https://easyeda.com/

You are expected to be prepared for each lab. This includes review of the associated lecture materials, completion of the associated reading, and, most importantly, completion of the pre-lab. You will NOT be allowed to participate in the lab unless you have completed the pre-lab.

You will be expected to complete a lab report for each laboratory experiment.

The laboratory experiments are administered by the instructor who will provide additional materials regarding the lab, including the lab schedule, pre-lab requirements, and lab report guidelines.

**Failure to complete all of the laboratory experiments will result in a failing grade for the course.**

Labs

Lab 1: Gates

Lab 2: Combinational Logic 1

Lab 3: Combinational Logic 2

Lab 4: Adder

Lab 5: BCD

Lab 6: Multiplexers

Lab 7: Flip-Flops

Lab 8: Counters

Homework

Homework is an essential part of the learning process. It is your opportunity to make use of the concepts discussed in class and in the assigned reading, and to apply these concepts to various types of problems. It will help you identify those things that you do not understand, and help you prepare for the exams.

You are expected to complete the assigned reading and ALL of the problems in the problem set on each homework assignment. You are encouraged to work together, to understand how to solve each of the problems, and to develop a more complete understanding of the material. However, you must submit your own work. If you copy someone else's work or allow others to copy your work, you will receive a 0 for the homework assignment.

Homework assignments will be posted on Canvas, on a weekly basis. You will have one week to complete each assignment. Homework MUST be submitted by the indicated due date on Canvas in electronic format. You can write your homework using any tool such as Microsoft word or do it on paper and then convert it to electronic form by taking clear images of it. Whichever method you choose, make sure to convert your homework to a single PDF file before submitting it to blackboard. Failure to submit a single PDF file for your homework assignment will result in point deductions up to losing all the points for a homework assignment if it is a repeated incident. **Late homework will NOT be accepted.**

The lowest homework grade will be dropped at the end of the semester.

Homework solutions should be formatted as follows:

1. Your name should appear at the top-left on all pages of your solutions.

2. The class number (ie. IT212-0001) and the assignment number should appear below your name.

3. All pages should be numbered at the top-right.

4. All solutions should be written neatly and clearly – if we cannot read it we will not grade it!

5. Solutions to individual problems should be clearly separated – you should either use a horizontal line to separate problem solutions or you should start the solution to a problem on a new page.

**Failure to follow the above guidelines will result in points deduction up to getting a 0 on the assignment!**

Assignments

Homework 1

Homework 2

Homework 3

Homework 4

Homework 5

Homework 6

Homework 7

Homework 8

Exam

See the detailed schedule for the date of each of the exams.

All exams are **closed book**. I will provide the necessary reference materials for each exam.

Use of **calculators** will be specified for each exam.

There will be NO makeup exams. If you cannot make one of the scheduled exams, you must speak with me **in advance** to arrange for an alternate time to take the exam.

Exams

• Midterm #1

• Midterm #2

• Final Exam

Attendance

Attendance is mandatory. You cannot receive credit for in-class exercises if you are absent from class. You are responsible for all material covered in class and in the assigned reading. The class meets twice a week through in either the lab or the classroom (check the schedule for the specific dates). Should you miss class, you must con-sult with one of your classmates to obtain the missed material. If you miss more than 3 classes, you will receive a zero for attendance. Any further absences will result in further point deduction from the overall course points.

Special circumstances and illness will be dealt with on individual basis.

Grading

The final grade for the course is based on my best assessment of your understanding of the material and your participation in the class during the semester. The exams, homework assignments, and in-class exercises will be used to determine your preliminary final grade according to the following weighting:

Attendance/Exercises 5%

Homework 15%

Lab Experiments 15%

Midterm #1 20%

Midterm #2 20%

Final 25%

Disability Services

If you are a student with a documented disability who will be requesting accommodations in my class, please make sure you are registered with JMU’s Office of Disability Services (www.jmu.edu/ods/, 107 Wilson Hall, 568-6705) and provide me with an Access Plan letter outlining your accommodations. I will be glad to meet with you privately during my office hours to discuss your special needs.

Honor Code

You are expected to abide by both the JMU Honor Code and the JMU Appropriate Use of

Information Technology Resources Policy. Please familiarize yourself with these documents. JMU’s Honor Code prohibits unauthorized sharing and use of electronic or printed material. Others’ work used in relation to your Project must be properly cited. Citation assistance is available from the Library and from JMU’s Writing Center. Protect your work – knowingly

providing access to your work and unauthorized use of another person’s work are both violations of the JMU Honor Code.

A JMU degree is a valuable commodity. Please don’t diminish the value of your degree by participating in or ignoring others’ dishonest actions. Use good judgment and insist that others do the same. I will gladly answer questions you have about applying the Honor Code, Appropriate Use Policy, and Academic Honesty to this course.

Do NOT cheat -- I will take appropriate action if I detect any instances of unauthorized collaboration or assistance. At a minimum this will result in a report to the JMU Honor Council and a reduction in your course grade.

Lecture Schedule

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Date** | **Lecture** | **Lab** | | **Topic** | **Reading** | **HW** | **HW Due** | **Lab Due** |
| 01/19 | 1 |  | Course overview and Introduction | | 1.1 – 1.5 | 1 |  |  |
| 01/21 | 2 |  | Number Systems | | 1.6, 5.1 | 2 |  |  |
| 01/26 | 3 |  | Combinational Logic Circuits I | | 2.1 – 2.5 |  |  |  |
| 01/28 | 4 |  | Combinational Logic Circuits II | | 2.6 – 2.8 |  | 1 |  |
| 02/02 |  | 1 | Lab #1: Gates | |  | 3 |  |  |
| 02/04 | 5 |  | Circuit Design (Examples) | | 2.1 – 2.8 |  | 2 |  |
| 02/09 |  |  | **Assessment Day (No Class)** | |  |  |  | 1 |
| 02/11 |  | 2 | Lab #2: Combinational Logic 1 | |  |  |  |  |
| 02/16 | 6 |  | Karnaugh Maps I | | 4.1 – 4.2 | 4 | 3 |  |
| 02/18 | 7 |  | Karnaugh Maps II | | 4.3 – 4.4 |  |  | 2 |
| 02/23 |  | 3 | Lab #3: Combinational Logic 2 | |  |  | 4 |  |
| 02/25 |  |  | **Midterm Exam #1: Lectures 1 – 7** | |  |  |  |  |
| 03/02 | 8 |  | Binary Arithmetic | | 5.1 – 5.3, 5.7 – 5.8 | 5 |  | 3 |
| 03/04 | 9 |  | Arithmetic Circuits I | | 5.2 – 5.3, 5.5; Appx. A |  |  |  |
| 03/09 |  | 4 | Lab #4: Adder | |  |  | 5 |  |
| 03/11 | 10 |  | Multiplexers | | 6.1, 6.6; Appx. A | 6 |  |  |
| 03/16 | 11 |  | Decoders and Encoders | | 6.2 – 6.4, 6.6, Appx. A |  |  | 4 |
| 03/18 |  | 5 | Lab #5: BCD | |  |  | 6 |  |
| 03/23 | 12 |  | One-bit Memory Elements I | | 7.1 – 7.4, Appx. A | 7 |  |  |
| 03/25 | 13 |  | Registers | | 7.8, 7.13, 7.14, 10.1 |  |  | 5 |
| 03/30 |  | 6 | Lab #6: Multiplexers | |  |  |  |  |
| 04/01 | 14 |  | Midterm Review #2 | |  |  | 7 |  |
| 04/06 |  |  | **Midterm Exam #2: Lectures 9 – 17** | |  |  |  |  |
| 04/08 |  |  | **Break Day #3 (No Class)** | |  |  |  |  |
| 04/13 | 15 |  | Sequential Logic Circuits I | | 8.1, 8.9, 7.15 | 8 |  | 6 |
| 04/15 | 16 |  | Sequential Logic Circuits II | | 7.9 – 7.11, 8.7, 7.13 |  |  |  |
| 04/20 |  | 7 | Lab #7: Flip-Flops | |  |  | 8 |  |
| 04/22 | 17 |  | Sequential Logic Circuits III | | 8.1– 8.2, 8.6, 8.5.2, 8.11 |  |  |  |
| 04/27 |  | 8 | Lab #8: Counters | |  |  |  | 7 |
| 04/29 | 18 |  | Final Exam Review | |  |  |  | 8 |
| **05/04** |  |  | **Final Exam: 10:30 am – 12:30 pm** | |  |  |  |  |