BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI - K. K. BIRLA GOA CAMPUS

DIGITAL DESIGN MODELSIM EXECUTION STEPS

Step 1 : Open Modelsim

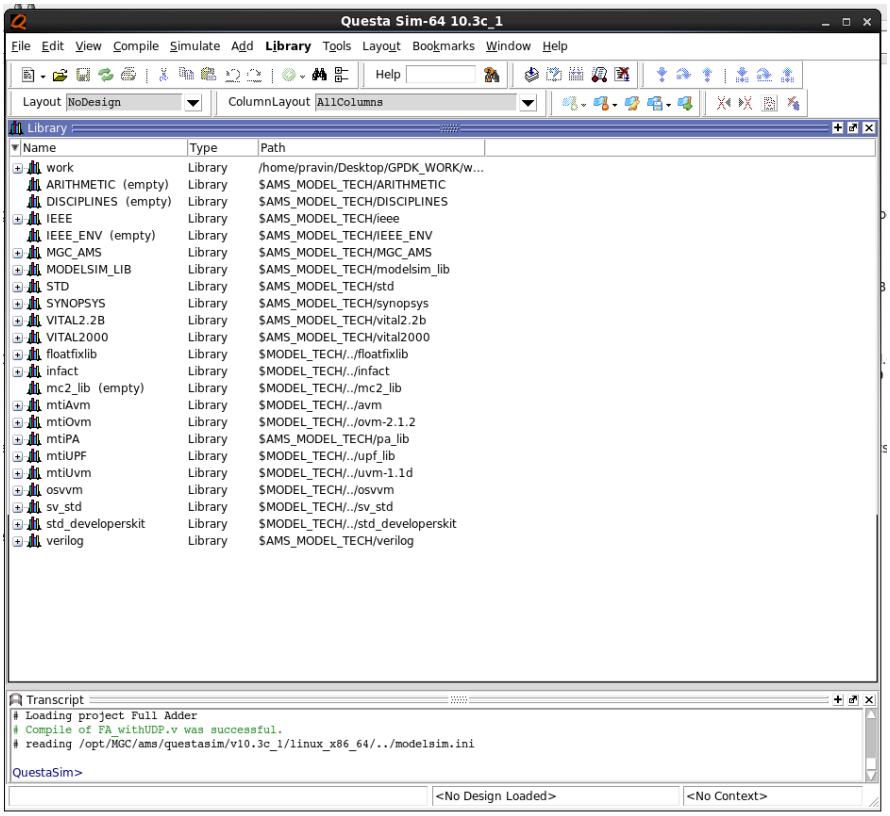

Figure 1: Modelsim interface

Step 2 : Click on **File →New →Project**

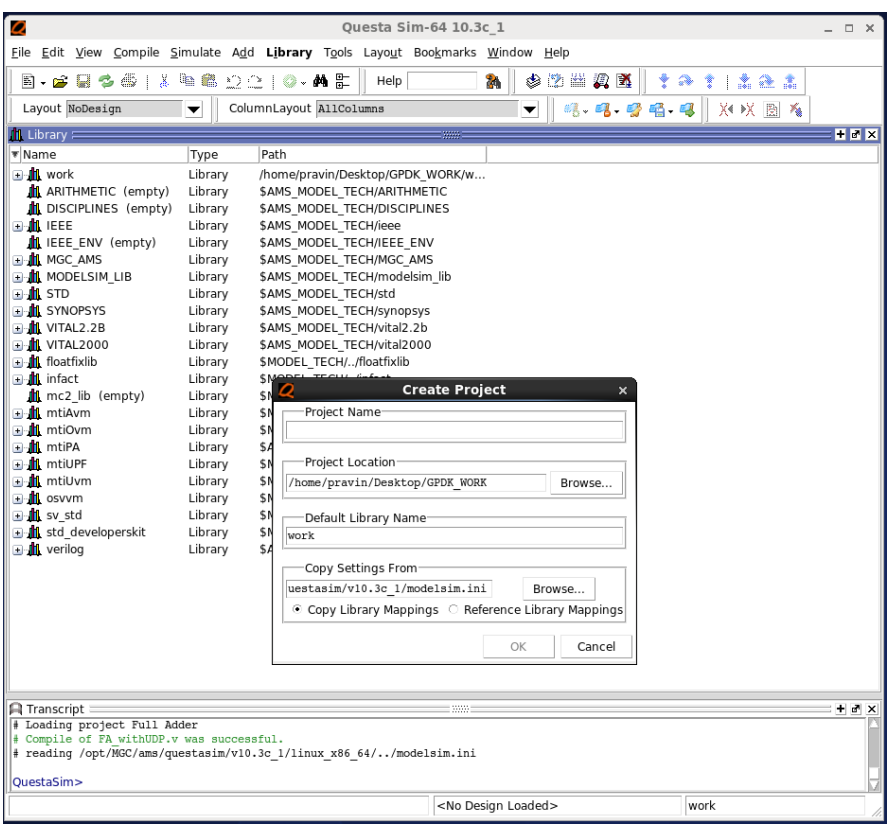

Figure 2: Modelsim new project

Step 3 : Enter **Project Name** and click **OK**

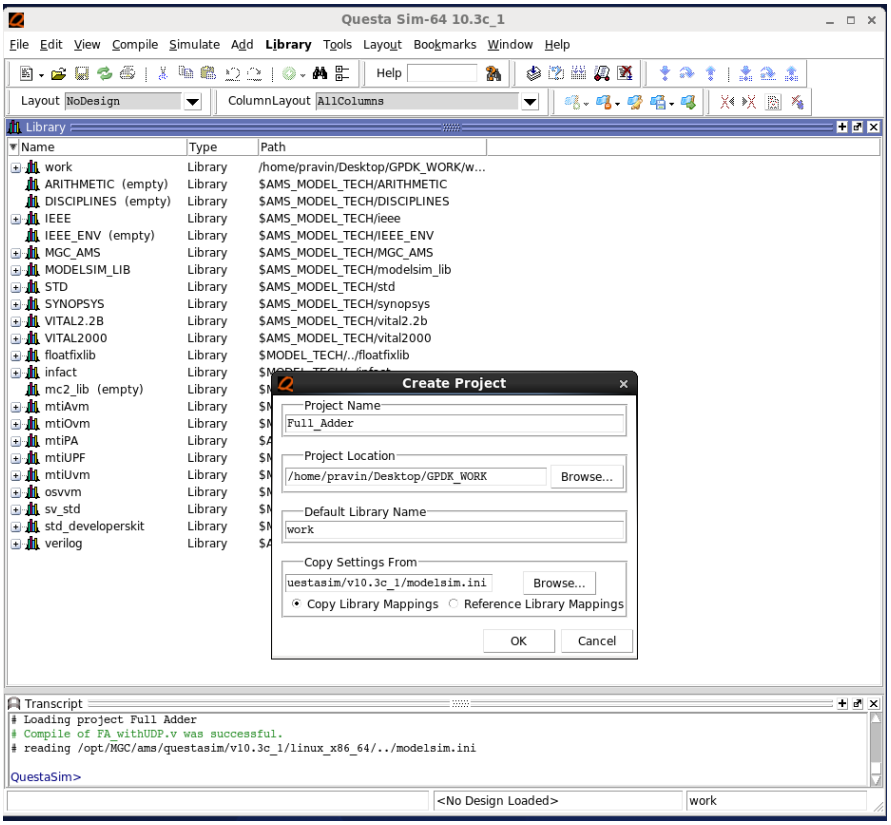

Figure 3: Modelsim project name

Step 4 : Add items to Project window will be automatically opened. Click on **Create New File**

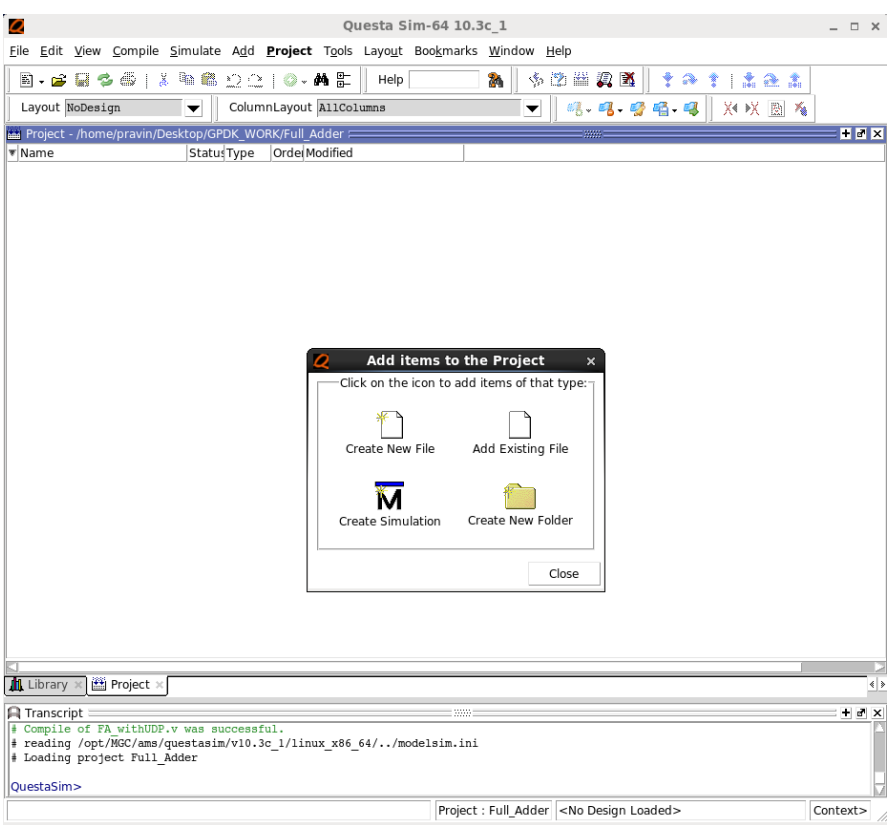

Figure 4: Modelsim Create New File

Step 5 : Create Project File window will be automatically opened. Enter **File Name**, select **Add file as type** as **verilog** and click **OK**

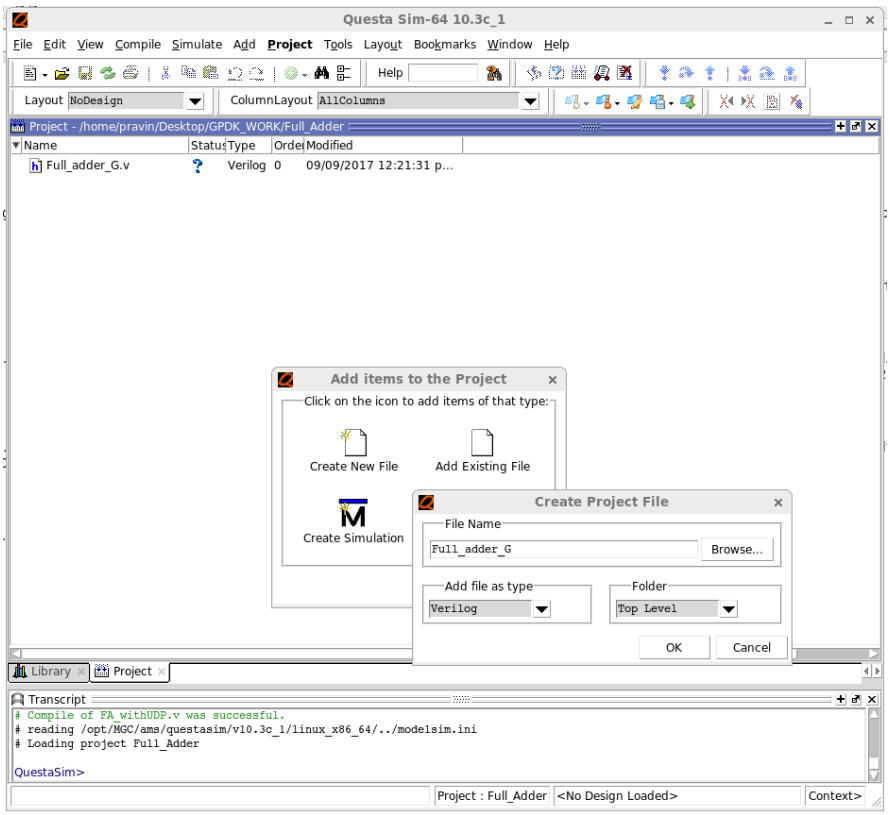

Figure 5: Modelsim Create Project File

Note : If **Add items to Project** window is not opened automatically, click on project tab, right click in project window area, click on **Add to project file** →**New File...** and then add the details as mentioned in step 5.

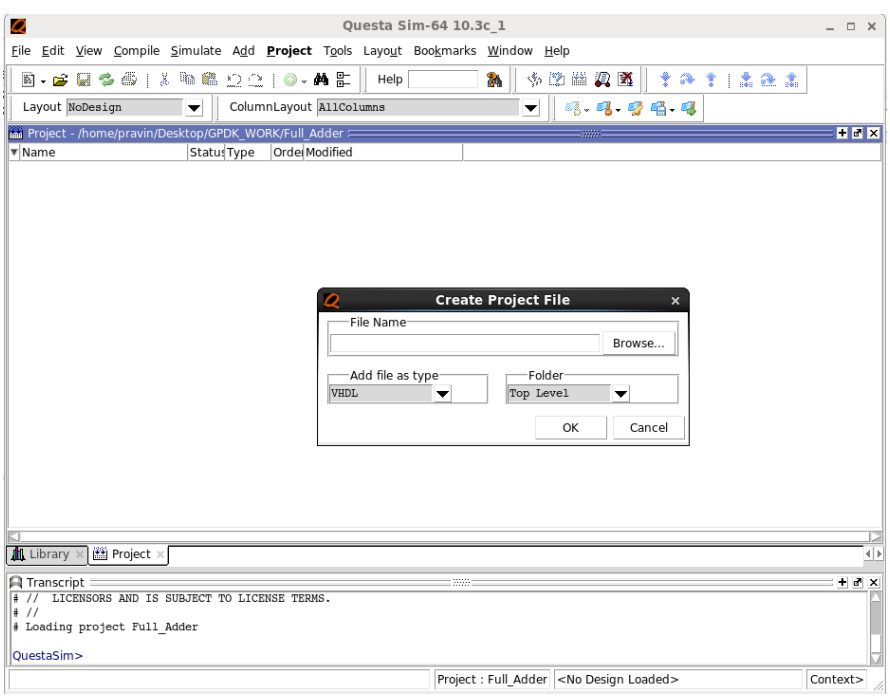

Figure 6: Modelsim Create Project File alternate

The **.v** file with file name entered in **Step 5** will be created and listed in Project window (e.g.Full_adder_G.v in this demonstration)

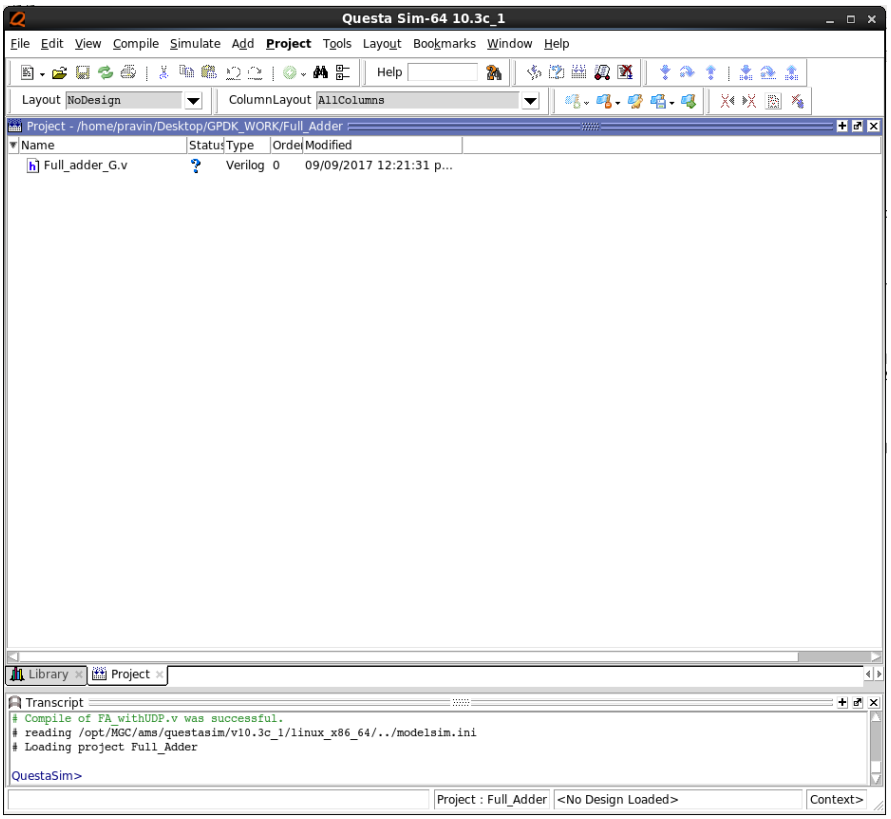

Figure 7: Modelsim listing of .v file in Project window

Step 6 : Select **.v** file in Project window, right click on it and select **Edit**. Editor subwindow will be opened in Modelsim

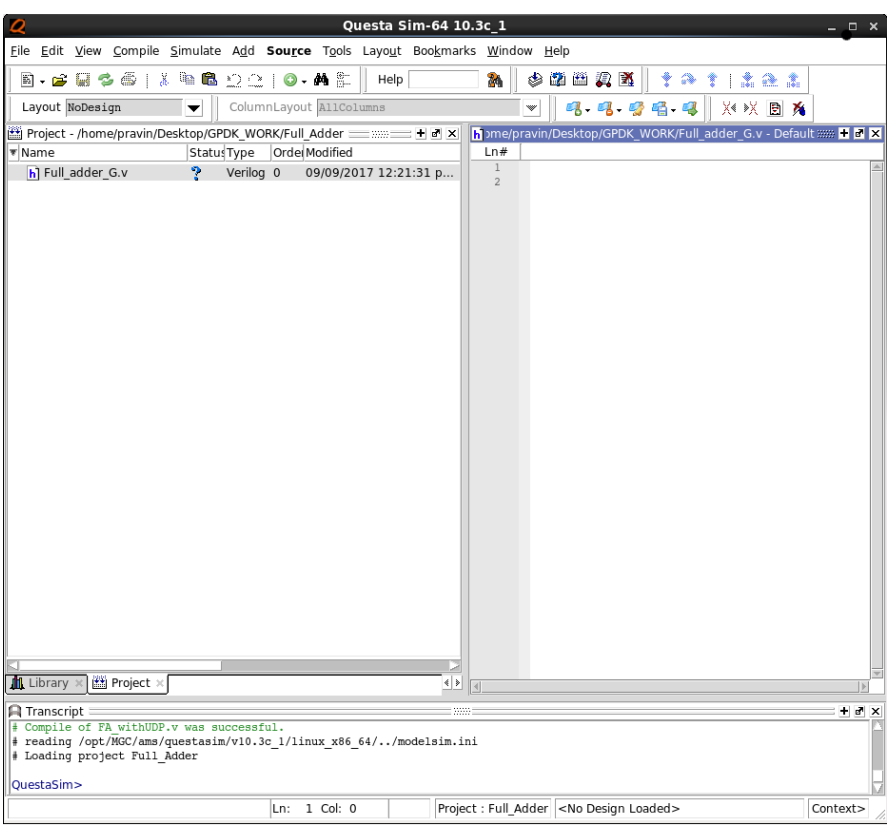

Figure 8: Modelsim Editor subwindow

Step 7 : Enter the verilog code in Editor window and save it.

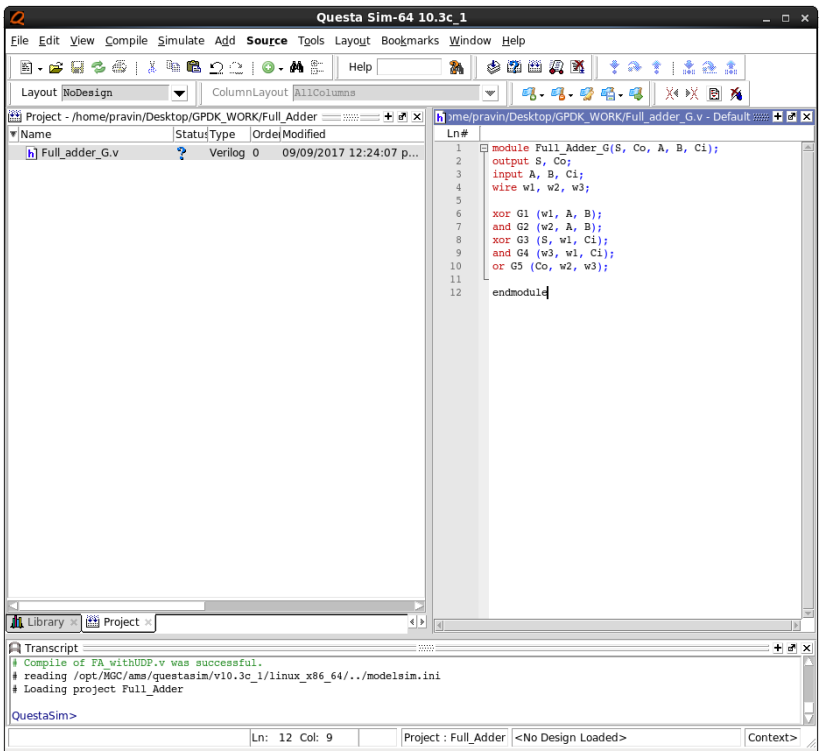

Figure 9: Modelsim Editor subwindow with verilog code

Note : The verilog file name can be different from Module name in verilog code. In fact they are different in this demonstration (Full_adder_G.v is file name and Full_Adder_G is module name. Remember that verilog is case sensitive).

Step 8 : Compilation- Right click on **.v** file in **Project** window, select **Compile** →**Compile Selected/Compile All**. If code is error-free, the code will be compiled successfully and such message can be seen in **Transcript** window. If any error is there in code, edit the verilog code, save it and compile it again until it is error-free.

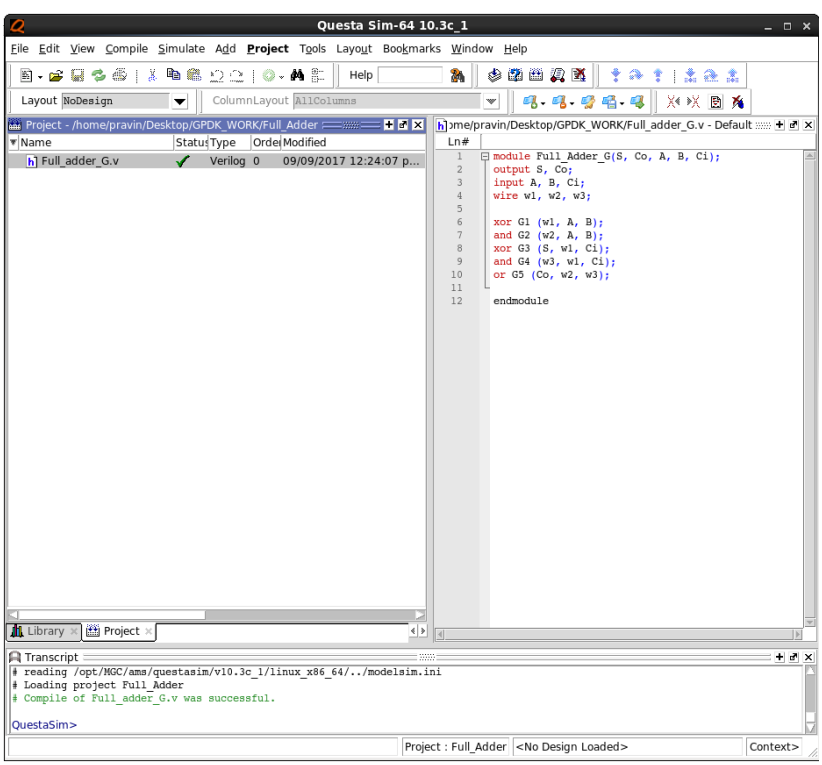

Figure 10: Modelsim Compilation successful

SIMULATION WITHOUT TESTBENCH

Step 9a : Select **Library** tab. **Library** window will be active in place of **Project** window.

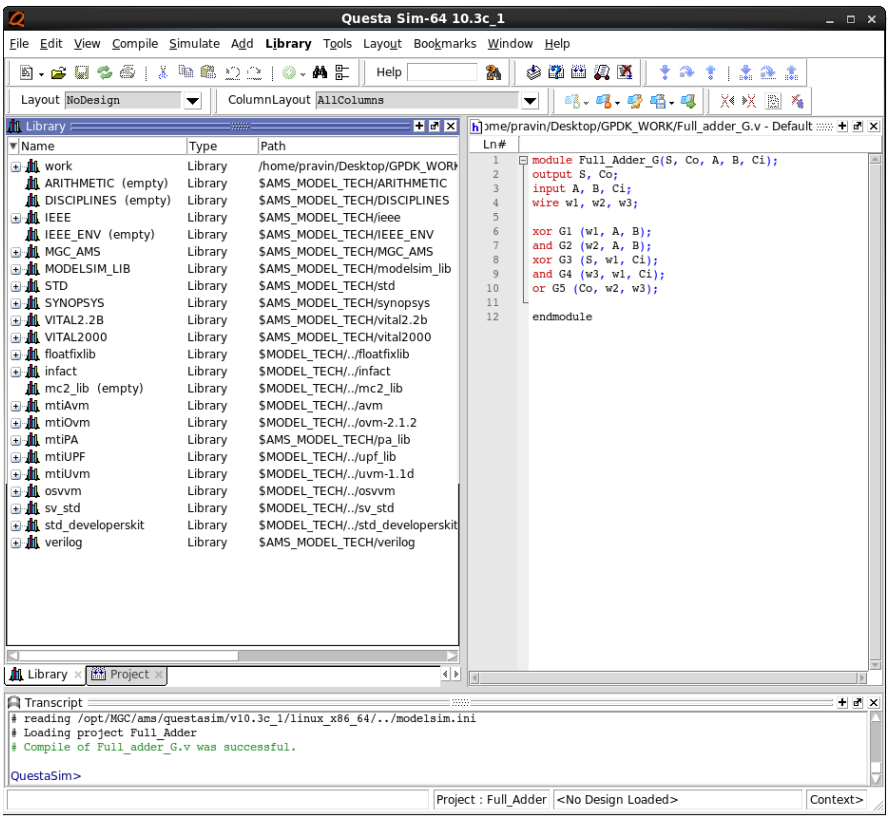

Figure 11: Modelsim Library window

Step 9b : In the **Library** window, expand **Work** folder hierarchy. You will find module name (written in code, e.g.Full_Adder_G in this demonstration) under it. Select module, right click it, and click on **Simulate** option in right click menu.

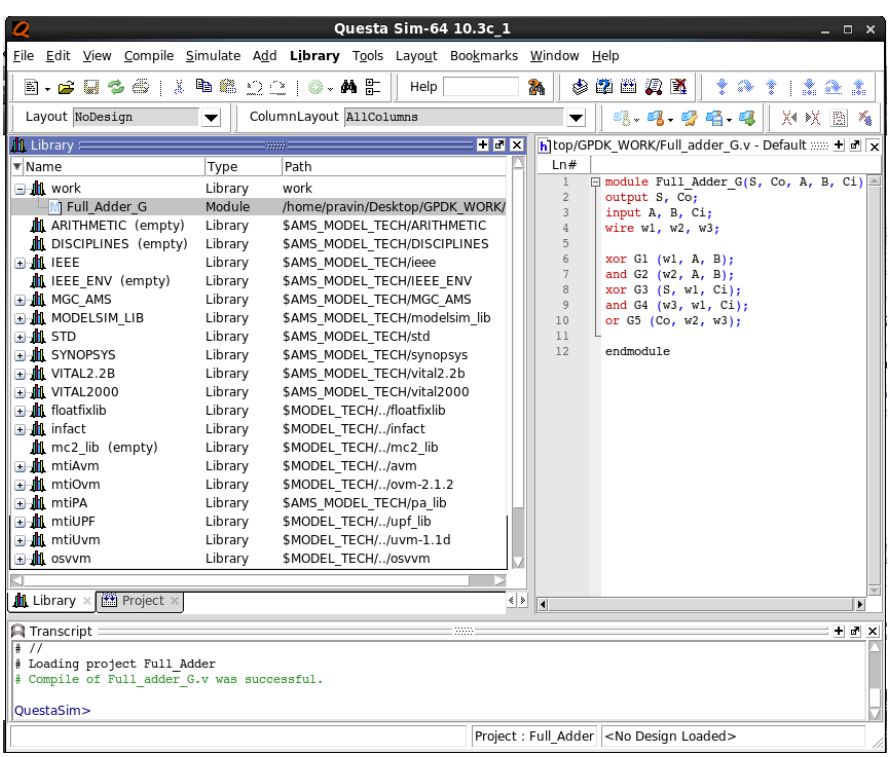

Figure 12: Modelsim Library window

Step 9b : Three windows will be available on GUI (1) **Library/Project/sim** window on left (2) **Objects** window in the middle and (3) **Wave/Editor** window on the right. If any of these windows not available (e.g. **Objects** window and **Wave** window), they can be added by clicking on **View** option on top menu in GUI and then selecting required option. Make **sim**, **Objects** and **Wave** windows active by selecting them.

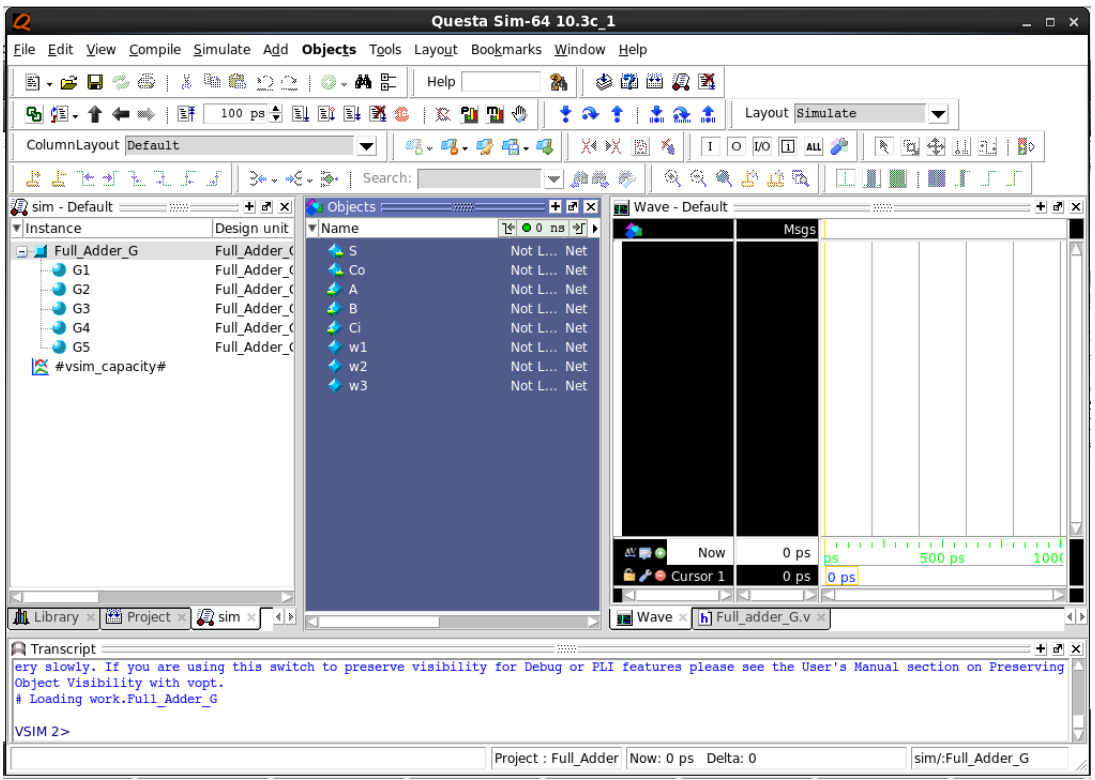

Figure 13: Modelsim Simulation environment

Step 9c : Select the signals to be plotted in **Objects** window, drag and drop them in **Wave** window.

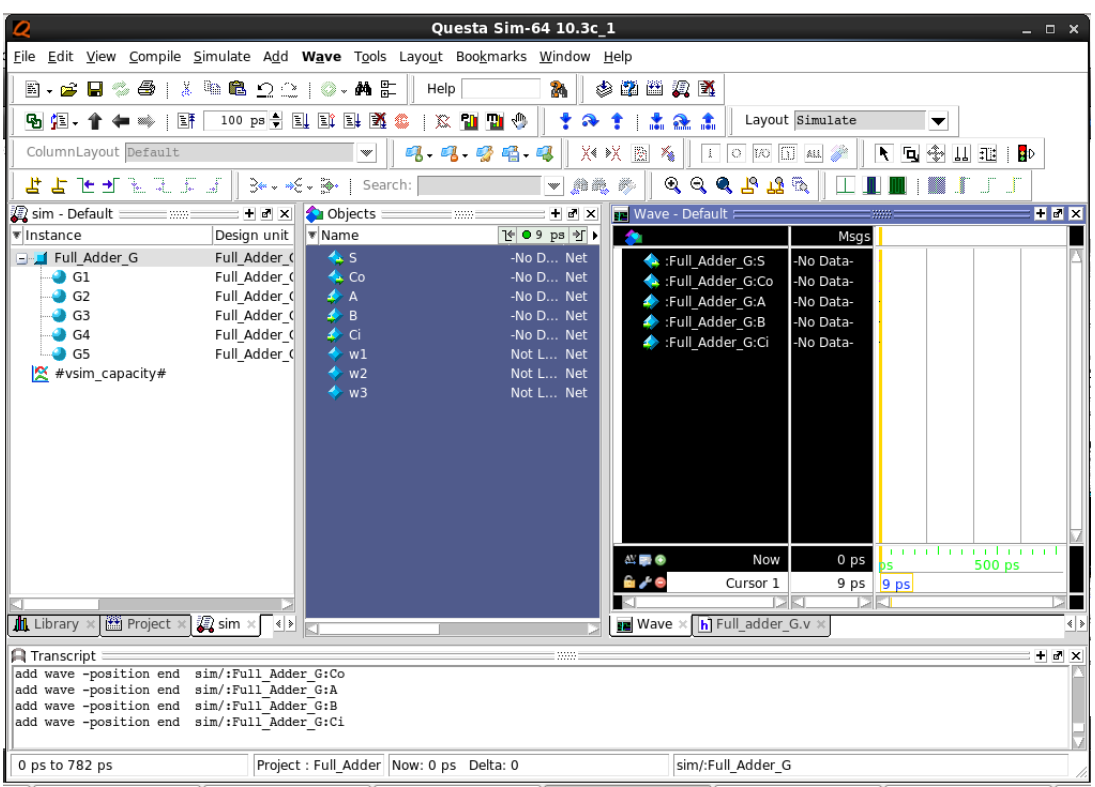

Figure 14: Modelsim Simulation environment with signals

Step 9d : Now select one **input** signal at a time from **Wave** window, right click on it and select **Force** option from right click menu. **Force Selected Signal** window will pop-up. Enter signal value in **Value** option in this form (either **0** or **1** in this demonstration) and click OK. Force the values on all **input** signals in similar manner.

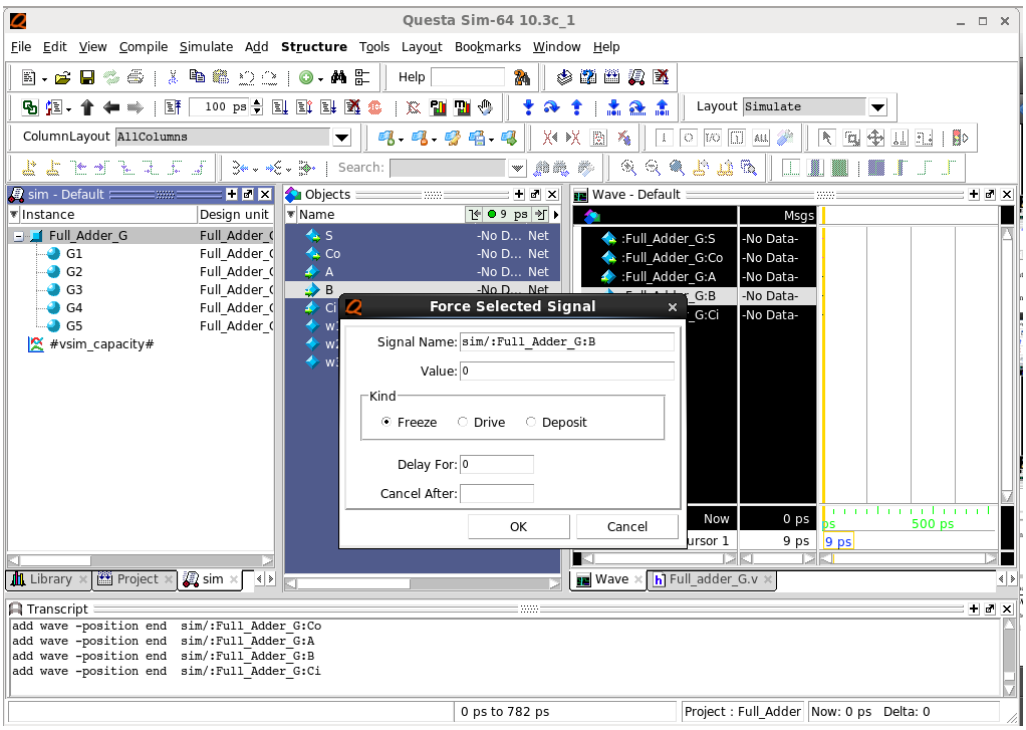

Figure 15: Modelsim Simulation environment forcing values

Step 9e : Click on **Run** button (adjacent to 100 ps incrementer/decrementer option for simulation time). If clicked once simulation will be run for 100 ps, if clicked multiple times, simulation will run for multiples of 100 ps. In this demonstration, simulation is run for 200 ps, another set of values forced on inputs as explained in Step 9d, and again simulation is done for 200 ps and so on.

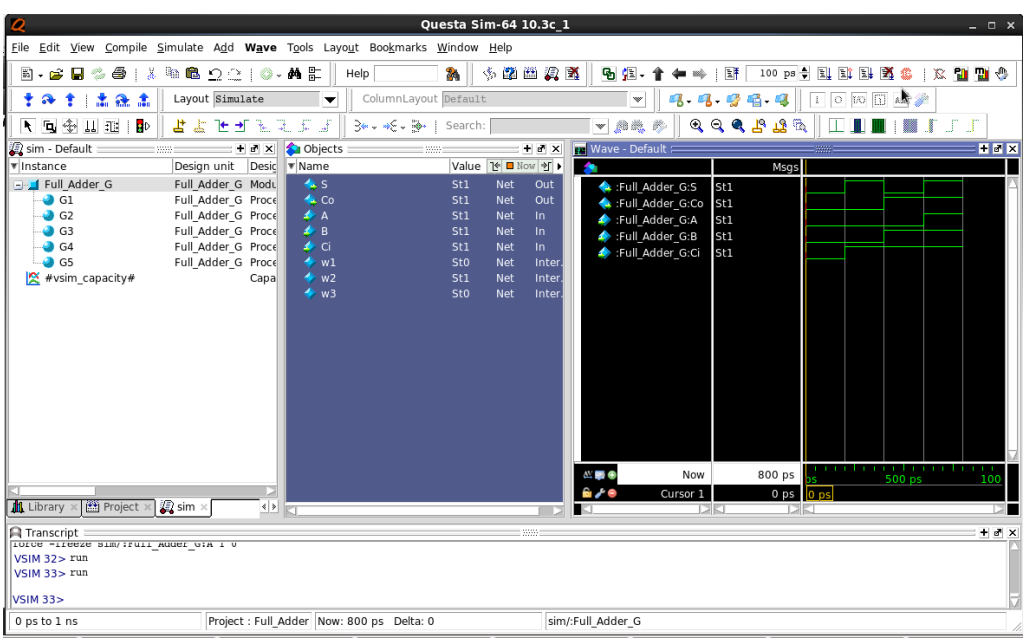

Figure 16: Modelsim Simulation environment waveforms

Visibility of waveforms in Wave window can be adjusted with **Zoom In**, **Zoom Out** and **Zoom Full** buttons.

To stop simulation, select **Simulate** menu on top of GUI and click **End Simulation** option in it.

SIMULATION WITH TESTBENCH

Step 10a : In the Project window area, right click and select **Add to project file** →**New File...**. In **Create Project File** form, **File Name** and **Add file as type** fields are filled appropriately.

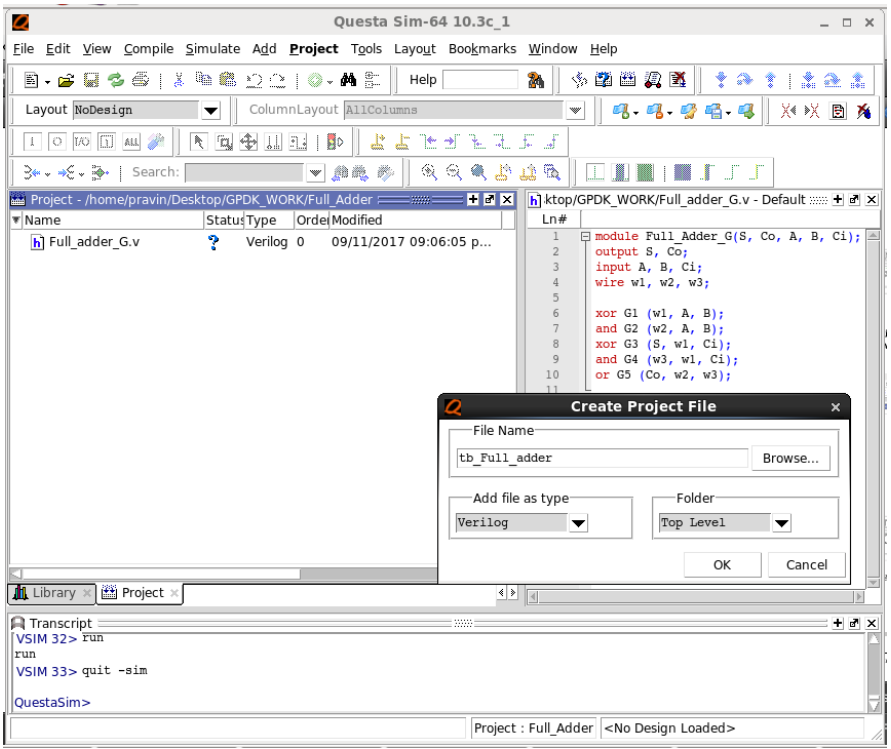

Figure 17: Modelsim adding testbench

The **.v** file with file name entered in **Step 10a** will be created and listed in Project window (e.g.tb_Full_adder.v in this demonstration) in addition to previously added file.

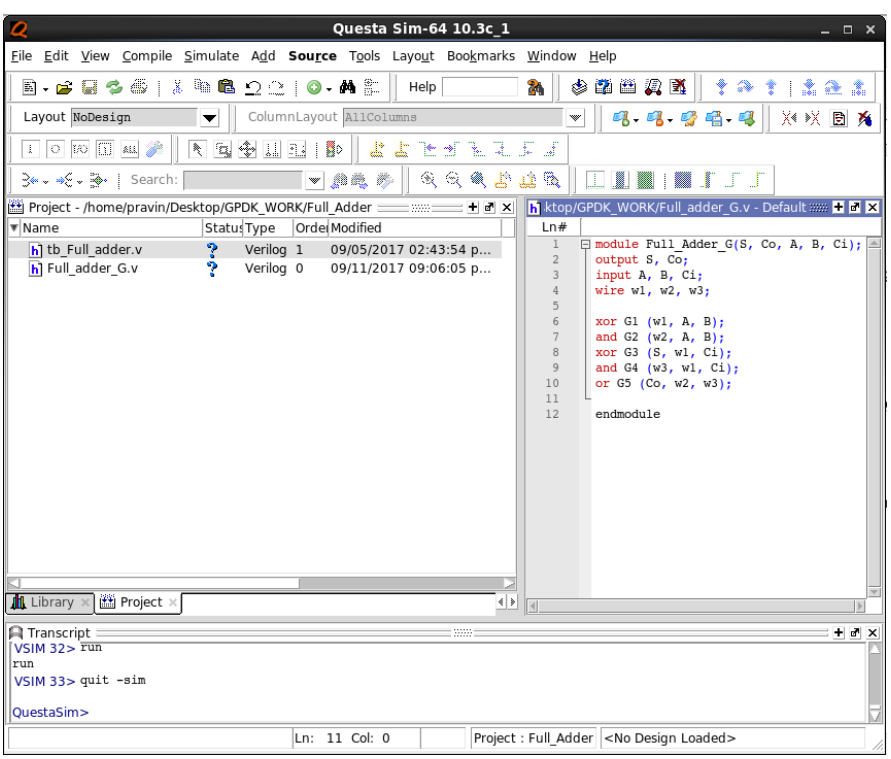

Figure 18: Modelsim file listing

Step 10b : In Project window, select newly added file, and open for editing by right clicking it. Enter code in editor and save it.

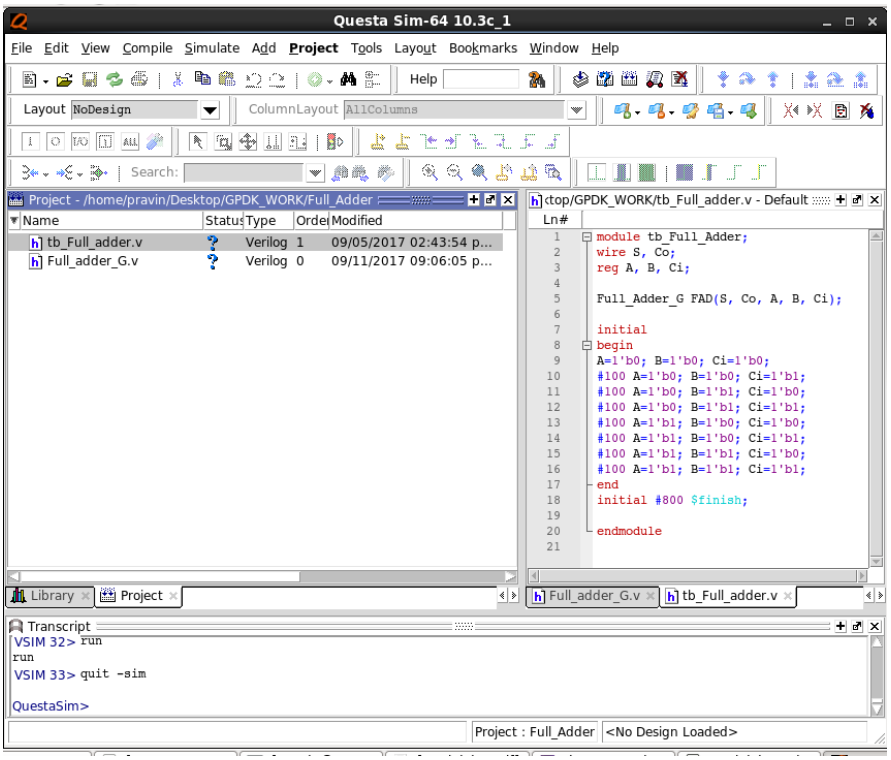

Figure 19: Modelsim entering testbench code

Step 10c : Compilation- Right click on **.v** (testbench) file in **Project** window, select **Compile** →**Compile All**. If code is error-free, the code will be compiled successfully and such message can be seen in **Transcript** window. If any error is there in code, edit the verilog code, save it and compile it again until it is error-free. Automatically other file gets compiled as it is component in testbench.

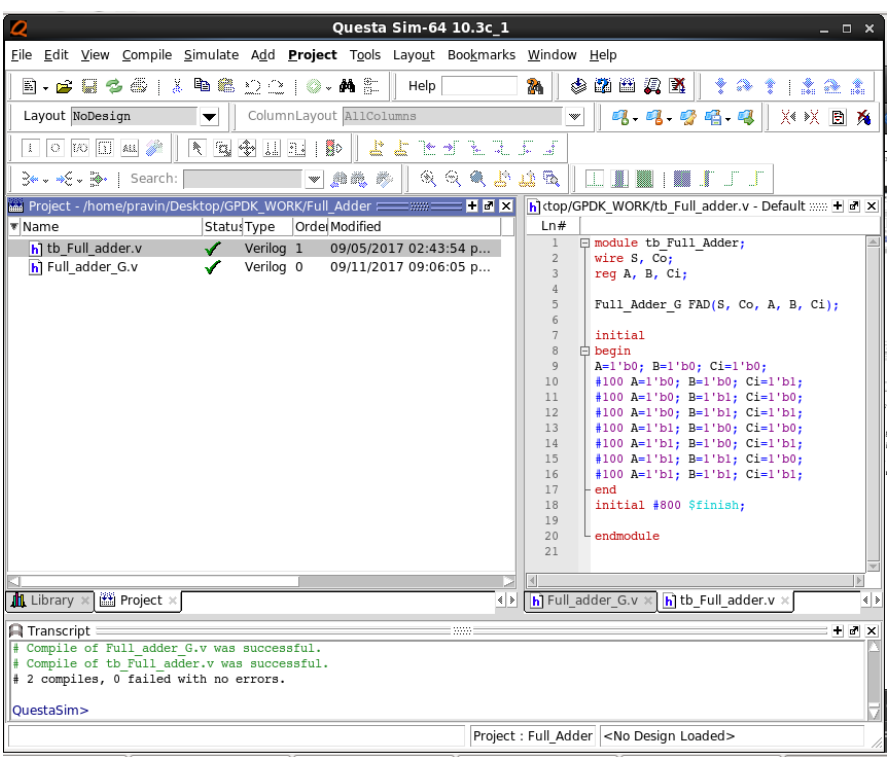

Figure 20: Modelsim entering testbench code compilation

Step 10d : Select **Library** tab. **Library** window will be active in place of **Project** window. In the **Library** window, expand **Work** folder hierarchy. You will find two modules (written in code, e.g.Full_Adder_G in Full_adder_G.v and tb_Full_Adder in tb_Full_adder.v in this demonstration) under it. Select testbench module (tb_Full_Adder), right click it, and click on **Simulate** option in right click menu.

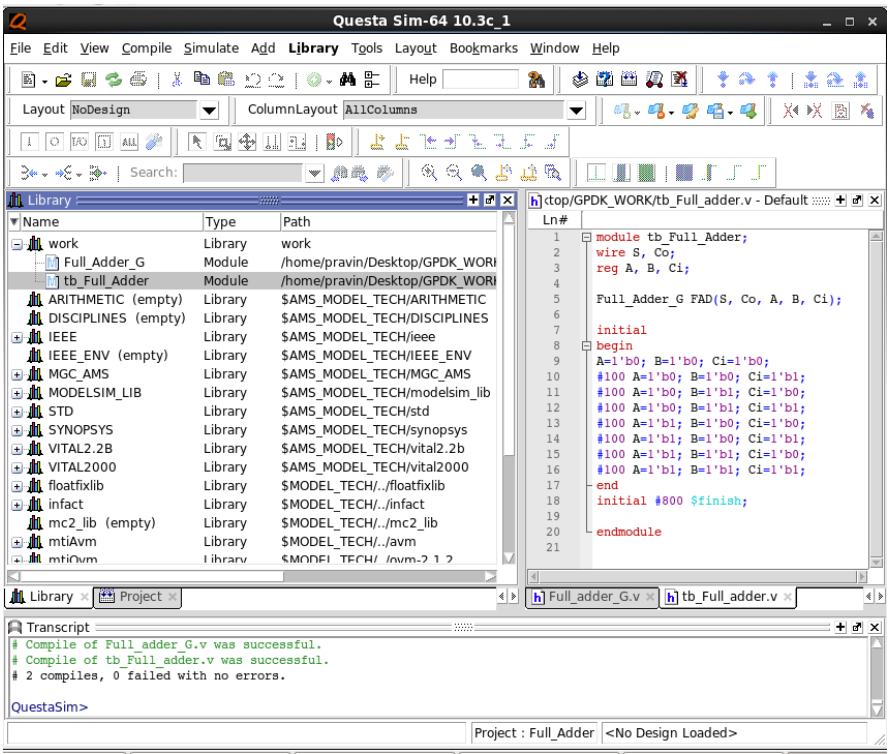

Figure 21: Modelsim Library window for simulation

Step 10e : Three windows will be available on GUI (1) **Library/Project/sim** window on left (2) **Objects** window in the middle and (3) **Wave/Editor** window on the right. If any of these windows not available (e.g. **Objects** window and **Wave** window), they can be added by clicking on **View** option on top menu in GUI and then selecting required option. Make **sim**, **Objects** and **Wave** windows active by selecting them. Also select the signals to be plotted in **Objects** window, drag and drop them in **Wave** window.

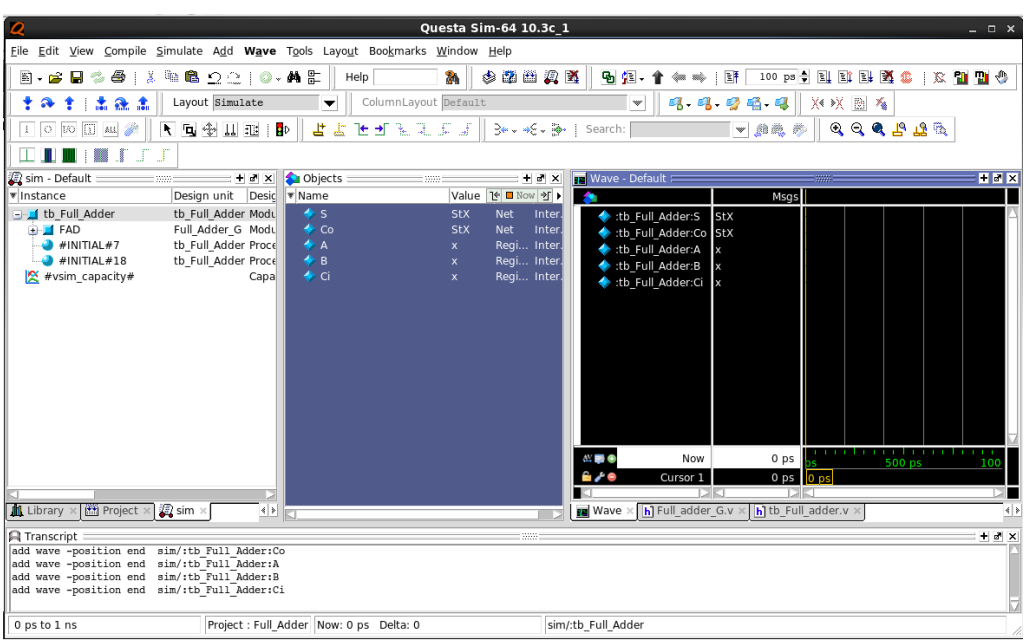

Figure 22: Modelsim simulation environment with signals

Step 10f : Click on **Run All** button to simulate it for time specified in the testbench. Inputs are taken from the **initial** block in testbench file.

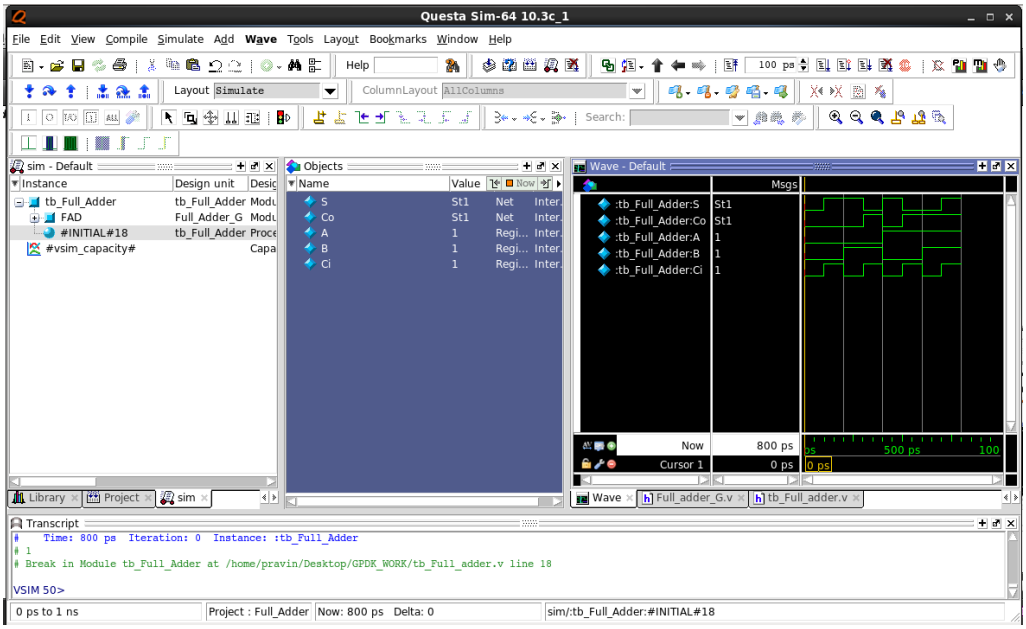

Figure 23: Modelsim simulation environment with waveforms after simulation

The example files used in this demonstration are provided separately.