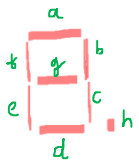
DIGITAL DESIGN

Lecture 16

Sarang Dhongdi

BCD to 7-Segment decoder

- Design a logic that will convert a NBCD value to 7-segment equivalent.



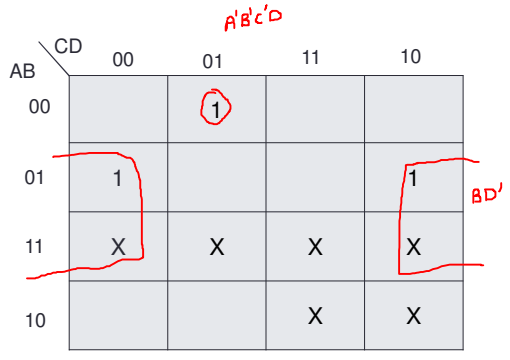
A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

a	b	c	d	e	f	g
0	0	0	0	0	0	1
1	0	0	1	1	1	1
0	0	1	0	0	1	0
0	0	0	0	1	1	0
1	0	0	1	1	0	0
0	1	0	0	1	0	0
1	1	0	0	0	0	0
0	0	0	1	1	1	1
0	0	0	0	0	0	0
0	0	0	1	1	0	0

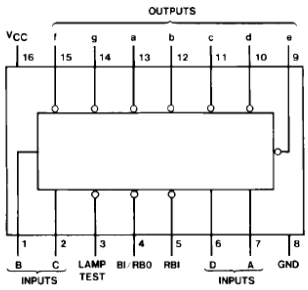
Functions

- a = Σ (1,4,6)
- b = Σ (5,6)
- c = Σ (2)
- d = Σ (1,4,7,9)
- e = Σ (1,3,4,5,7,9)
- f = Σ (1,2,3,7)
- g = Σ (0,1,7)

AB \ CD	00	01	11	10
00		1		
01	1			1
11	X	X	X	X
10			X	X



IC 7447

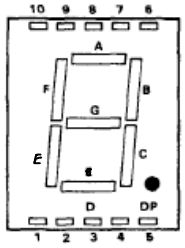


DCBA (MSB to LSB)

LT – Lamp test
BI – Blanking input
RBI – Ripple blanking i/p
RBO – Ripple blanking o/p

When LT = L, all segment outputs are L.
When BI/RBI = L, all segment outputs are H.

FND 507



Pin	FND507/567
1	Segment E
2	Segment D
3	Common Anode
4	Segment C
5	Decimal Point
6	Segment B
7	Segment A
8	Common Anode
9	Segment F
10	Segment G

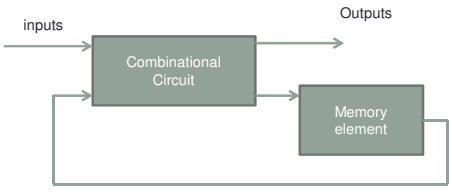
SYNC SEQUENTIAL LOGIC

Ch. 5

Sequential Logic

- Combinational circuits - value of each output depends solely on the values of signals applied to the inputs.
- There exists another class of logic circuits in which the values of the outputs depend not only on the present values of the inputs but also on the past behavior of the circuit.
- Such circuits include storage elements that store the values of logic signals. The contents of the storage elements are said to represent the *state* of the circuit.

Block diagram



Sequential Logic

- Sequential Logic – O/p are function not only of i/p but also of present state of storage elements.
- State of sequential ckt (at time t) – Binary information stored in storage element at that time.
- Next state of storage elements is also function of input and present state.

- Sequential Circuits

Synchronous

Behavior defined at discrete Intervals of time.

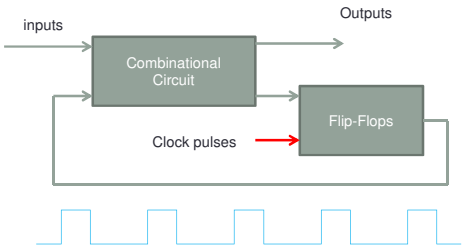
Asynchronous

Depends on i/p signals at any instant of time and the order in which i/ps change.

Synchronous sequential circuits

- Synchronous with the help of clock generator.
- Clock signal has periodic train of clock pulses.
- Storage elements are affected only with the arrival of each pulse.
- Activity within the circuit and the resulting updating of stored values is synchronized to the occurrence of clk pulses.
- ***clocked sequential circuits***

Block diagram



STORAGE ELEMENTS

LATCHES

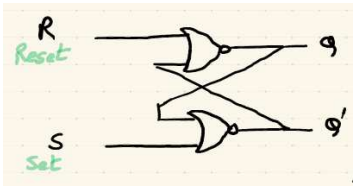
Latches and Flip-flops

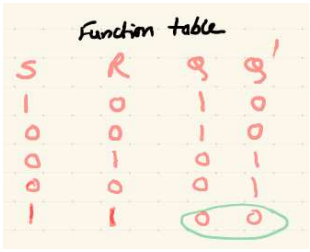
- *Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops.*
- Latches are said to be level sensitive devices; flip-flops are edge-sensitive devices.

Latch

- a circuit which retains whatever output state results from a momentary input signal until reset by another signal.
- (of a device) become fixed in a particular state.

S-R Latch



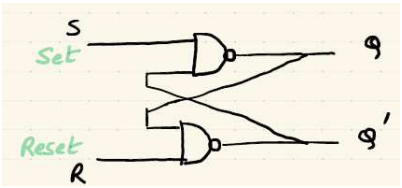


After S=1, R =0

After S=0, R =1

Forbidden state

SR Latch with NAND gates

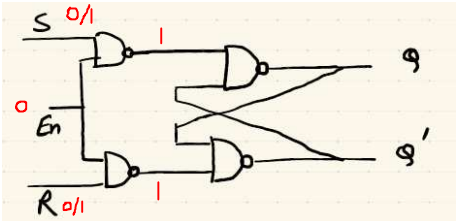


After S=1, R =0

After S=0, R =1

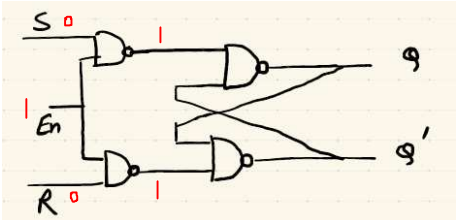
Forbidden state

SR Latch with control input



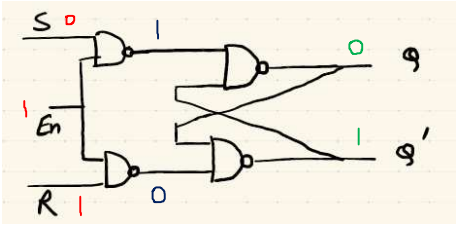
En	S	R	Next state of Q
0	X	X	No change

SR Latch with control input



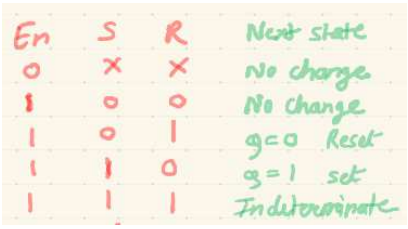
En	S	R	Next state of Q
1	0	0	No change

SR Latch with control input

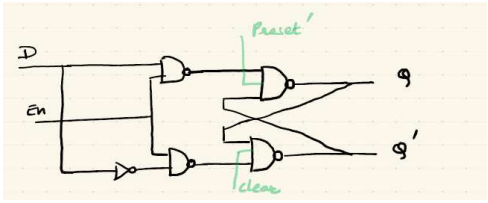


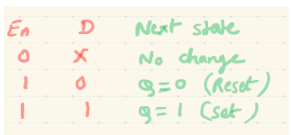
En	S	R	Next state of Q
1	0	1	Q=0, Reset

- When *En* returns to 0, the circuit remains in its current state.
- The control input disables the circuit by applying 0 to *En*, so that the state of the output does not change regardless of the values of *S* and *R* .
- Moreover, when *En* = 1 and both the *S* and *R* inputs are equal to 0, the state of the circuit does not change.

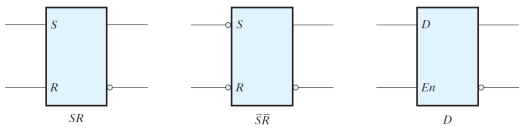


D Latch (Transparent Latch)





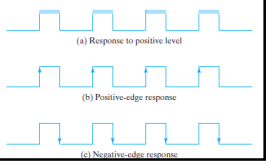
Symbols



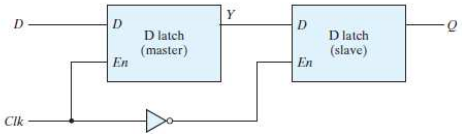
FLIP-FLOPS

Flip-flops

- Latches respond to the change in *level* of a clock pulse.
- State of the latches may keep changing for as long as the clock pulse stays at "active" level –Unreliable operation.
- Flip-flop is triggered only during a signal *transition* – providing proper operation in the sequential ckt having common clock.



Edge-Triggered *D* Flip-Flop



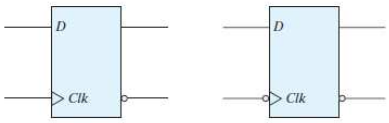
A change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

Edge-Triggered *D* Flip-Flop

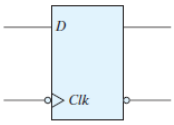
(1) the output may change only once,

(2) a change in the output is triggered by the negative edge of the clock, and

(3) the change may occur only during the clock's negative level.



D Flip Flop

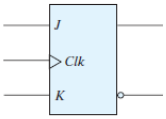


Q(t+1) =D

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

J-K Flip Flop



JK Flip-Flop

J	K	Q(t + 1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement