BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI –K. K. BIRLA GOA CAMPUS
INSTRUCTION DIVISION
FIRST SEMESTER 2018-2019
COURSE HANDOUT (PART II)

August 2, 2018

In addition to part-I (General Handout for all courses appended to the time-table), this portion gives further specific details regarding the course.

Course No. : CS F215/ECE F215/EEE F215/INSTR F215

Course Title : Digital Design

Instructor-in-charge : PRAVIN MANE *(pravinmane@goa.bits-pilani.ac.in)*

Team of Instructors : Sarang C Dhongdi, Sudeep Baudha, Debidas Kundu, Shailendra Dhakad, Hrishikesh Sonalikar, Darshak Bhatt, Naik Akhilesh Gurudas, Prateek Singh, Manish Varun Yadav

1 Course Description:

This course covers the topics on logic circuits and minimization, Combinational and Sequential logic Circuits, Programmable Logic devices, State table and state diagrams, Digital ICs, Arithmetic operations and algorithms, Introduction to Computer organization, Algorithmic State Machines.

2 Scope and Objective of the Course:

The objective of the course is to impart knowledge about the basic tools for the design of digital circuits and to provide methods and procedures suitable for a variety of digital design applications. The course also introduces fundamental concepts of computer organization. The course also provides laboratory practice using MSI devices, Xilinx ISE software tools and FPGA.

3 Text Books:

1. M.Moris Mano, “Digital Design”, Pearson, 4^{th} Edition, 2009.
2. Brian Holdsworth, Clive Woods, “Digital Logic Design”, Elsevier, 4^{th} Edition, 2008

4 Reference Book:

1. John.M.Yarbrough, “Digital Logic Design”, Cengage Learning, 2009.

2. Ronald.J.Tocci, Neal.S.Widmer, Gregory.L.Moss, “Digital Systems”, 2007.

3. Stephen Brown, Zvonko Vranesic, “Digital Logic with VHDL Design”, McGraw Hill,2013

5 Course Plan:

Lect. No.	Learning Objectives	Topics to be covered	Reference to Text Book 1
1	Introduction to Digital Systems and Characteristics of Digital ICs.	Digital Systems, Digital ICs	1.1;1.9; 2.8
T1	Codes number systems	Number systems and codes	1.2-1.8
2-6	Boolean Algebra Simplification of Boolean functions	Law of Boolean Algebra, K-Maps (4,5 variables), QM Method	2.1-2.7, 3.1 to 3.8
7-9	Combinational Logic, Arithmetic circuits	Adders, Subtracters Multipliers	4.1 - 4-6
10-12	MSI Components	Comparators, Decoders, Encoders, MUXs, DEMUXs	4.7 to 4.10
13-14	Digital Integrated Circuits	TTL, MOS Logic families and their characteristics	10.3, 10.5, 10.7 to10.10
15-16	Sequential Logic	Flip-Flops & Characteristic tables, Latches.	5.1 to 5.3
17-18	Clocked Sequential Circuits	Analysis of clocked sequential circuits, state diagram and reduction	5.4, 5.6
19-23	Registers & Counters	Shift registers, Synchronous & Asynchronous counters	6.1 to 6.5
24-28	Design of Asynchronous Circuits.	Asynchronous Sequential Logic	9.1 – 9.7
29-30	Memory and PLDs	RAM, ROM, PLA, PAL	7.1, 7.5 to 7.7
31-32	Analysis of arithmetic units	Multiplication & Division algorithms	T2: Appendix A
33-35	Modular approach for CPU Design	RTL, HDL description	8.1,8.2, 8.4 to 8.7
36-38	Design of Digital Systems	Algorithmic State Machines	R2. Chapter 8
39-40	Memory Organization	Memory Hierarchy & different types of memories	T2: Ch 6

6 Evaluation:

Component	Duration	Maximum Marks	Date	Remarks
Theory				
Mid-Term Test	90 Min	60	11/10/2018 11.00 am to 12.30 pm	CB
Quiz-I	30 Min	10	28/08/2018 6.00 pm to 6.30 pm	CB
Quiz-II	30 Min	10	25/09/2018 6.00 pm to 6.30 pm	OB
Quiz-III	30 Min	10	23/10/2018 6.00 pm to 6.30 pm	CB
Quiz-IV	30 Min	10	20/11/2018 6.00 pm to 6.30 pm	OB
Comprehensive Examination	3 Hrs	100	08/12/2018 (FN) 9.00 am to 12.00 noon	CB/OB
Lab				
H/w Lab Evaluation		50	Regularly	OB
Verilog Evaluation-I		10	23/09/2018 10.00 am to 5.00 pm	OB
Verilog Evaluation-II		10	18/11/2018 10.00 am to 5.00 pm	OB
H/w Lab Comprehensive		30	01/11-21/11	OB

7 Chamber Consultation Hour:

To be announced in the class.

8 Make-up Policy:

Make up for any component will be given only in genuine cases. In all cases prior intimation must be given to IC.

9 Notices:

All notices related to the course will be put on moodle page of course. Also students are requested to check their mails on institute Email ID regularly.

Instruction Incharge

CS F215/ECE F215/EEE F215/INSTR F215