Ex 1: Draw the logic diagram of a 2-to-4-line decoder using (a) NOR gates only and (b) NAND gates only. Include an enable input.

Ex 2: Design a BCD-to-decimal decoder using the unused combinations of the BCD code as don't-care conditions.

Ex 3: Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components.

Ex 4: Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.

Ex 5: A combinational circuit is specified by the following three Boolean functions:

$$F_1(A,B,C) = \sum m(1,4,6)$$

$$F_2(A,B,C) = \sum m(3,5)$$

$$F_3(A,B,C) = \sum m(2,4,6,7)$$

Implement the circuit with a decoder constructed with NAND gates and NAND or AND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.

Ex 6: Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

(a)

$$F_1 = x'yz' + xz$$

$$F_2 = xy'z' + x'y$$

$$F_3 = x'y'z' + xy$$

(b)

$$F_1 = (y' + x)z$$

$$F_2 = y'z' + x'y + yz'$$

$$F_3 = (x + y)z$$

Ex 7: Design a four-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority.

Ex 8: Construct a 16×1 multiplexer with two 8×1 and one 2×1 multiplexers. Use block diagrams.

Ex 9: Implement the following Boolean function with a multiplexer

(a) $F_1(A,B,C,D) = \sum m(0,2,5,8,10,14)$

(b) $F_1(A,B,C,D) = \prod M(2,6,11)$

Ex 10: Implement a full adder with two 4×1 multiplexers.

Ex 11: An 8×1 multiplexer has inputs A , B , and C connected to the selection inputs S_2 , S_1, and S_0, respectively. The data inputs I_0 through I_7 are as follows:

(a) I_1=I_2= I_7=0; I_3=I_5=1; I_0= I_4= D ; and I_6=D'.

(b)I_1=I_2=0; I_3=I_7=1; I_4= I_5= D ; and I_0=I_6=D'.

Determine the Boolean function that the multiplexer implements.

Ex 12: Implement the following Boolean function with a 4×1 multiplexer and external gates.

(a) $F_1(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$

(b) $F_1(A,B,C,D) = \sum m(1,2,5,7,8,10,11,13,15)$

Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D . These values are obtained by expressing F as a function of C and D for each of the four cases when AB=00, 01, 10, and 11. These functions may have to be implemented with external gates.