Electronic Devices

Lecture 3

09-08-2018

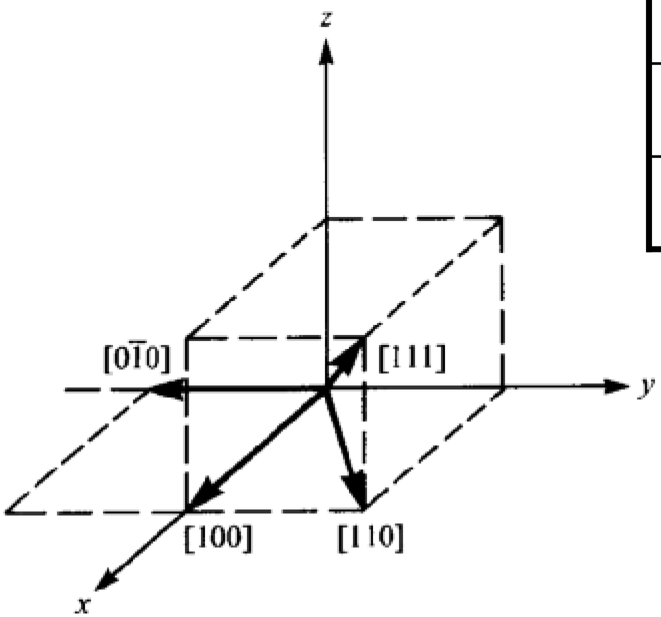
Crystallographic Notation

Miller Indices

Notation	Interpretation
(*h k l*)	crystal plane
{ *h k l* }	equivalent planes
[*h k l*]	crystal direction
< *h k l* >	equivalent directions

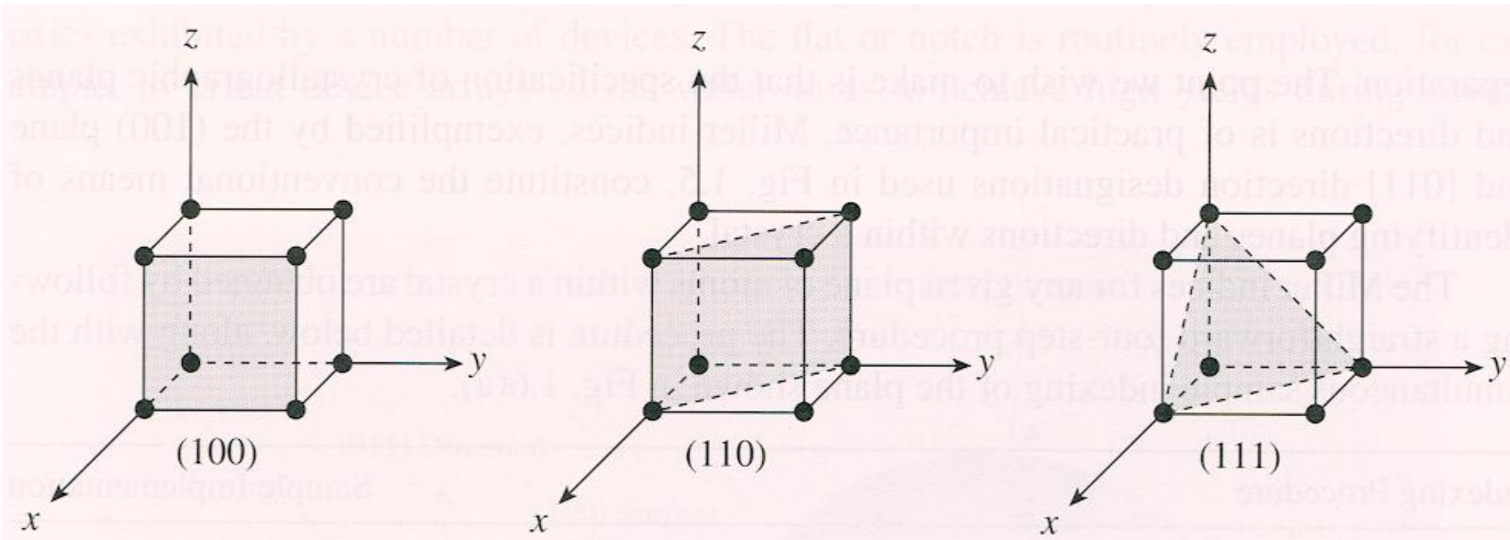
h: **inverse *x*-intercept of plane**
k: **inverse *y*-intercept of plane**
l: **inverse *z*-intercept of plane**

(*h*, *k* and *l* are reduced to 3 integers having the same ratio.)

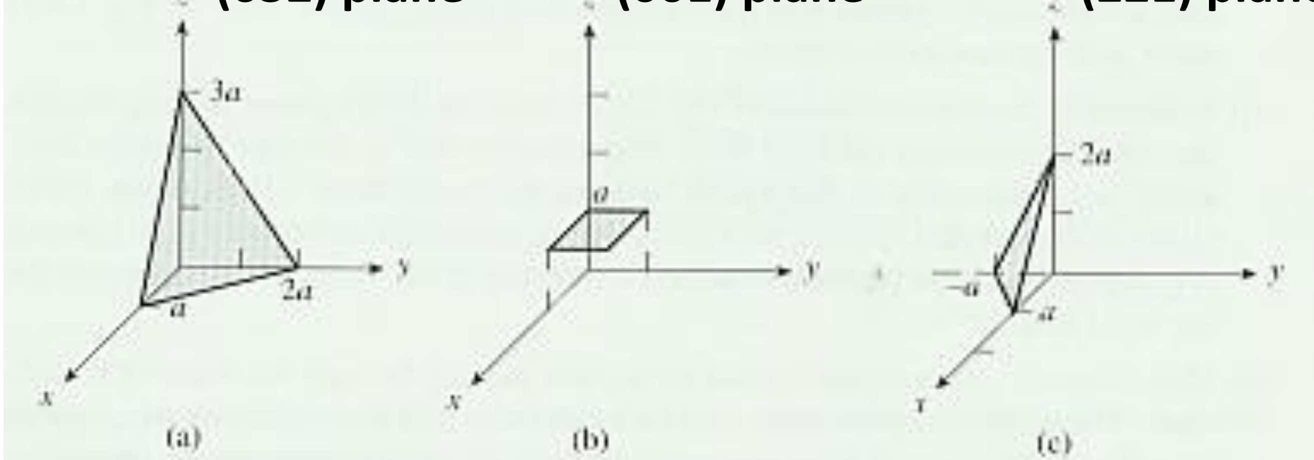


Sample direction vectors and their corresponding Miller indices.

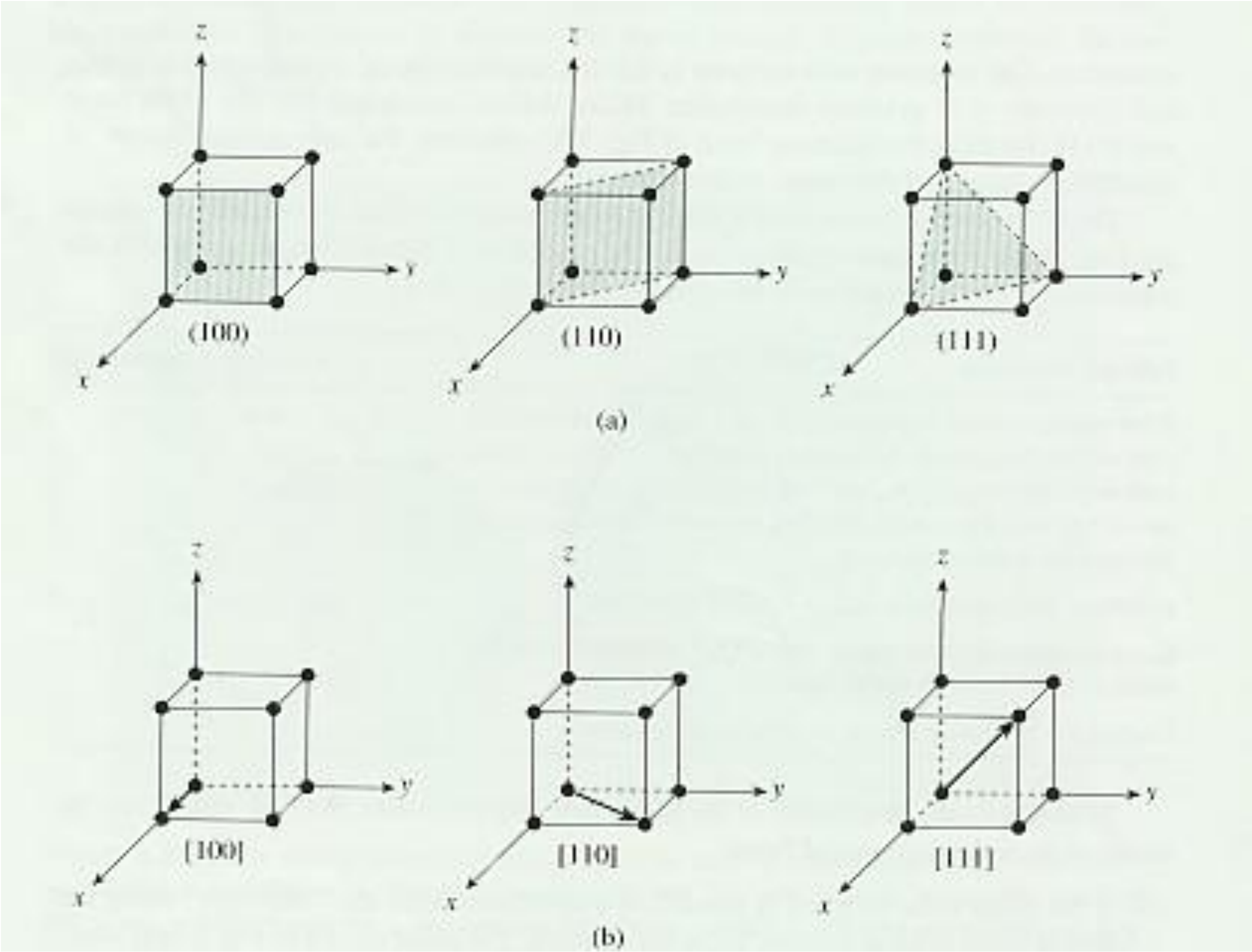
Crystallographic Planes



(632) plane **(001) plane** **(2$\bar{2}$1) plane**



Crystallographic Planes



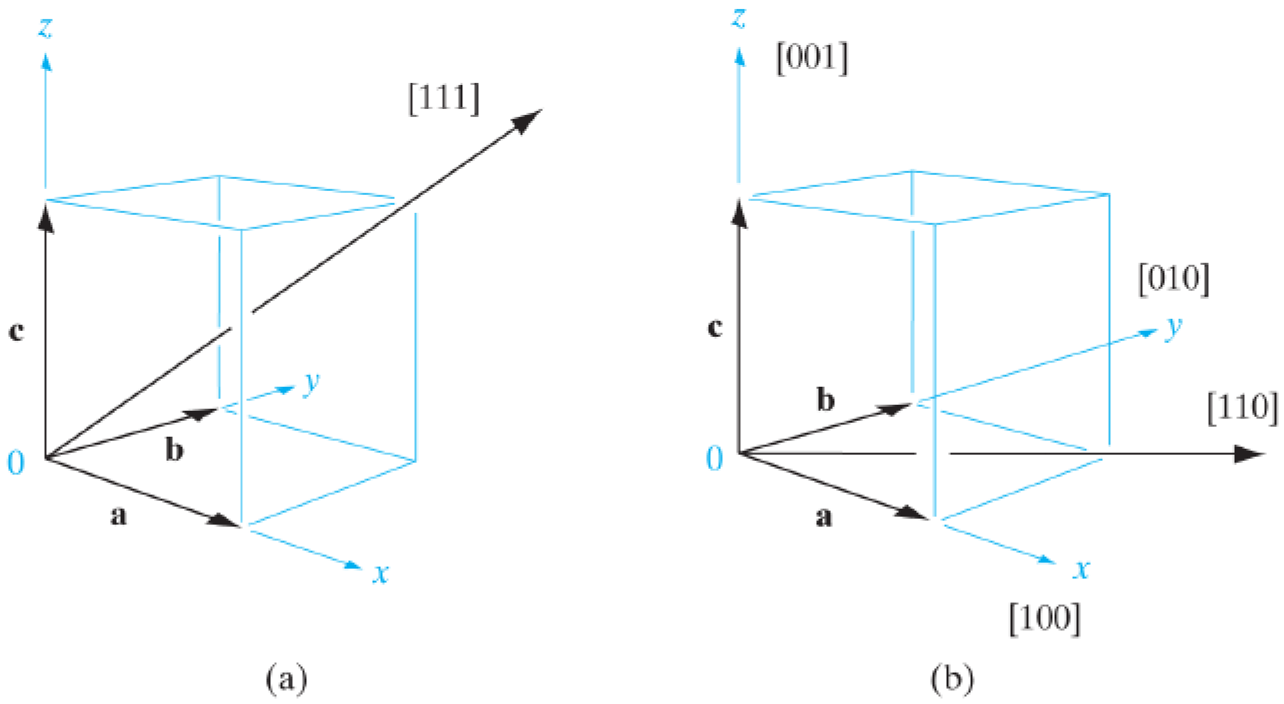
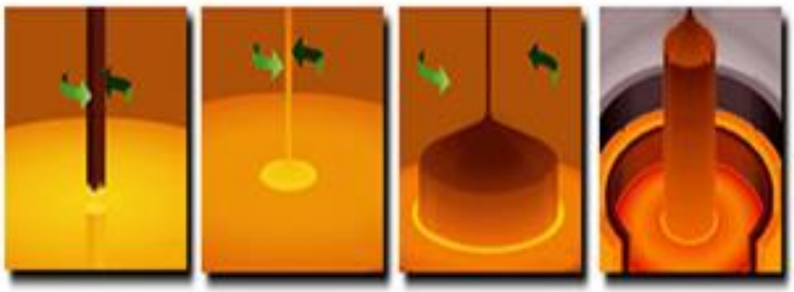
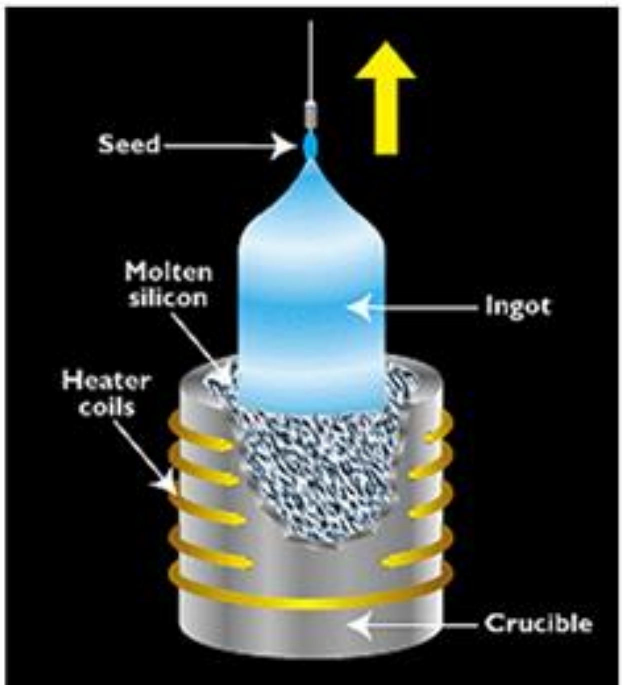


Figure 1.7

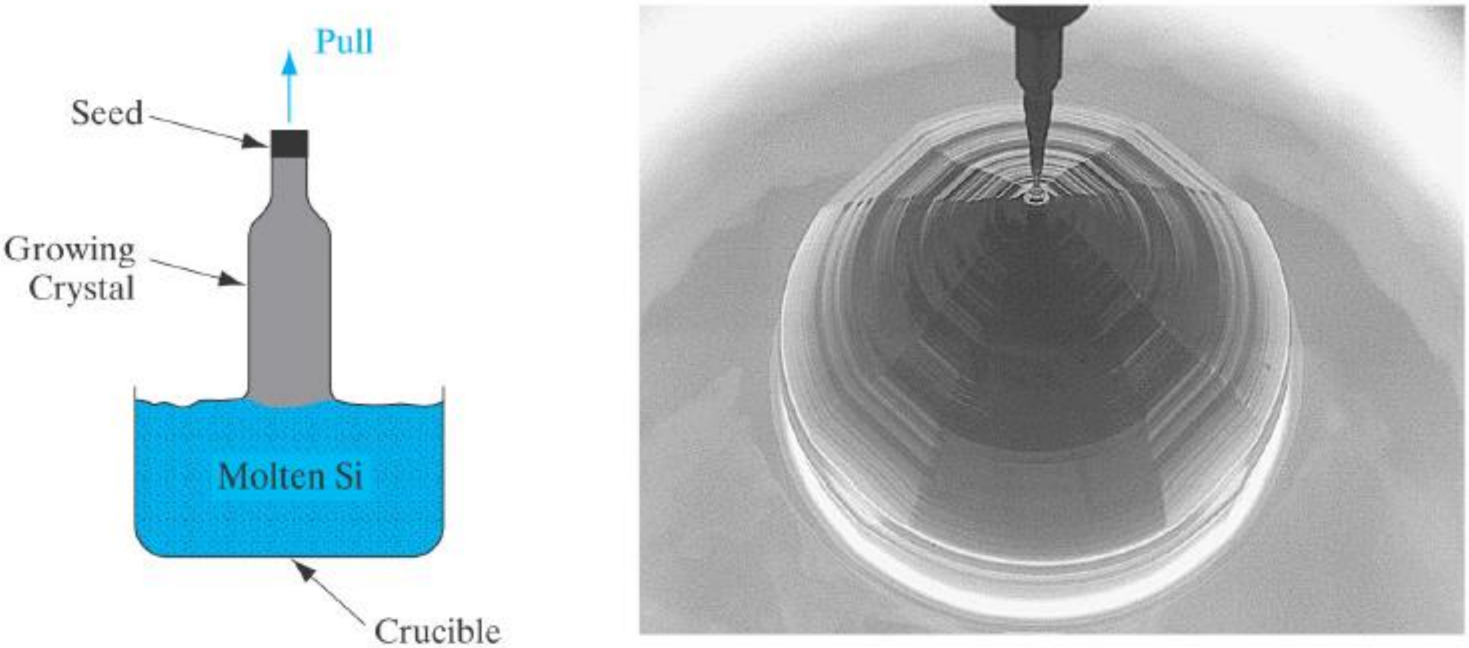
Crystal directions in the cubic lattice.

IC Fabrication Steps





Crystal Growth   CZ Method



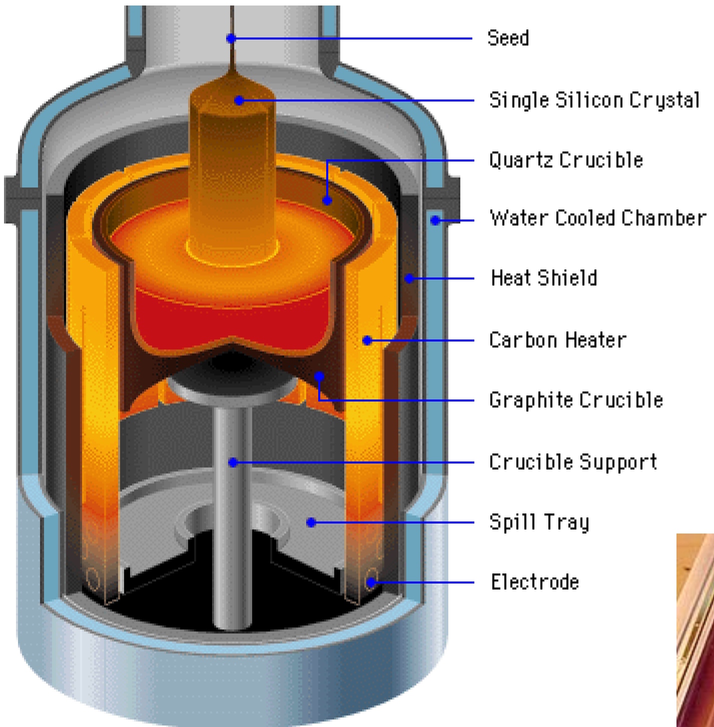
(a) (b)

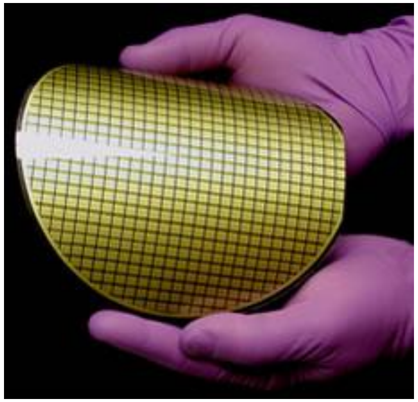
Figure 1.10

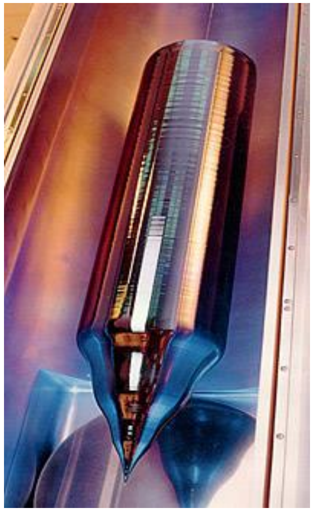
Pulling of a Si crystal from the melt (Czochralski method): (a) schematic diagram of the crystal growth process; (b) an 8-in. diameter, ⟨100⟩ oriented Si crystal being pulled from the melt.

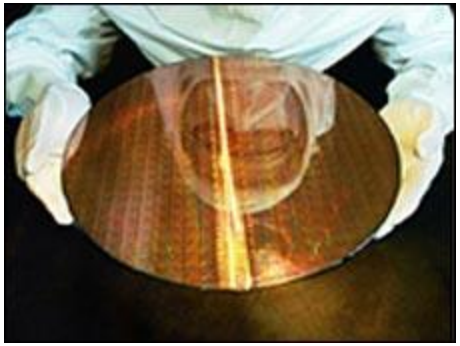
(Photograph courtesy of MEMC Electronics Intl.)

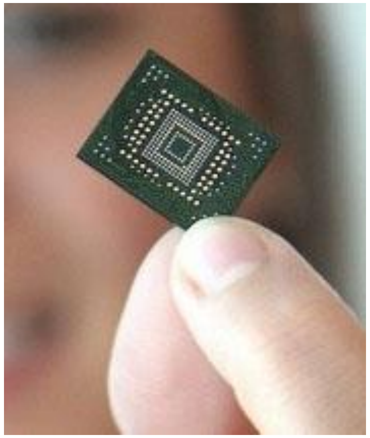
Crystal Growth Until Device Fabrication



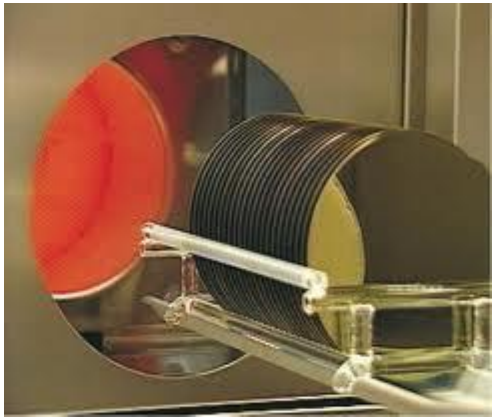


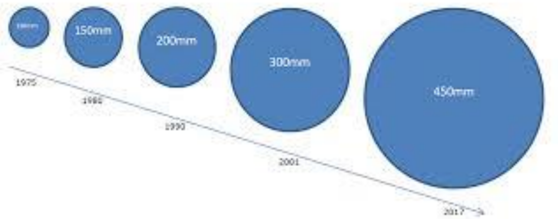


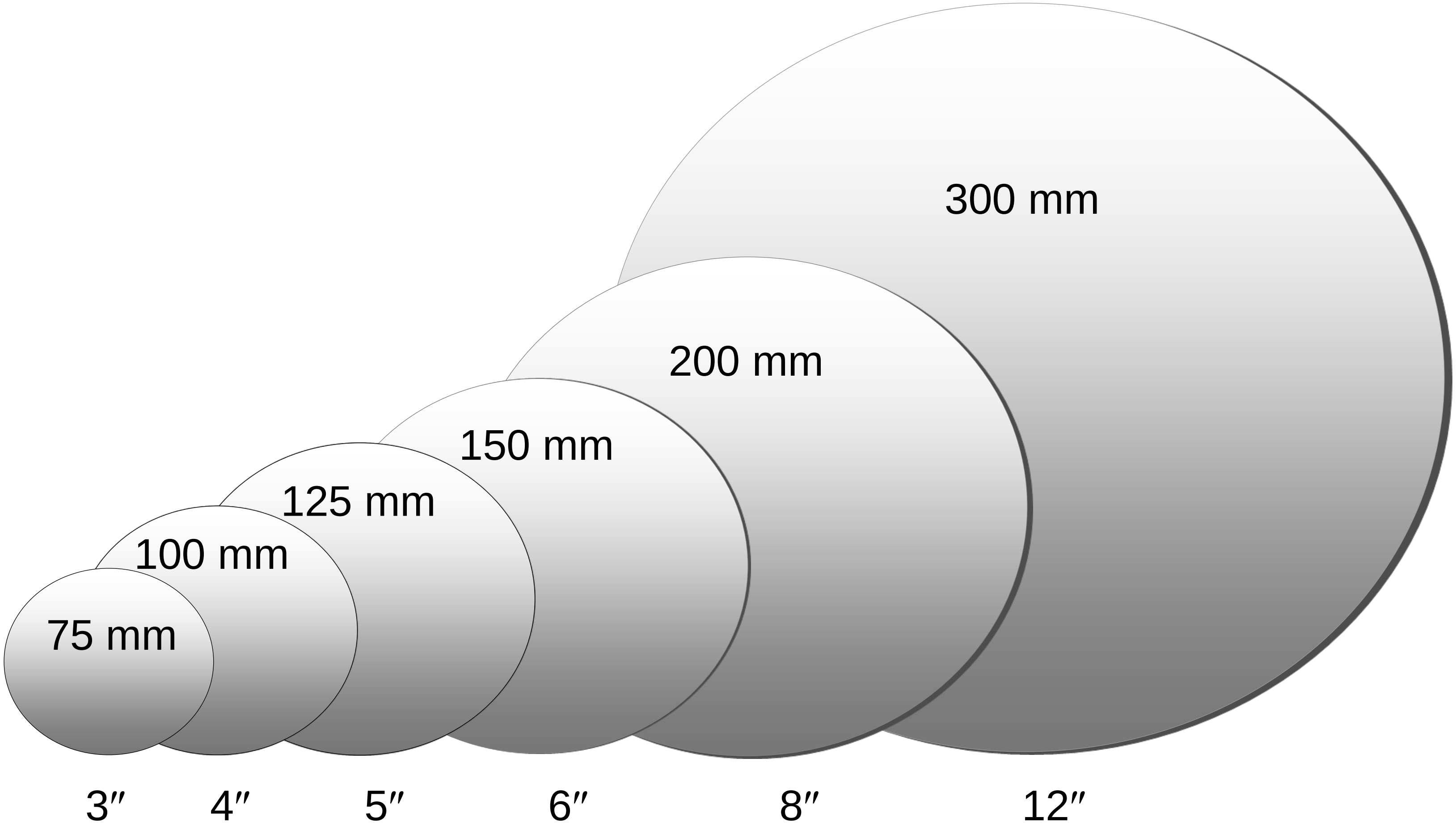




Metallurgical *grade silicon* - MGS
Electronic Grade Silicon - EGS

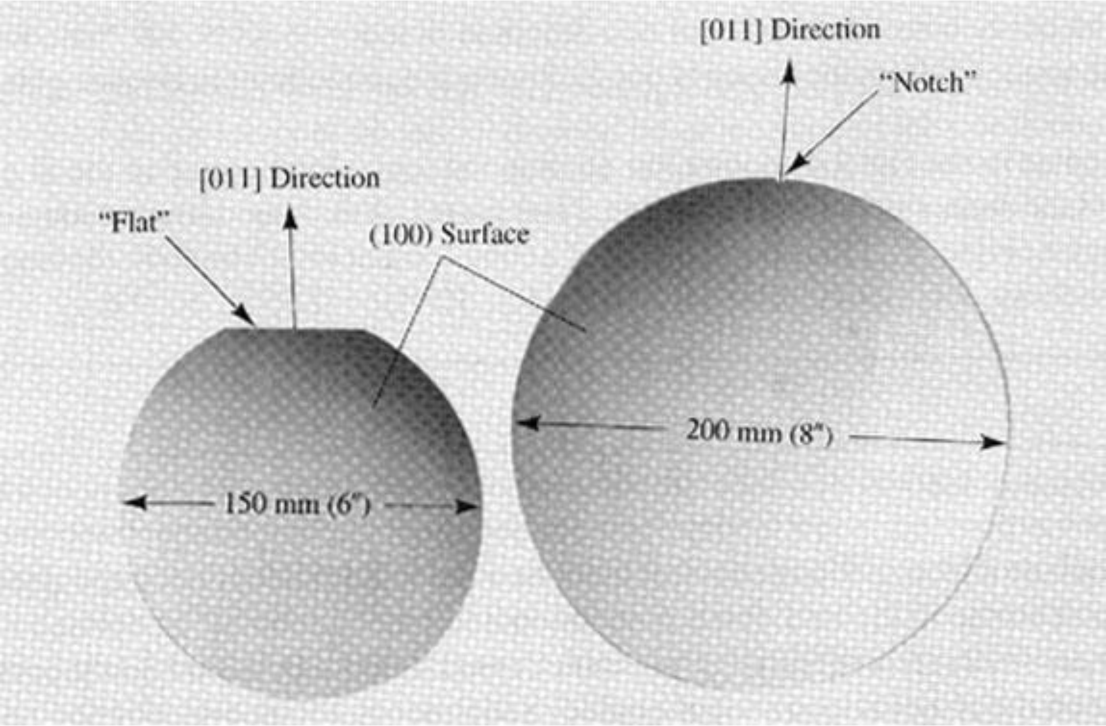





300 mm
200 mm
150 mm
125 mm
100 mm
75 mm
3″
4″
5″
6″
8″
12″

Crystallographic Planes of Si Wafers

- Silicon wafers are usually cut along a {100} plane with a flat or notch to orient the wafer during integrated-circuit fabrication.
- The facing surface is polished and etched yielding mirror-like finish.



Doping

- Impurities are added intentionally to the Si melt to change its electrical properties.
- At the solidifying interface between the melt and the solid, there will be a certain distribution of impurities between two phases.
- This property is measured by distribution coefficient k_d,

$$k_d = \frac{C_S}{C_L}$$

Crystallographic Planes of Si Wafers

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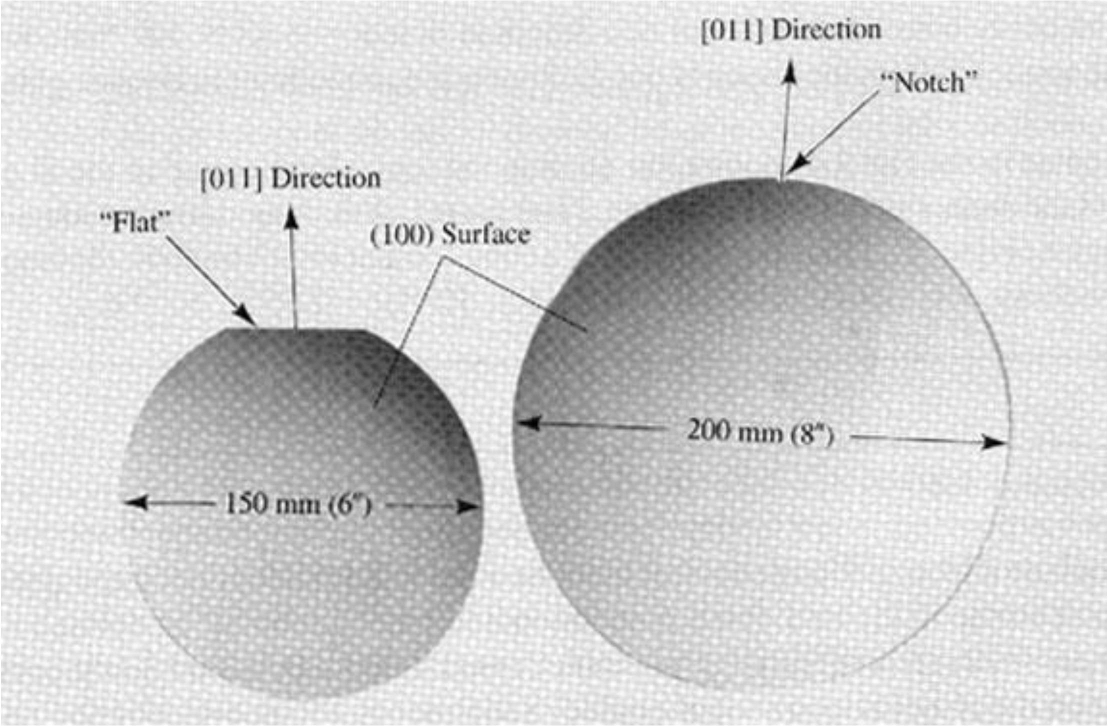
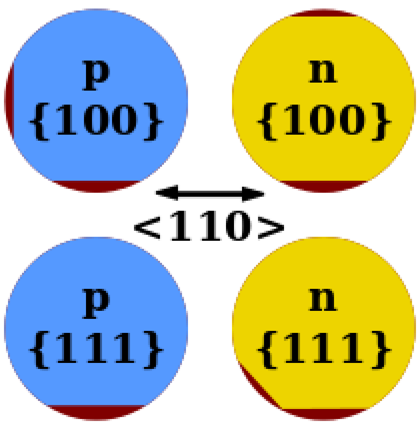
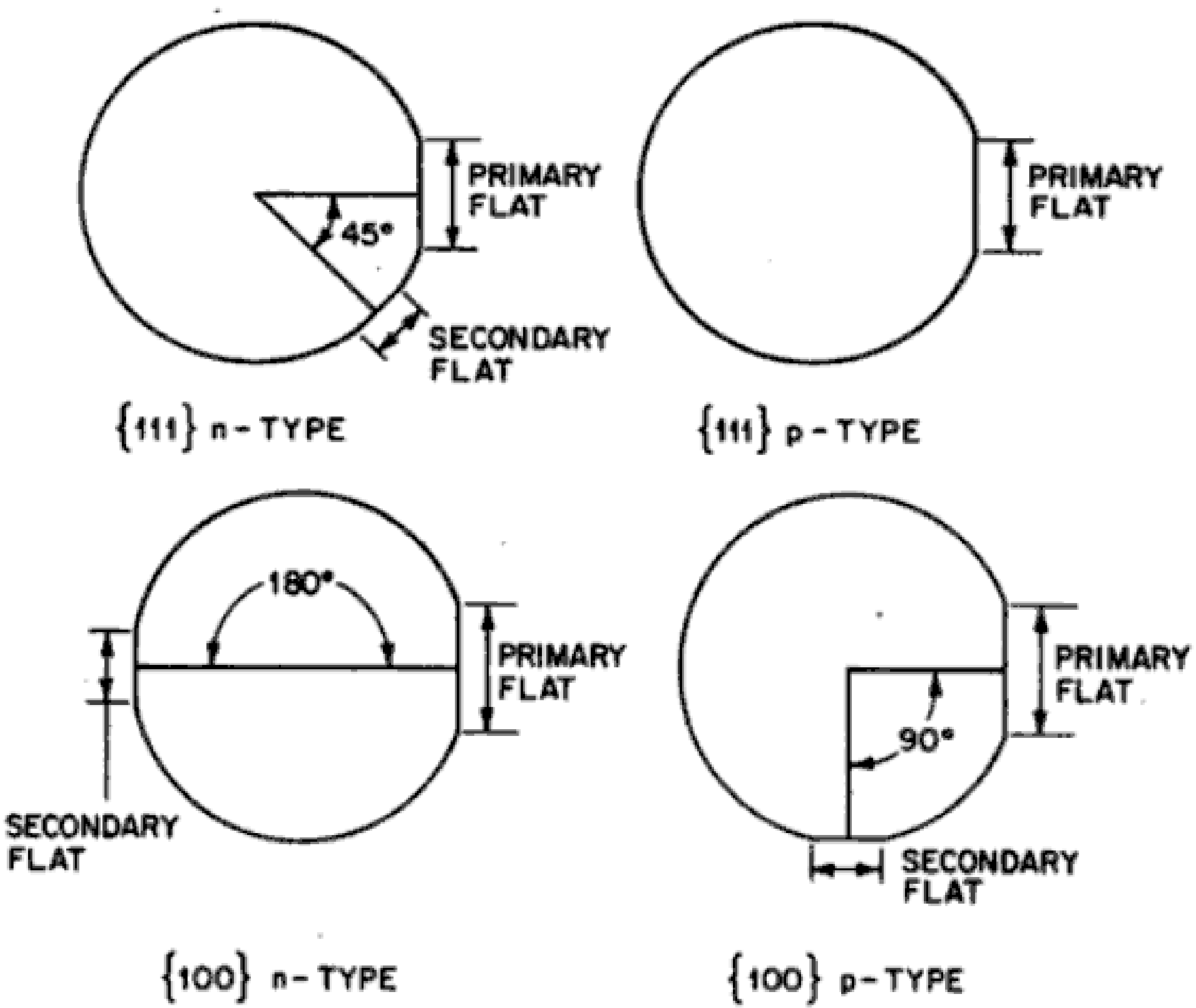


Identifying flats on Silicon wafers





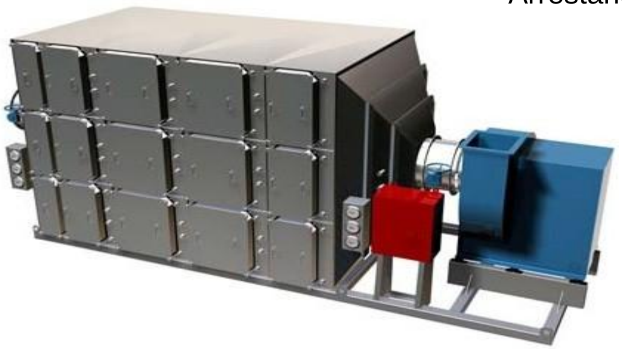
Clean Room Components

Clean room

HEPA Filter

High-Efficiency Particulate Arrestance (**HEPA**)

Laminar flow



Wafer Contaminations

Environmental Contaminations and precautions:

Air Filters : High Efficiency Particulate Air (HEPA) – made up of perforated fiber sheet.

Clean Room specifications:

Class X, where X denotes the total number of particles in cubic feet.

Nomenclature of Class X means that the 0.5 μm of particulate size should not be more than X number

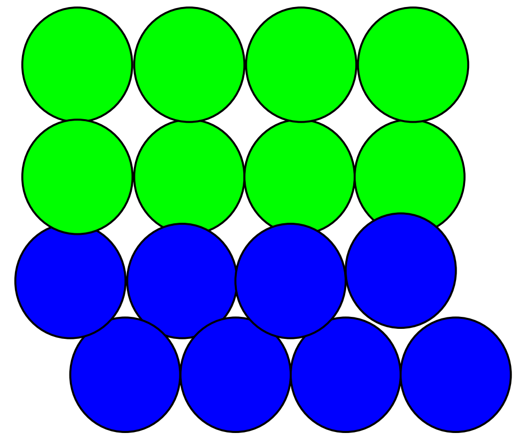
Epitaxy

- Epi means "upon"
- Taxis means "ordered"
- Epitaxy- A process used to grow a thin crystalline layer on a crystalline substrate
- The substrate wafer acts as a seed crystal
- Epitaxy - When a material is grown epitaxially on a substrate of the same material, such as silicon on silicon, the process is called homoepitaxy.
- If the layer and substrate are of different materials, such as $Al_xGa_{1-x}As$ on GaAs, the process is termed as heteroepitaxy. However, in heteroepitaxy the crystal structures of the layer and the substrate should be similar if crystalline growth is to be obtained.

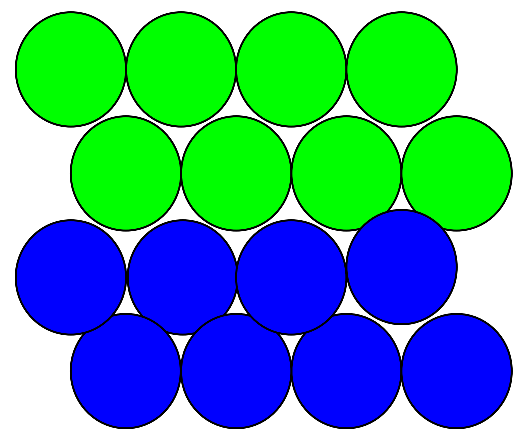
Epitaxial Growth

- Deposition of a layer on a substrate which matches the crystalline order of the substrate
- Homoepitaxy
  - Growth of a layer of the same material as the substrate
  - Si on Si
- Heteroepitaxy
  - Growth of a layer of a different material than the substrate
  - GaAs on Si

Ordered, crystalline growth; NOT epitaxial



Epitaxial growth:



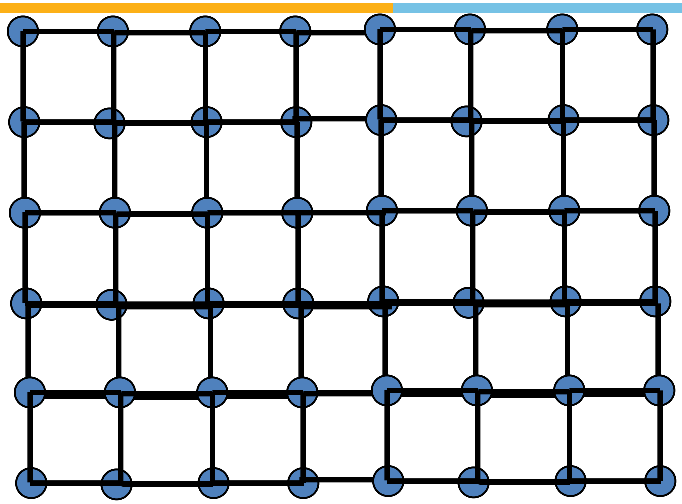
Properties of Epitaxial Layer

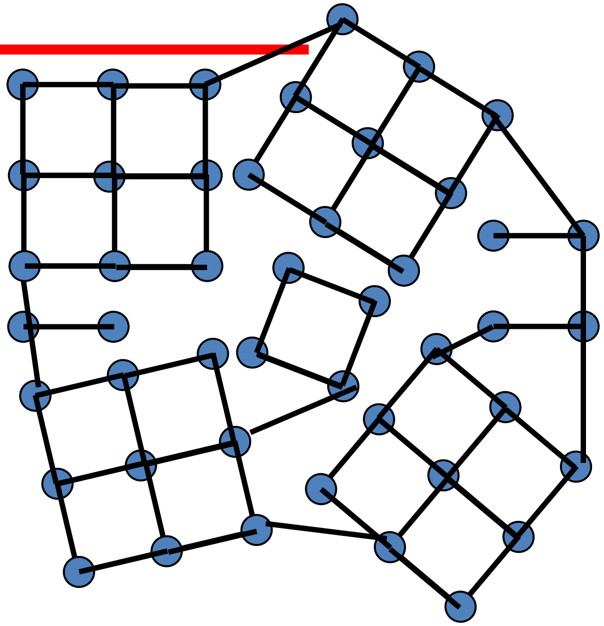
- Crystallographic structure of film reproduces that of substrate
- Substrate defects reproduced in epi layer
- Electrical parameters of epi layer independent of substrate
- Dopant concentration of substrate cannot be reduced
- Epitaxial layer with less dopant can be deposited
- Epitaxial layer can be chemically purer than substrate
- Abrupt interfaces with appropriate methods

Methods of Epitaxy

- Epitaxial silicon is usually grown using Vapor Phase Epitaxy (VPE), a modification of Chemical Vapor Deposition
- Molecular-beam and liquid-phase epitaxy (MBE and (LPE) are also used, mainly for compound semiconductors.
- Metal Organic CVD(MOCVD)

What makes a crystal?





-Crystals possess long-range order,

-We may have instead poly-crystalline or even amorphous material.

Crystal structure and defects

Crystal Structure: Crystal can be grown on 111, 100, 110 planes

Point Defects:

- Point Defects
- Line Defect (dislocation)
- Area (planar) defects
- Volume Defects

Crystal structure and defects

Point Defects:

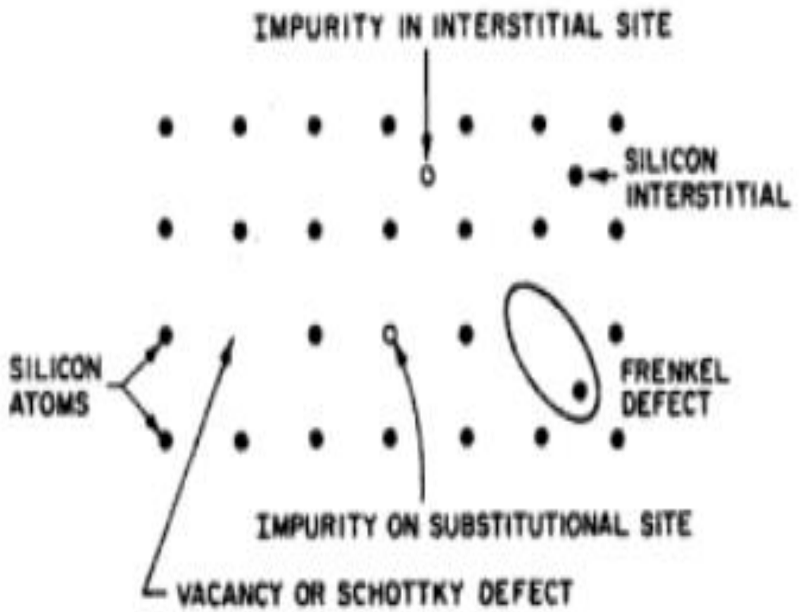


FIGURE 5
The location and types of point defects in a simple lattice.

Crystal structure and defects

Dislocations:

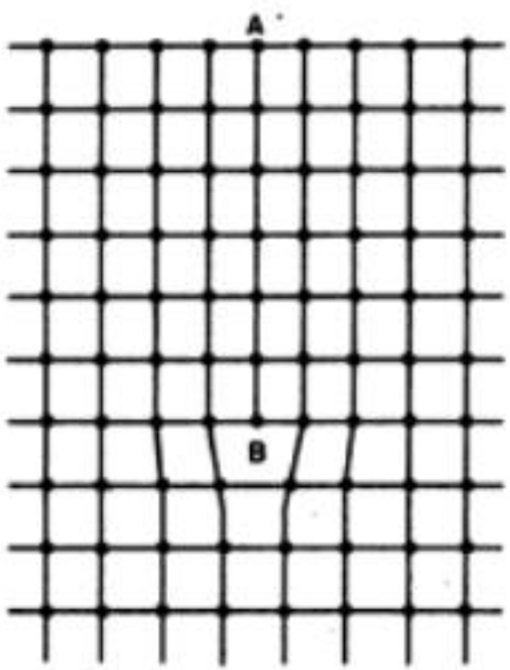


FIGURE 6
An edge dislocation in a cubic lattice created by an extra plane of atoms. The line of the dislocation is perpendicular to the page.

Crystal structure and defects

Area (planar) Defects: Two area defects are twins and grain boundaries. The defect appears during crystal growth, but such crystals are simply discarded.

Basic Process Steps for Wafer Preparation