Maicon Schneider Cardoso

Pelotas/RS, Brazil

maiconsc.github.io

maiconscardosoo@gmail.com

maiconscardoso

SUMMARY

I received the Ph.D, M.Sc., and B.Sc. degrees in Computer Science from the Federal University of Pelotas (UFPel) in 2022, 2017, and 2014, respectively, and the B.Eng. in Electrical Engineering from the Federal Institute Sul-rio-grandense (IFSul) in 2018.
My main research interests include the development of EDA solutions for conventional and emerging technologies.

EDUCATION

2017 – 2022

Doctor of Philosophy (Ph.D.), Computer Science.

Federal University of Pelotas (UFPel).

- Advisor: Prof. Felipe Marques.
- Ph.D. thesis: Cell Implementation Through Boolean Satisfiability for Conventional and Emerging Technologies.

2015 – 2017

Master of Science (M.Sc.), Computer Science.

Federal University of Pelotas (UFPel).

- Advisor: Prof. Felipe Marques.
- Master thesis: Design and Evaluation of Complex Logic Gates Without Topological Constraints (in Portuguese: "Projeto e Avaliação de Portas Lógicas Complexas sem Restrições Topológicas").

2009 – 2014

Bachelor of Science (B.Sc.), Computer Science.

Federal University of Pelotas (UFPel).

- Advisor: Prof. Felipe Marques.
- Final project: Placement and Routing of Non-Series-Parallel Transistor Networks (in Portuguese: "Posicionamento e Roteamento de Redes de Transistores Não-Série-Paralelo").

2009 – 2018

Bachelor of Engineering (B.Eng.), Electrical Engineering.

Federal Institute Sul-rio-grandense (IFSul).

- Advisor: Prof. Júlio César Ruzicki.
- Final project: Libra: a Methodology for the Automatic Design of SCCGs (in Portuguese: "Libra: uma Metodologia de Desenvolvimento Automático de SCCGs").

2007 – 2009

Technical, Electronics.

Federal Institute Sul-rio-grandense (IFSul).

WORK EXPERIENCE

2021 – present

Professor.

Federal Institute Sul-rio-grandense (IFSul).
Electronics (technical college-level course).

- Classes: computer architecture and digital electronics.

2017 – 2021

Ph.D. Student Researcher.

Federal University of Pelotas (UFPel).
Group of Architectures and Integrated Circuits (GACI).

2019 – 2020

Ph.D. Visiting Research Scholar.

Polytechnic University of Catalonia (UPC).
Supervisor: Prof. Jordi Cortadella.

2015 – 2017 M.Sc. Student Researcher.
Federal University of Pelotas (UFPel).
Group of Architectures and Integrated Circuits (GACI).

2013 – 2014 Undergraduate Researcher.
Federal University of Pelotas (UFPel).
Group of Architectures and Integrated Circuits (GACI).

2012 – 2013 Undergraduate Information Systems Technician.
Federal University of Pelotas (UFPel).
Center of Informatics (CI).

2010 – 2011 Undergraduate Hardware Technician.
Federal University of Pelotas (UFPel).
UFPel Computer Science and Computer Engineering Laboratories.

PUBLICATIONS

[1] Cardoso, M., Bubolz, A., Cortadella, J., Rosa Jr., L. and Marques, F. *Transistor Placement for Automatic Cell Synthesis through Boolean Satisfiability*. In: Proceedings of the 53th IEEE International Symposium of Circuits and Systems (53th IEEE ISCAS), 2020, Seville.

[2] Cardoso, M., Smaniotto, G., Bubolz, A., Moreira, M., Rosa Jr., L. and Marques, F. *Libra: an Automatic Design Methodology for CMOS Complex Gates*. IEEE Transactions on Circuits and Systems II-Express Briefs, v. 65, 2018.

[3] Cardoso, M., Smaniotto, G., Bubolz, A., Rosa Jr., L. and Marques, F. *Area-Aware Design of Static CMOS Complex Gates*. In: Proceedings of the 16th IEEE International New Circuits and Systems Conference (16th IEEE NEWCAS), 2018, Montreal.

[4] Smaniotto, G., Zanandrea, R., Cardoso, M., Souza, R., Moreira, M., Marques, F. and Rosa Jr., L. *A post-processing methodology to improve the automatic design of CMOS gates at layout-level*. In: Proceedings of the 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS) (24th IEEE ICECS), 2017, Batumi.

[5] Ávila, C., Cavalheiro, S., Bordini, A., Marques, M., Cardoso, M. and Feijó, G. *Computational Thinking Assessment Methodologies: a Systematic Review* In: Proceedings of the XXVIII Brazilian Symposium on Informatics in Education (XVIII SBIE), 2017, Recife.

[6] Cardoso, M., Smaniotto, G., Machado, J., Moreira, M., Rosa Jr., L. and Marques, F. *Transistor Placement Strategies for Non-Series-Parallel Cells*. In: Proceedings of the 60th IEEE International Midwest Symposium on Circuits and Systems (60th IEEE MWSCAS), 2017, Boston.

[7] Smaniotto, G., Zanandrea, R., Cardoso, M., Souza, R., Moreira, M., Marques, F. and Rosa Jr., L. *Post-Processing of Supergate Networks Aiming Cell Layout Optimization*. In: Proceedings of the 50th IEEE International Symposium of Circuits and Systems (50th IEEE ISCAS), 2017, Baltimore.

[8] Cardoso, M., Smaniotto, G., Zanandrea, R., Souza, R., Rosa Jr., L. and Marques, F. *Physical Design of Supergate Cells Aiming Geometrical Optimizations*. In: Proceedings of the 59th IEEE International Midwest Symposium on Circuits and Systems (59th IEEE MWSCAS), 2016, Abu Dhabi.

[9] Cardoso, M., Zanandrea, R., Souza, R., Machado, J., Rosa Jr., L. and Marques, F. *Topological Characteristics of Logic Networks Generated by a Graph-based Methodology*. In: Proceedings of the 7th IEEE Latin American Symposium on Circuits & Systems (7th IEEE LASCAS), 2016, Florianópolis.

[10] Cardoso, M., Rosa Jr., L. and Marques, F. *Evaluating Geometric Aspects of Non-Series-Parallel Cells*. In: Proceedings of the 28th Symposium on Integrated Circuits and Systems Design (28th SBCCI), 2015, Salvador.

SKILLS

Programming Python, C/C++, Java, Git, Latex.

Languages Portuguese (native), English, Spanish (Castilian), and Catalan (beginner).