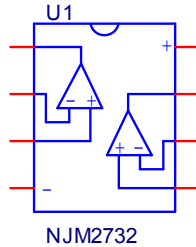# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER:NJM2732
MANUFACTURER: NEW JAPAN RADIO CO.,LTD

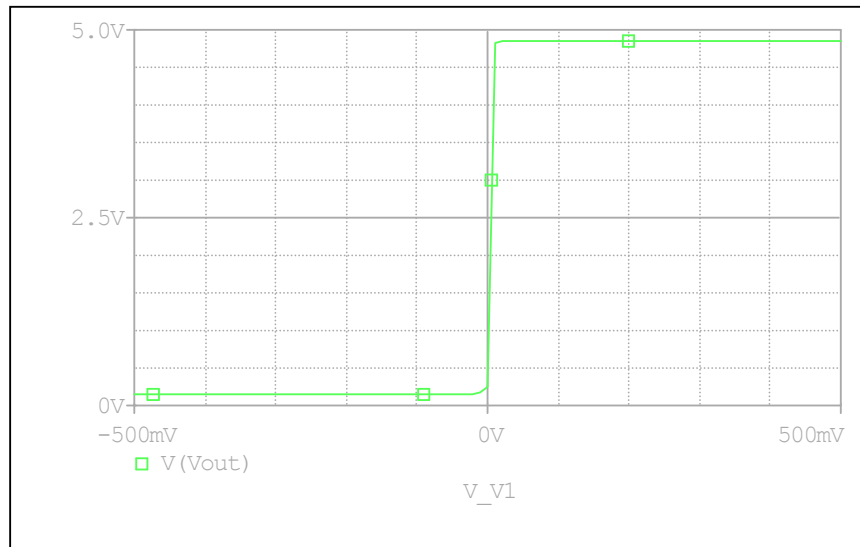Bee Technologies Inc.

Spice Model

U1

NJM2732

```
*$
*PART NUMBER: NJM2732
*MANUFACTURER: NEW JAPAN RADIO
*OPAMP
*All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM2732 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X_U1    +IN1 -IN1 V+ V- OUT1 NJM2732_S
X_U2    +IN2 -IN2 V+ V- OUT2 NJM2732_S
.ends njm2732
.subckt njm2732_S  1 2 3 4 5
 c1   11 12 8.6603E-12
 c2    6  7 30.000E-12
 dc    5 53 dy
 de   54  5 dy
 dlp  90 91 dx
 dln  92 90 dx
 dp    4  3 dx
 egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
 fb    7 99 poly(5) vb vc ve vlp vln 0 3.4037E6 -1E3 1E3 3E6 -3E6
 ga    6  0 11 12 215.07E-6
 gcm   0  6 10 99 66.995E-9
 iee   3 10 dc 12.129E-6
 hlim 90  0 vlim 1K
 q1   11  2 13 qx1
 q2   12  1 14 qx2
 r2    6  9 100.00E3
 rc1   4 11 4.6496E3
 rc2   4 12 4.6496E3
 re1  13 10 346.78
 re2  14 10 346.78
 ree  10 99 16.489E6
 ro1   8  5 50
 ro2   7 99 25
 rp    3  4 50.006
 vb    9  0 dc 0
 vc    3 53 dc .945
 ve   54  4 dc .9488
 vlim  7  8 dc 0
 vlp  91  0 dc 20
 vln   0 92 dc 20
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=112.24)
.model qx2 PNP(Is=850.7231E-18 Bf=131.31)
.ends
*$
```
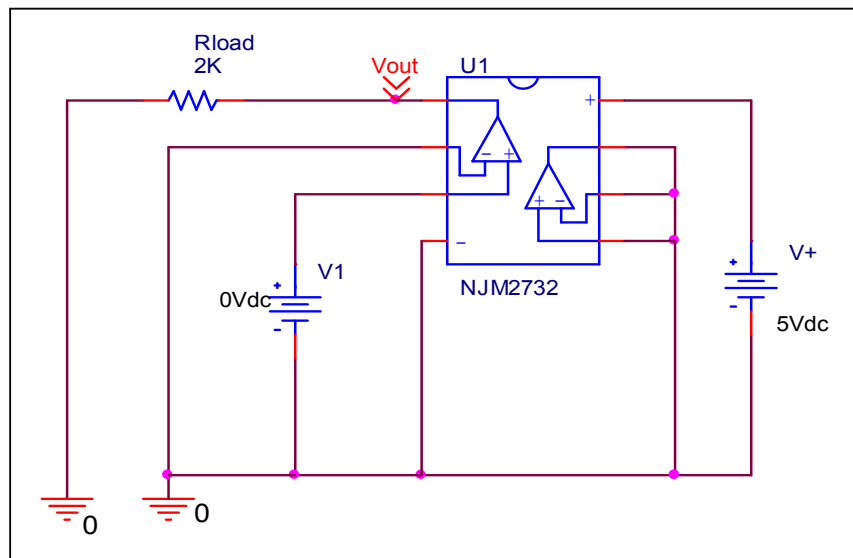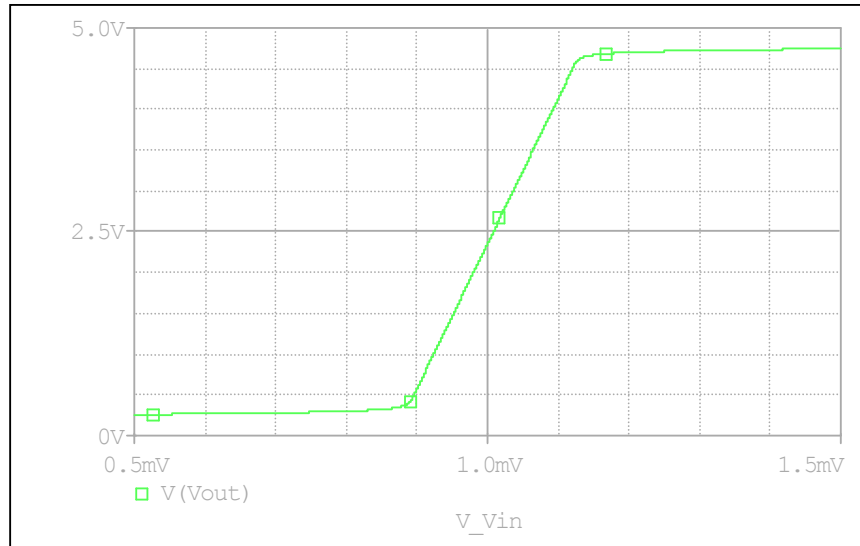
Output Voltage Swing

Output Voltage Swing	Measurement	Simulation	%Error
VOH (V)	4.85	4.8504	0.008
VOL (V)	0.15	0.150	0

Input Offset Voltage

Simulation result

Evaluation circuit

VOFF = 0
VAMPL = 0
FREQ = 0
AC = 0
DC = 0

Rload
2k

Vout

U1

NJM2732

Vin

V+

5Vdc

0   0
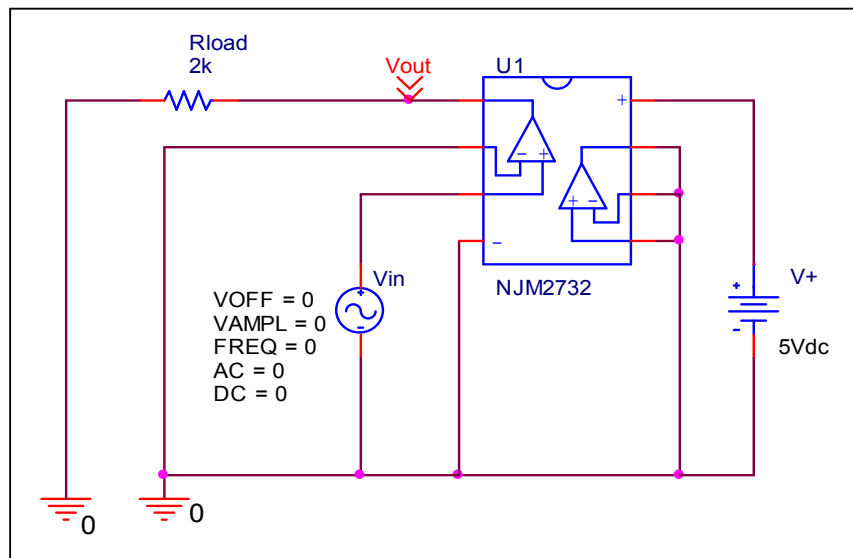
Comparison table

	Measurement	Simulation	%Error
Vos (mV)	1	1.0082	0.82

Slew Rate

V1 = 0
V2 = 5
TD = 10u
TR = 10n
TF = 10n
PW = 50u
PER = 500u

Rload
2k

Vout

U1

NJM2732

Vi

V+

5Vdc
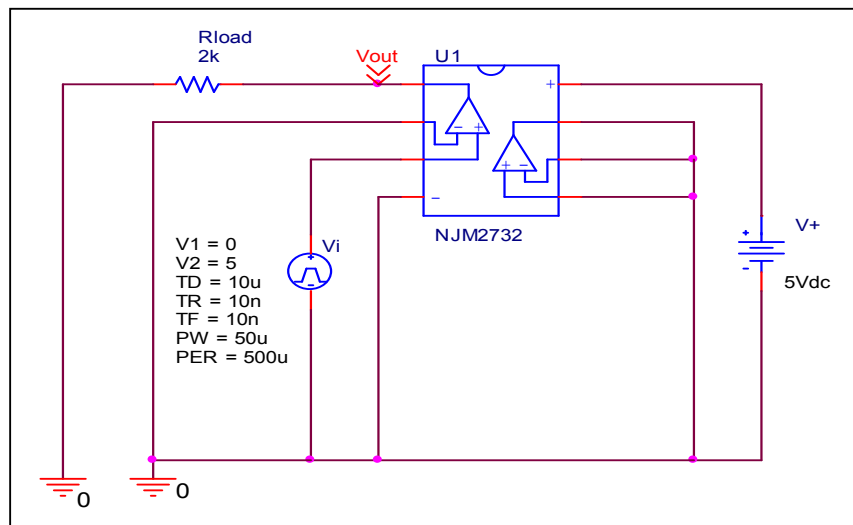
	Measurement	Simulation	%Error
Slew Rate(v/us)	0.4	0.398	-0.5

Input current
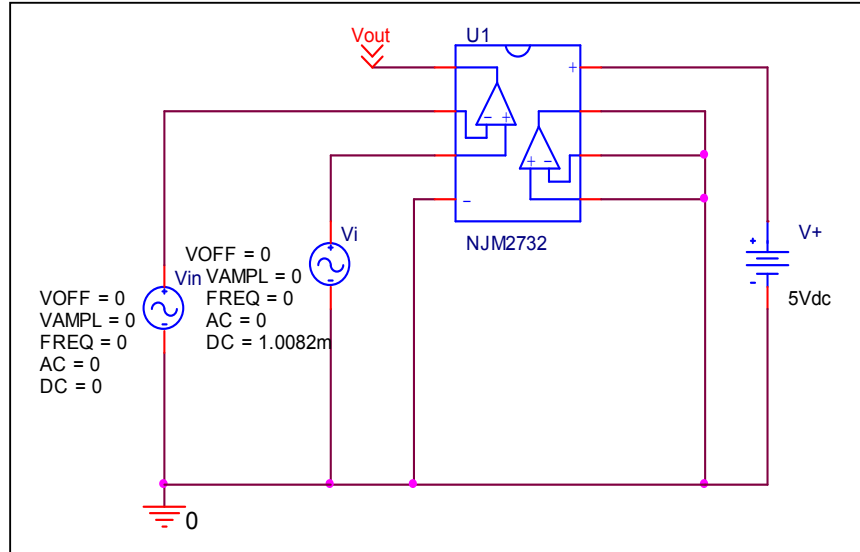
	Measurement	Simulation	%Error
Ib(nA)	50	50.061	0.122
Iio(nA)	5	5.0025	0.050

Open Loop Voltage Gain vs. Frequency

Simulation result
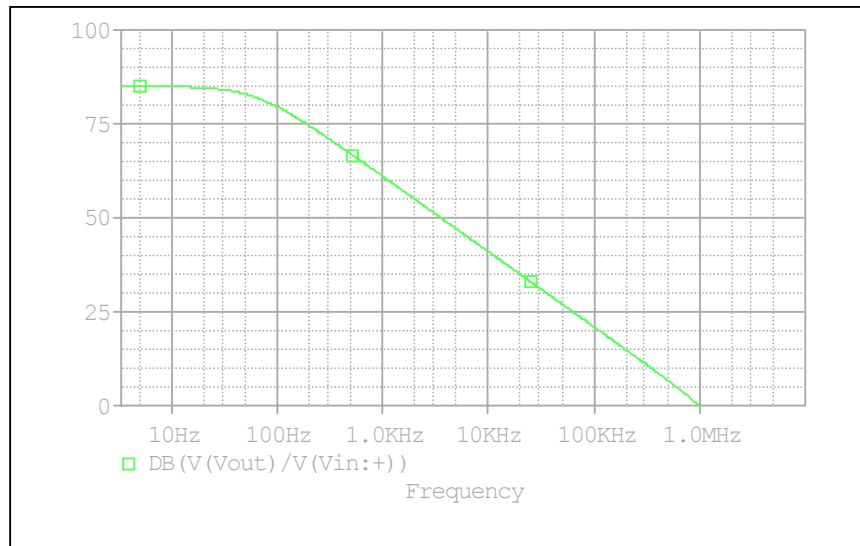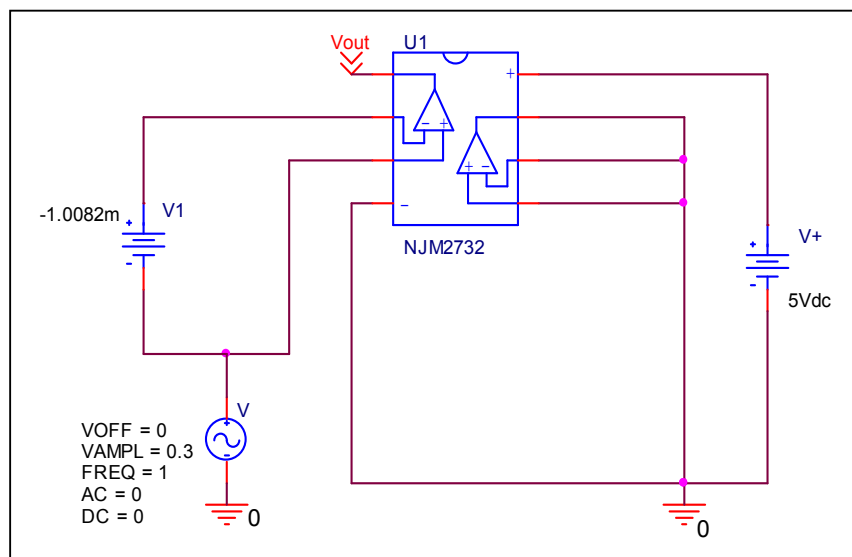

Evaluation circuit
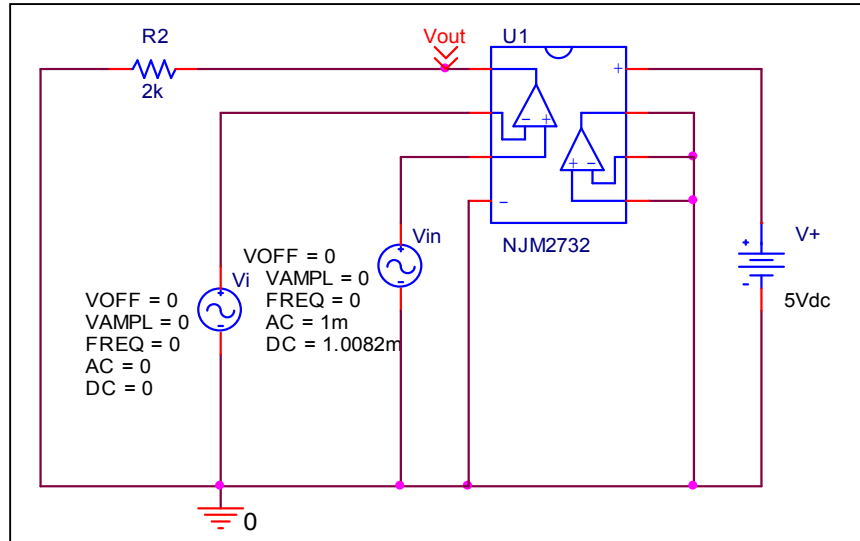
Comparison table

	Measurement	Simulation	%Error
f-0dB(MHz)	1	1	0
Av-dc	85	84.992	-0.009

Common-Mode Rejection Voltage gain
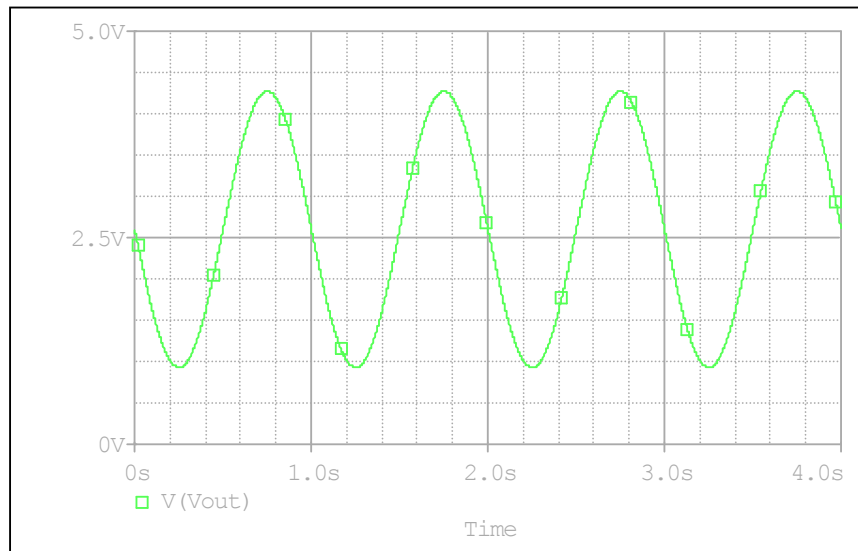
Evaluation circuit

CMRR=20*LOG(17766.423/(3.3913 /0.6)) = 69.948 dB

Comparison table

	Measurement	Simulation	%Error
CMRR(dB)	70	69.948	-0.074

Remark Output Voltage Swing

Before
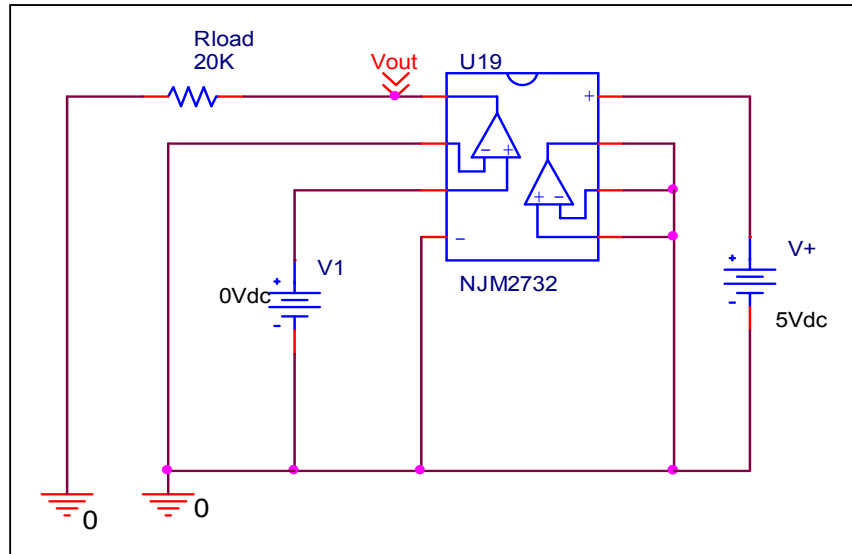
After
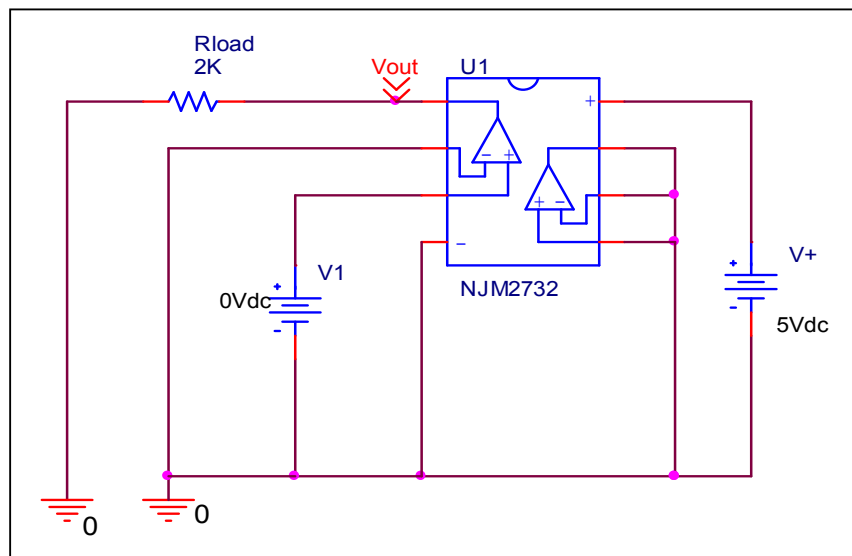
Remark Input Offset Voltage

Before

Rload
20k

Vout

U14

NJM2732

VOFF = 0
VAMPL = 0
FREQ = 0
AC = 0
DC = 0

Vin

V+

5Vdc

0

0

After

Rload
2k

Vout

U1

NJM2732

VOFF = 0
VAMPL = 0
FREQ = 0
AC = 0
DC = 0

Vin

V+

5Vdc

0

0
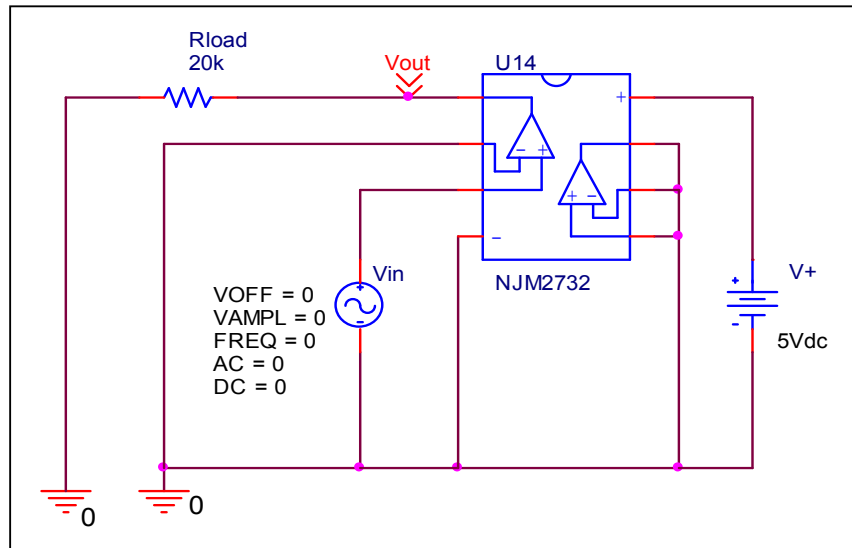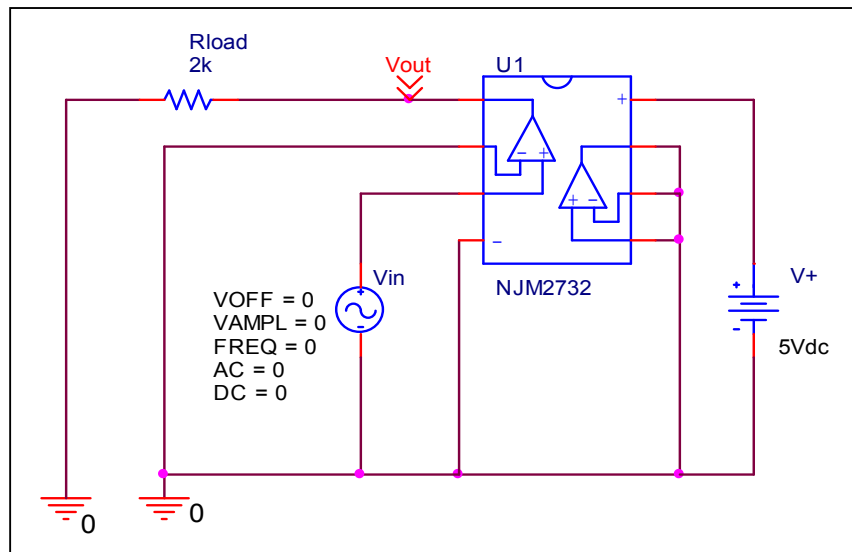
Remark Slew Rate
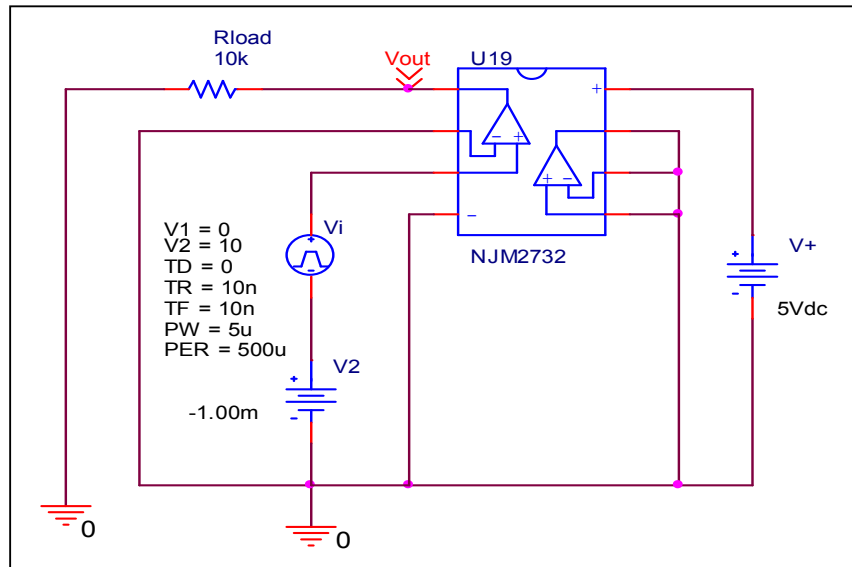
Before

After
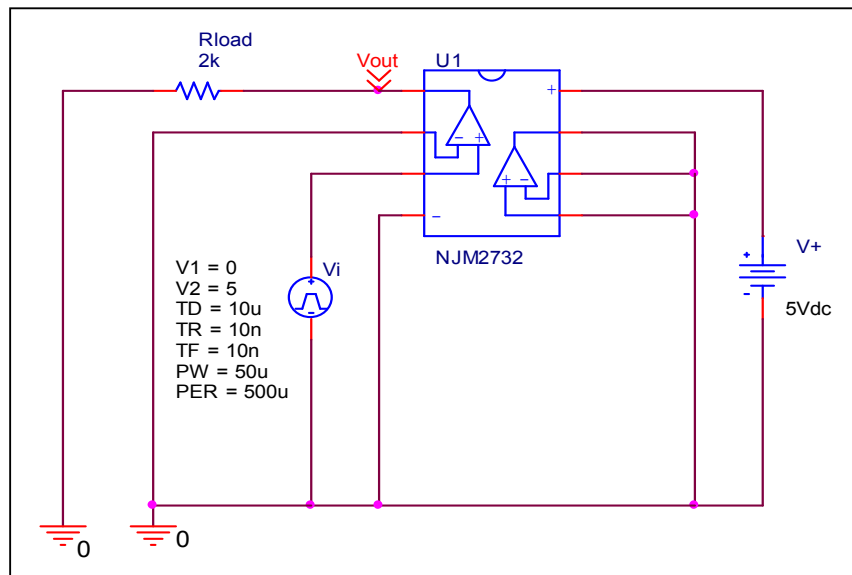
Remark Input current

Before

Rload
10k

Vout

U18

+

NJM2732

Vin

VOFF = -1.00m
Vi VAMPL = 0
FREQ = 0
AC = 0
DC = 0

VOFF = 0
VAMPL = 0
FREQ = 0
AC = 0
DC = 0

V+

5Vdc

0

0

After

Vout

U1

+

NJM2732

Vi

VOFF = 0
Vin VAMPL = 0
FREQ = 0
AC = 0
DC = 1.0082m

VOFF = 0
VAMPL = 0
FREQ = 0
AC = 0
DC = 0

V+

5Vdc

0
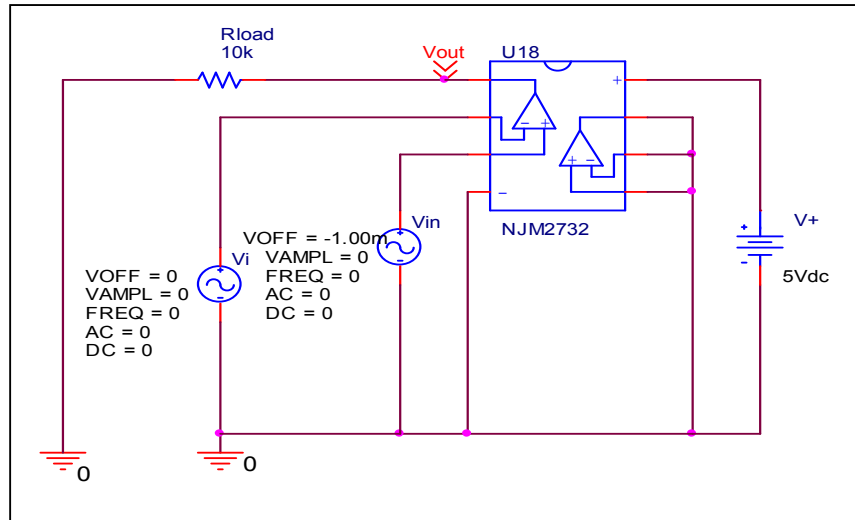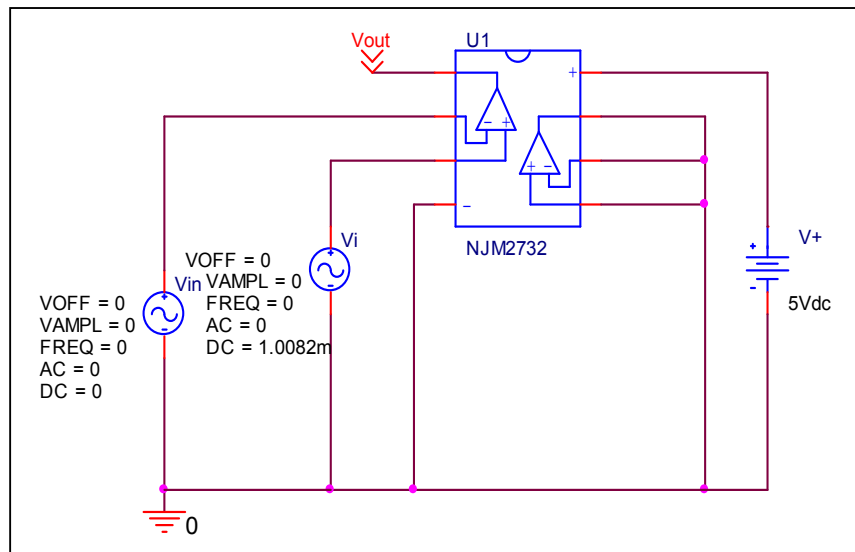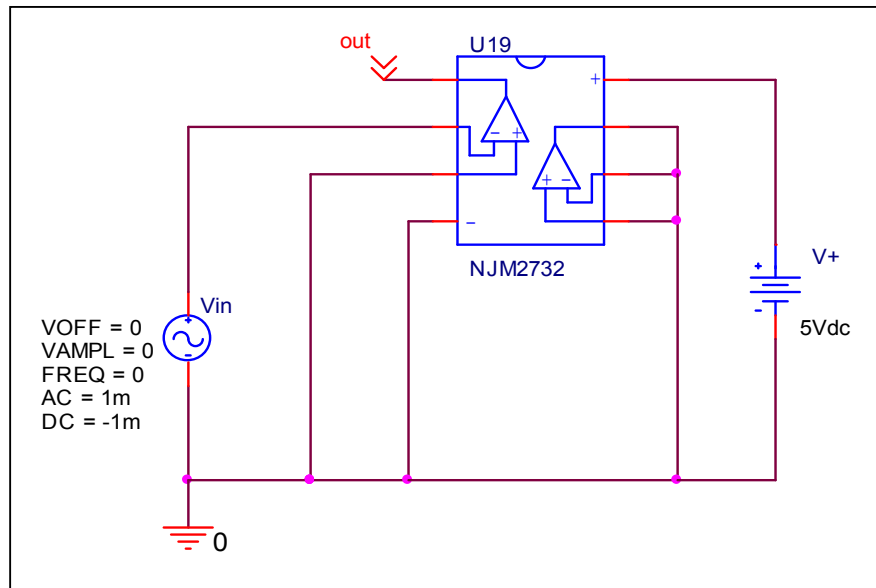
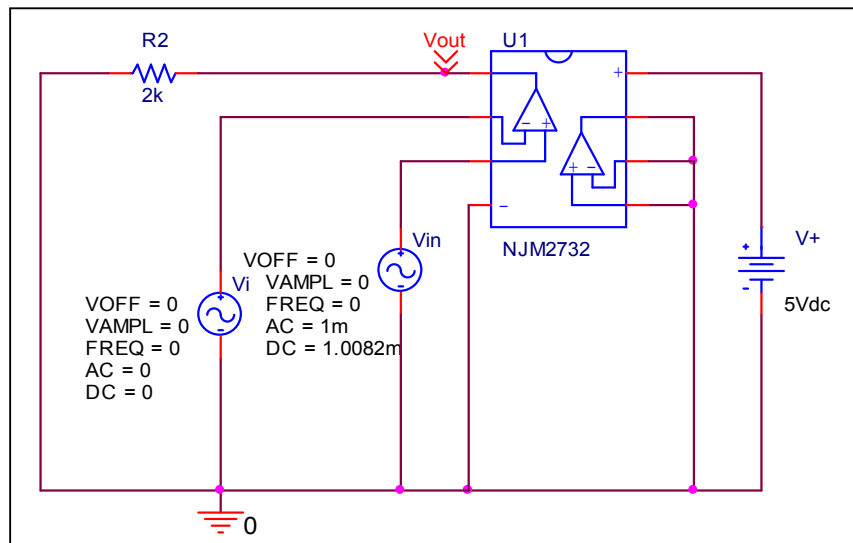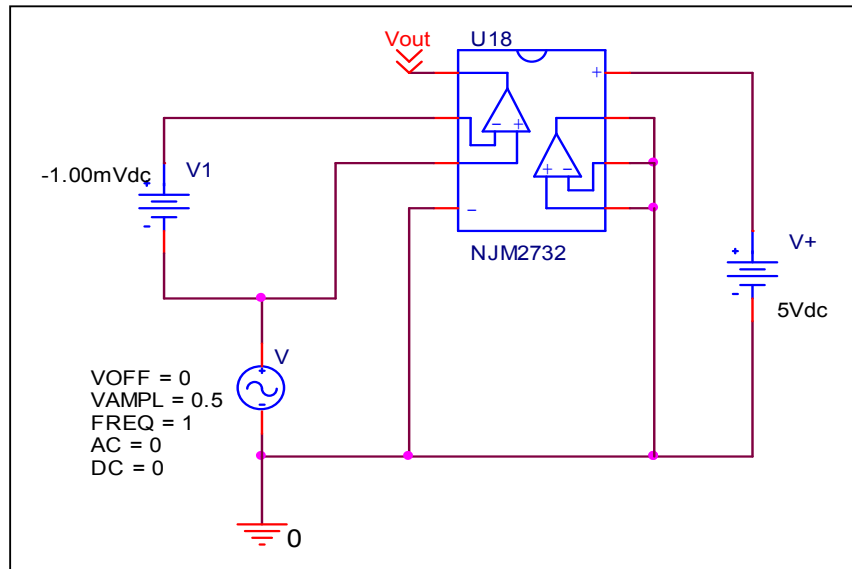# Remark Open Loop Voltage Gain vs. Frequency

Before

After

Remark Common-Mode Rejection Voltage gain

Before

After