Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER (CMOS)

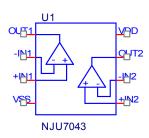
PART NUMBER: NJU7043

MANUFACTURER: NEW JAPAN RADIO



Bee Technologies Inc.

Spice Model



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*$
*PART NUMBER: NJU7043
*MANUFACTURER: NEW JAPAN RADIO
*CMOS OPAMP
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.SUBCKT nju7043 OUT1 -IN1 +IN1 VSS +IN2 -IN2 OUT2 VDD
X U1 +IN1 VSS -IN1 OUT1 VDD nju7043 s
X_U2 +IN2 VSS -IN2 OUT2 VDD nju7043_s
.ENDS nju7043
.SUBCKT nju7043 s IN+ VSS IN- OUT VDD
M1
           2 IN- 3 VDD MbreakPD3
M2
           2 IN+ 4 VDD MbreakPD2
М3
           VDD 1 2 VDD MbreakPD4
M4
           VDD 1 5 VDD MbreakPD
M5
           VDD 1 6 VDD MbreakPD
           VDD 1 1 VDD MbreakPD
M6
M7
           5 5 VSS VSS MbreakND
           5 4 VSS VSS MbreakND
M8
M9
           3 3 IN1 VSS MbreakND4
M10
           4 3 IN2 VSS MbreakND1
M11
           1 6 11 11 MbreakND
M12
           6 6 VSS VSS MbreakND3
           7 5 VSS VSS MbreakND5
M13
M14
           VDD 7 7 VDD MbreakPD
M15
           VDD 7 OUT VDD MbreakPD1
M16
           OUT 4 VSS VSS MbreakND2
C1
          OUT 4 90p
C2
          OUT 6 7.2p
R1
           11 VSS 1.522k
R2
          IN1 VSS 2.0k
R3
          IN2 VSS 2.423k
```

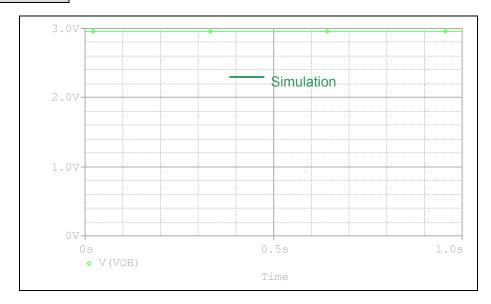
```
11
         0 IN- 0.505p
12
         0 IN+ 1.5p
X U1
          VSS 3 DbreakZ
X U2
           VSS 4 DbreakZ
.model MbreakND NMOS (LEVEL=3 L=6u W=3.2m VTO=0.2 RS=10E-3
+ RD=10E-3 RDS=1.00E6 TOX=2.00E-6 RG=5 RB=1.0000E-3 KP=1E-6)
.model MbreakND1 NMOS (LEVEL=3 L=6u W=0.165 VTO=0.2 RS=10E-3
+ RD=10E-3 RDS=1.00E6 TOX=2.00E-6 RG=5 RB=1.0000E-3 KP=1E-6)
.model MbreakND2 NMOS (LEVEL=3 L=6u W=27.4m VTO=0.2 RS=10E-3
+ RD=10E-3 RDS=1.00E6 TOX=2.00E-6 CGSO=1E-10 CGDO=300e-12
+ CBD=45.0E-12 RG=5 RB=1.0000E-3 KP=1E-6)
.model MbreakND3 NMOS (LEVEL=3 W=3.2m L=6u VTO=0.1 RS=10E-3
+ RD=10E-3 RDS=1E6 TOX=2.00E-6 RG=5 RB=1.00E-3 KP=1E-6)
.model MbreakND4 NMOS (LEVEL=3 L=6u W=0.165 VTO=0.2 RS=10E-3
+ RD=10E-3 RDS=1.00E6 TOX=2.00E-6 CGSO=1E-8 CBD=100.00E-12
+ RG=5 RB=1.0000E-3 KP=1E-6)
.model MbreakND5 NMOS (LEVEL=3 L=6u W=0.165 VTO=0.2 RS=10E-3
+ RD=10E-3 RDS=1.00E6 TOX=2.00E-6 RG=5 RB=1.0000E-3 KP=1E-6)
.model MbreakPD PMOS (LEVEL=3 L=6u W=0.23 VTO=-0.1 RS=10.0E-3
+ RD=10E-3 RDS=1.00E6 TOX=2.00E-6 RG=5 RB=1.0000E-3 KP=1E-6)
.model MbreakPD1 PMOS (LEVEL=3 L=6u W=0.4 VTO=-0.1 RS=10.0E-3
+ RD=10E-3 RDS=1E6 TOX=2E-6 CGDO=1.9E-8 RG=5 RB=1E-3 KP=1E-6)
.MODEL MbreakPD2 PMOS (LEVEL=3 L=6u W=0.00175 VTO=-.34 RS=10E-3
+ RD=10E-3 RDS=2.1E6 TOX=2E-6 CBD=10E-12 RG=5 RB=1E-3 KP=1E-5)
.MODEL MbreakPD3 PMOS (LEVEL=3 L=6u W=0.00177 VTO=-.34 RS=10E-3
+ RD=10E-3 RDS=1.0E6 TOX=2.0E-6 RG=5 RB=1.0000E-3 KP=1E-5)
.model MbreakPD4 PMOS (LEVEL=3 W=.23 L=0.3u VTO=-0.1 RS=10E-3
+ RD=10E-3 RDS=1E6 TOX=2E-6 CGDO=1.2e-10 RG=5 RB=1E-3 KP=1E-6)
.ENDS nju7043 s
.SUBCKT DbreakZ A K
D1 A K DF
DZ A2 A DR
VZ K A2 1
.MODEL DF D
.MODEL DR D
.ENDS DbreakZ
*$
```

MOSFET MODEL

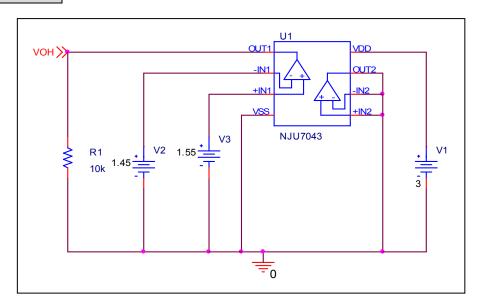
Pspice model	Model description		
parameter	·		
LEVEL			
L	Channel Length		
W	Channel Width		
KP	Transconductance		
RS	Source Ohmic Resistance		
RD	Ohmic Drain Resistance		
VTO	Zero-bias Threshold Voltage		
RDS	Drain-Source Shunt Resistance		
TOX	Gate Oxide Thickness		
CGSO	Zero-bias Gate-Source Capacitance		
CGDO	Zero-bias Gate-Drain Capacitance		
CBD	Zero-bias Bulk-Drain Junction Capacitance		
MJ	Bulk Junction Grading Coefficient		
PB	Bulk Junction Potential		
FC	Bulk Junction Forward-bias Capacitance Coefficient		
RG	Gate Ohmic Resistance		
IS	Bulk Junction Saturation Current		
N	Bulk Junction Emission Coefficient		
RB	Bulk Series Resistance		
PHI	Surface Inversion Potential		
GAMMA	Body-effect Parameter		
DELTA	Width effect on Threshold Voltage		
ETA	Static Feedback on Threshold Voltage		
THETA	Modility Modulation		
KAPPA	Saturation Field Factor		
VMAX	Maximum Drift Velocity of Carriers		
XJ	Metallurgical Junction Depth		
UO	Surface Mobility		

Output Voltage Swing (V_{OH1})

Simulation result



Evaluation Circuit

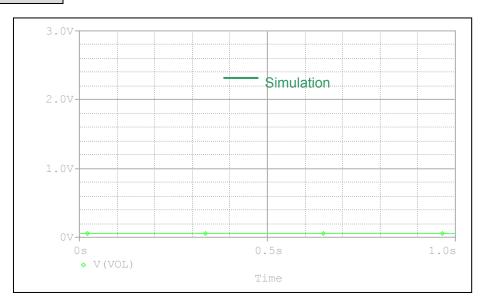


$$VIN+ = (VDD/2) + 0.05,$$
 $VIN- = (VDD/2) - 0.05$

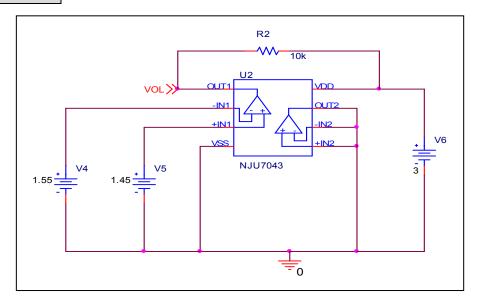
RL=10KΩ	Measurement	Simulation	%Error
V _{OH1} (V)	2.95	2.9532	0.108

Output Voltage Swing (V_{OL1})

Simulation result



Evaluation Circuit

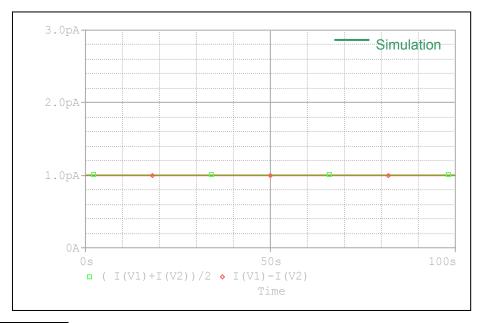


VIN+ = (VDD/2) - 0.05, VIN- = (VDD/2) + 0.05

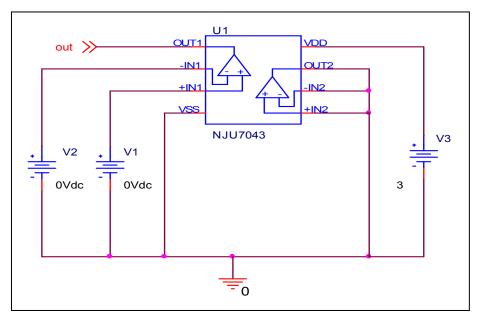
RL=10KΩ	Measurement	Simulation	%Error
V _{OL1} (V)	0.05	0.049225	-1.550

Input Current

Simulation result



Evaluation Circuit

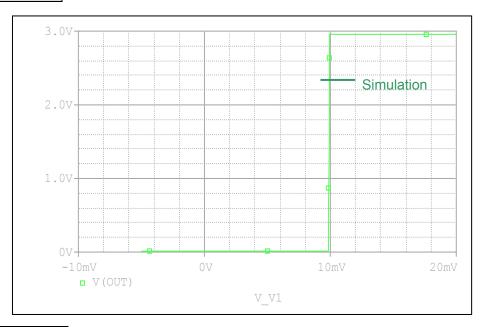


	Measurement	Simulation	% Error
I _b (pA)	1	1.0025	0.25
Ios (pA)	1	0.995	-0.5

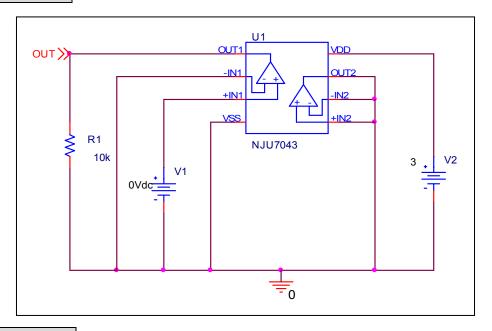
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Input Offset Voltage

Simulation result



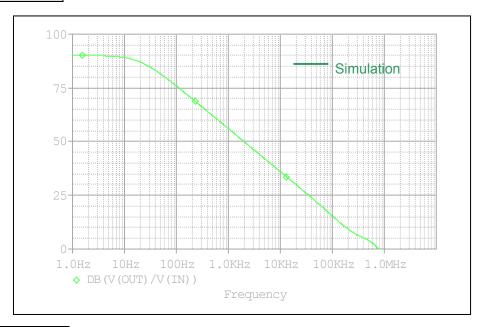
Evaluation Circuit



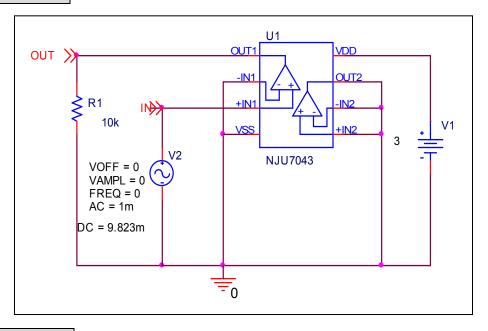
	Measurement	Simulation	%Error
V _{IO} (mV)	10	9.823	-1.770

Open loop Voltage Gain

Simulation result



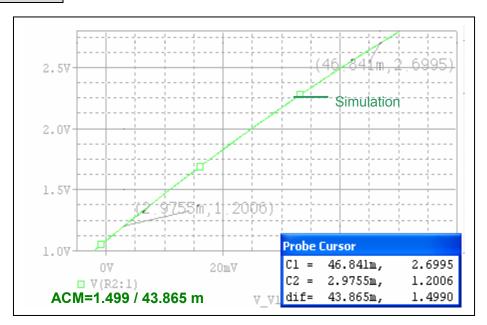
Evaluation Circuit



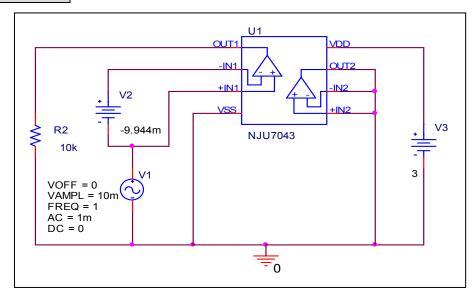
	Measurement	Simulation	%Error
Av (dB)	90	90.184	0.204
Ft (MHz)	0.8	0.779305	-2.587

Common-Mode Rejection Ratio

Simulation result



Evaluation Circuit

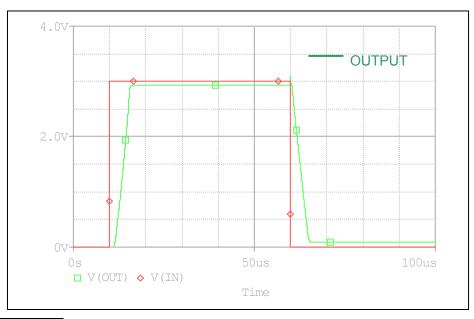


CMRR = AV/ACM

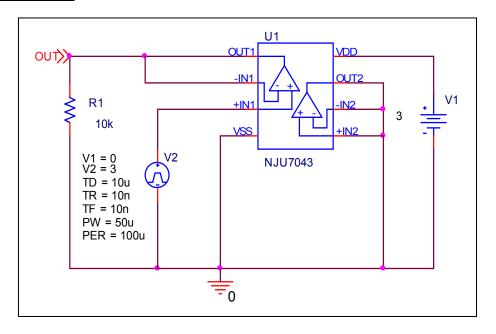
	Measurement	Simulation	%Error
CMRR (dB)	60	59.326	-1.123

Slew Rate

Simulation result



Evaluation Circuit



	Measurement	Simulation	%Error
SR (V/us)	0.7	0.6998	-0.029