Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER

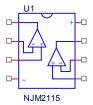
PART NUMBER:NJM2115

MANUFACTURER: NEW JAPAN RADIO CO.,LTD



Bee Technologies Inc.

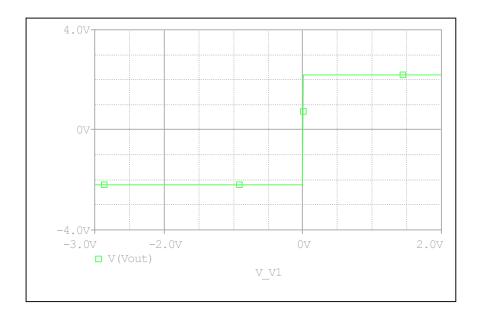
Spice Model



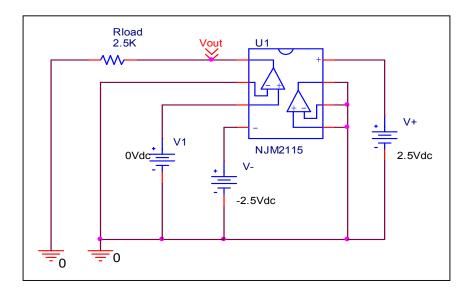
```
*$
* PART NUMBER:NJM2115
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM2115 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X U1 +IN1 -IN1 V+ V- OUT1 NJM2115 S
X U2
       +IN2 -IN2 V+ V- OUT2 NJM2115_S
.ends NJM2115
.subckt NJM2115 S 1 2 3 4 5
 c1 11 12 1.00E-15
 c2 6 7 30.0E-12
 cee 10 99 1.0000E-30
 dc 5 53 dy
 de 54 5 dy
 dlp 90 91 dx
 dln 92 90 dx
 dp 4 3 dx
 egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
 fb 7 99 poly(5) vb vc ve vlp vln 0 187.00E3 -1E3 1E3 190E3 -190E3
 ga 6 0 11 12 2.600E-3
 gcm 0 6 10 99 430.19E-9
 iee 3 10 dc 124.70E-6
 hlim 90 0 vlim 1K
 q1 11 2 13 qx1
 q2 12 1 14 qx2
 r2 6 9 100.00E3
 rc1 4 11 400.26
 rc2 4 12 400.26
 re1 13 10 0.1
 re2 14 10 0.1
 ree 10 99 1.6038E6
 ro1 8 5 50
 ro2 7 99 25
 rp 3 4 125.39
 vb 9 0 dc 0
 vc 3 53 dc 1.0309
 ve 54 4 dc 1.0309
 vlim 7 8 dc 0
 vlp 91 0 dc 1.5000
 vln 0 92 dc 1.5000
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=582.59)
.model qx2 PNP(Is=828.3277E-18 Bf=654.23)
.ends
*$
```

Output Voltage Swing

Simulation result



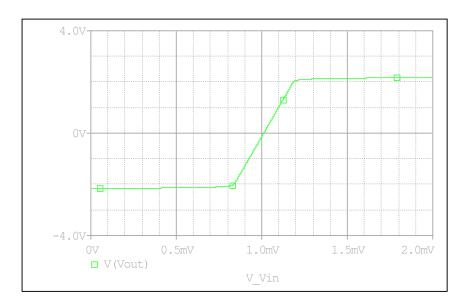
Evaluation circuit



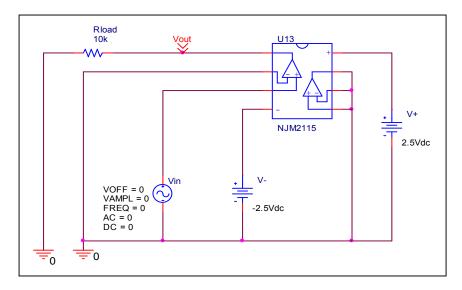
Output Voltage Swing	Measurement	Simulation	%Error
V+	+2.2	+2.1961	-0.177
V-	-2.2	-2.1961	-0.177

Input Offset Voltage

Simulation result



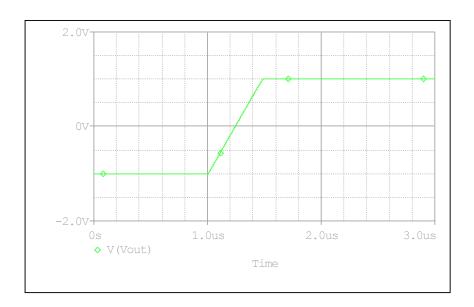
Evaluation circuit



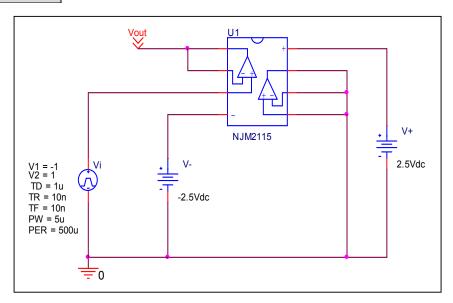
	Measurement	Simulation	%Error
Vos (mV)	1	1.0118	1.18

Slew Rate

Simulation result



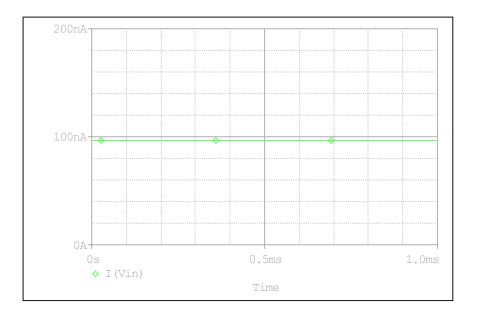
Evaluation circuit



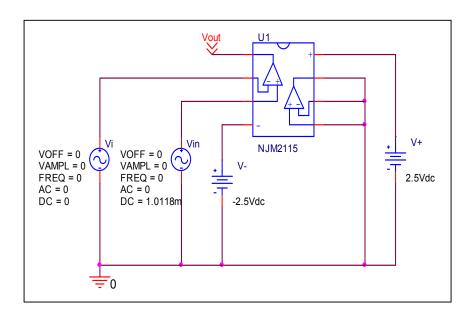
	Measurement	Simulation	%Error
Slew Rate(v/us)	4	4.194	4.850

Input current

Simulation result



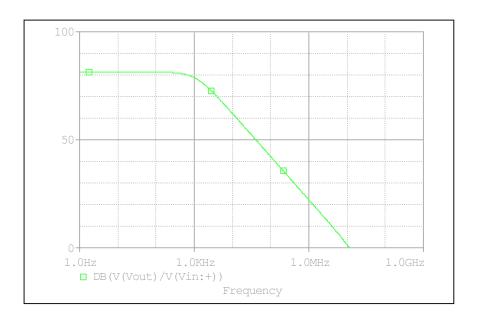
Evaluation circuit



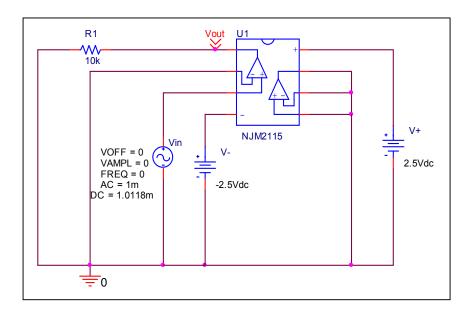
	Measurement	Simulation	%Error
lb(nA)	100	96.487	-3.513

Open Loop Voltage Gain vs. Frequency

Simulation result



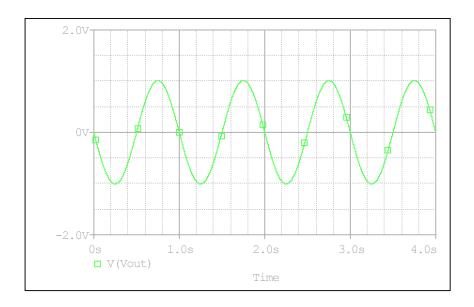
Evaluation circuit



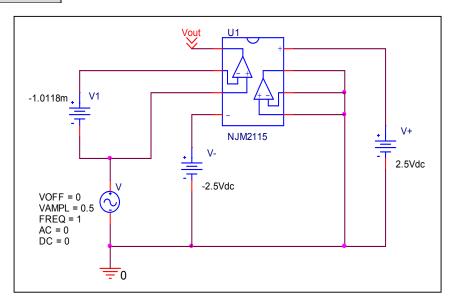
	Measurement	Simulation	%Error
f-0dB(MHz)	12	11.418	-4.850
Av-dc	80	81.275	1.594

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit

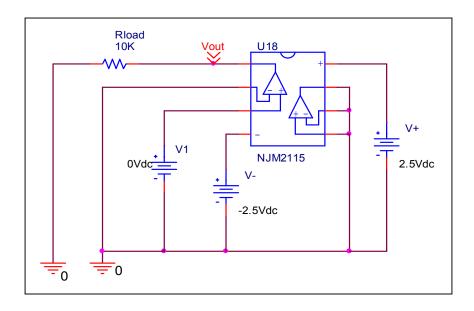


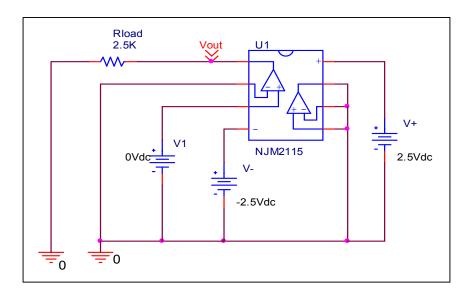
CMRR=20*LOG(11581.105/2.0174) = 75.179 dB

	Measurement	Simulation	%Error
CMRR(dB)	74	75.179	1.593

Remark Output Voltage Swing

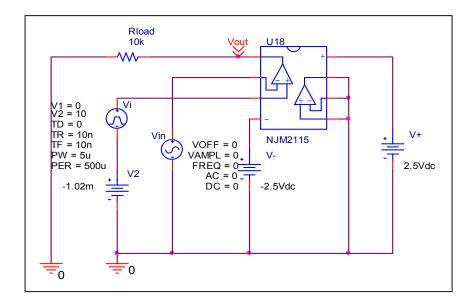
Before

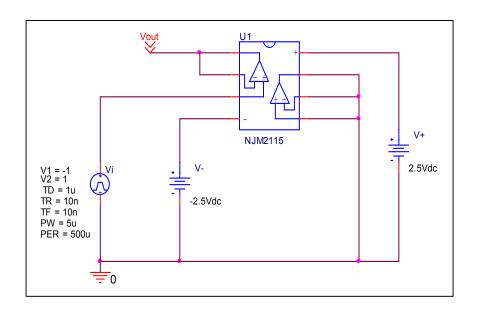




Remark Slew Rate

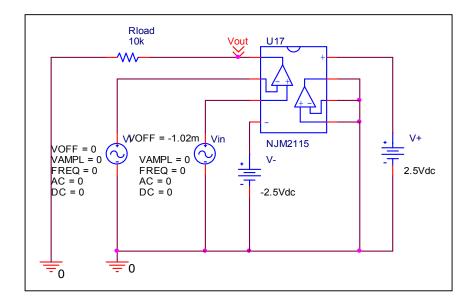
Before

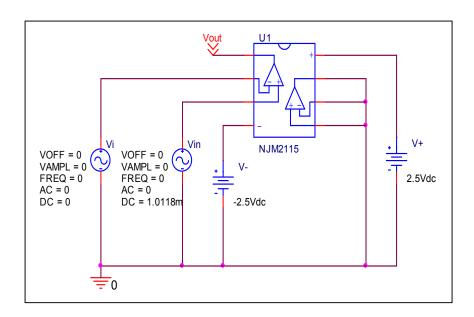




Remark Input current

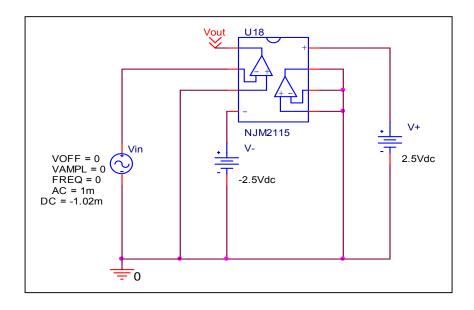
Before

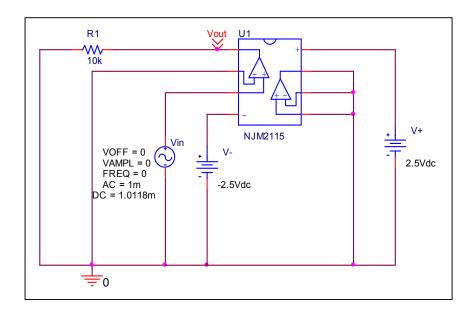




Remark Open Loop Voltage Gain vs. Frequency

Before





Remark Common-Mode Rejection Voltage gain

Before

