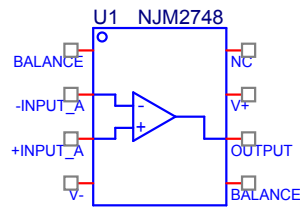# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM2748
MANUFACTURER: NEW JAPAN RADIO

**Bee Technologies Inc.**

Spice Model


```
*$
* PART NUMBER:NJM2748
* MANUFACTURER: NEW JAPAN RADIO
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.Subckt NJM2748 BALANCE -INPUT_A +INPUT_A V- BALANCE
OUTPUT V+ NC
X_U1   +INPUT_A -INPUT_A V+ V- OUTPUT  NJM2748_SUB
.ends  NJM2748
.subckt NJM2748_SUB 1 2 3 4 5
  c1   11 12 2.8868E-12
  c2    6  7 10.000E-12
  css  10 99 1.0000E-30
  dc    5 53 dy
  de   54  5 dy
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 35.967E6 -1E3 1E3 36E6 -36E6
  ga    6  0 11 12 111.21E-6
  gcm   0  6 10 99 2.7935E-9
  iss   3 10 dc 129.10E-6
  hlim 90  0 vlim 1K
  j1   11  2 10 jx1
  j2   12  1 10 jx2
  r2    6  9 100.00E3
  rd1   4 11 8.9918E3
  rd2   4 12 8.9918E3
  ro1   8  5 50
  ro2   7 99 25
  rp    3  4 1.8000E3
  rss  10 99 1.5492E6
  vb    9  0 dc 0
  vc    3 53 dc 2.2979
  ve   54  4 dc 2.2979
  vlim  7  8 dc 0
  vlp  91  0 dc 20
  vln   0 92 dc 20
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model jx1 PJF(Is=23.875E-12 Beta=95.803E-6 Vto=-.99965)
.model jx2 PJF(Is=11.375E-12 Beta=95.803E-6 Vto=-1.000350)
.ends
*$
```
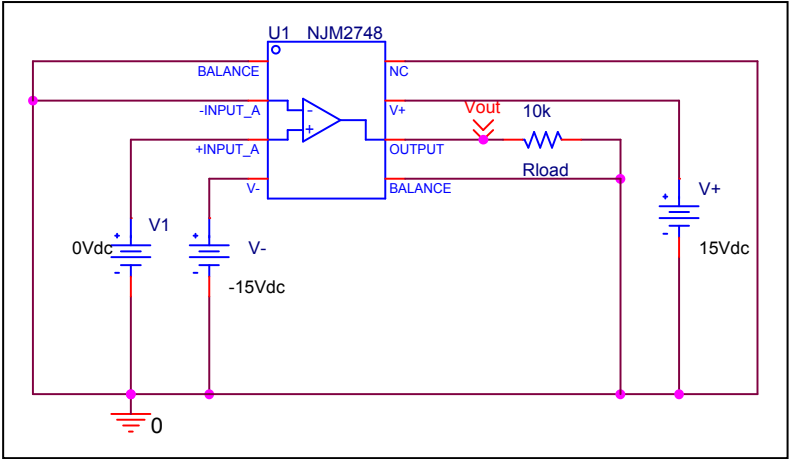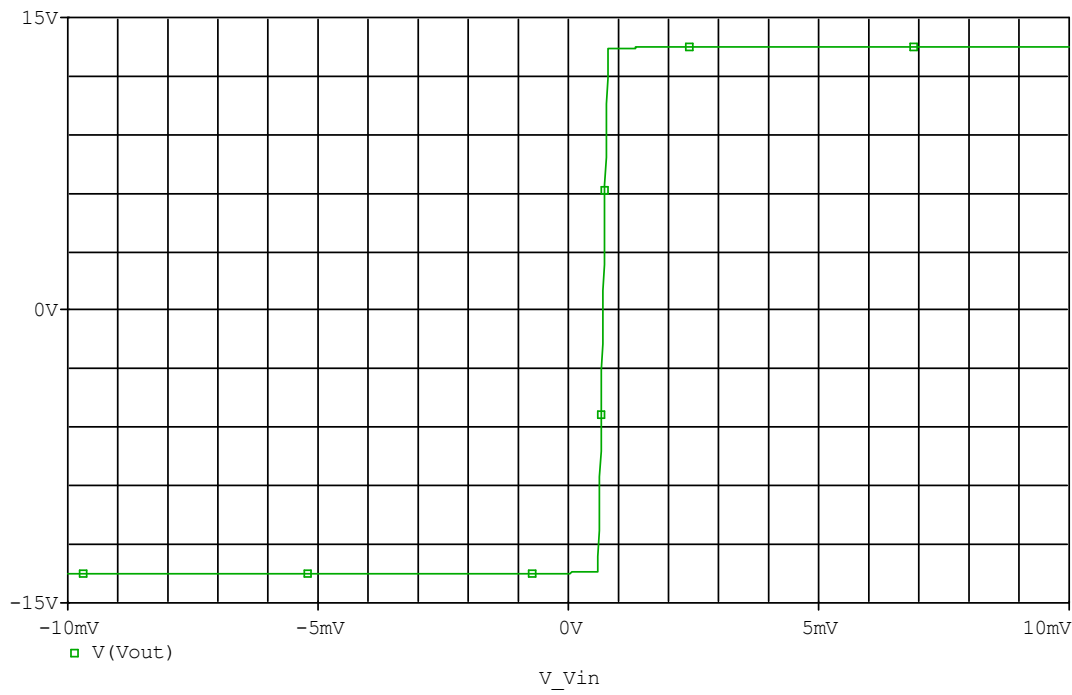
Output Voltage Swing

V_V1
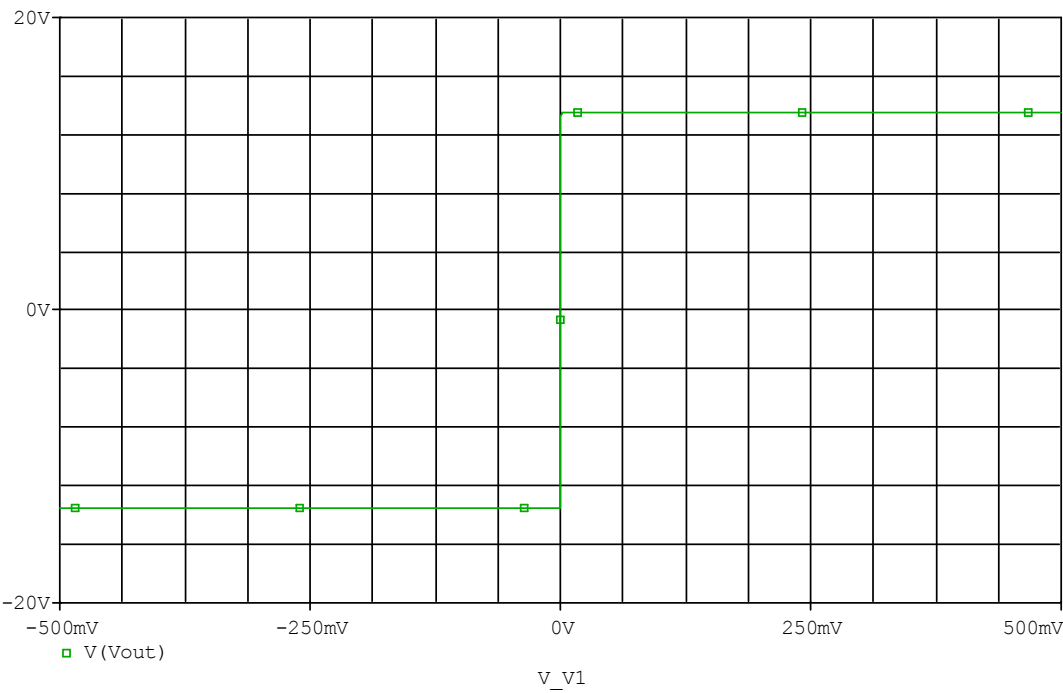
Evaluation circuit

Comparison table
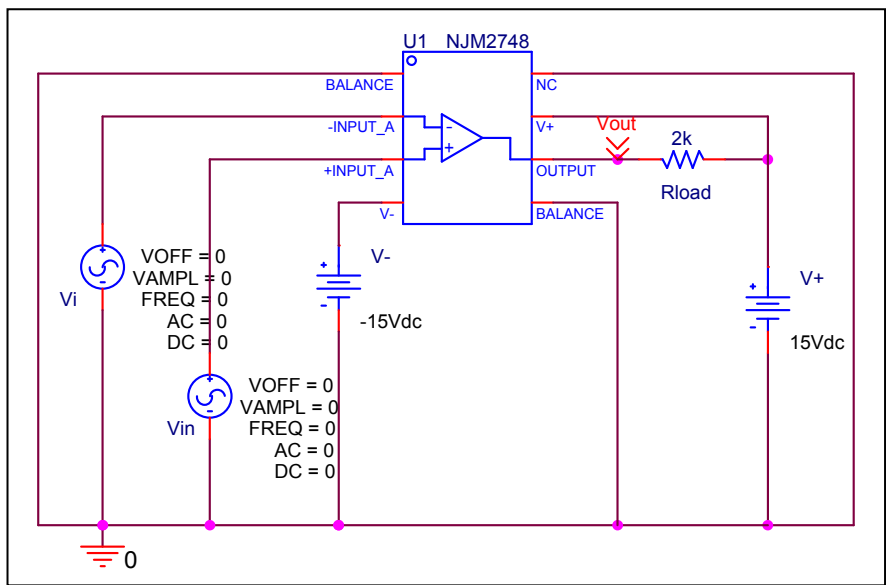
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	13.500	13.491	-0.067
-Vout(V)	-13.500	-13.491	-0.067

Input Offset Voltage

Simulation result

Evaluation circuit

Comparison table

Vos(mV)	Measurement	Simulation	%Error
	0.700	0.692	-1.143

Slew Rate

Simulation result
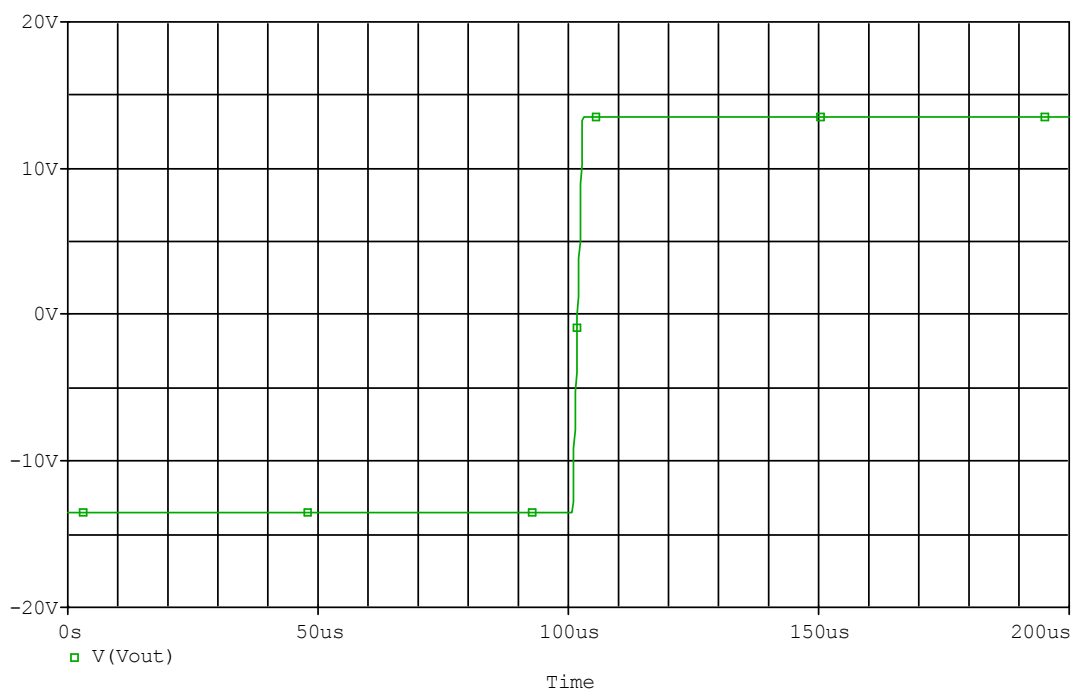
Evaluation circuit
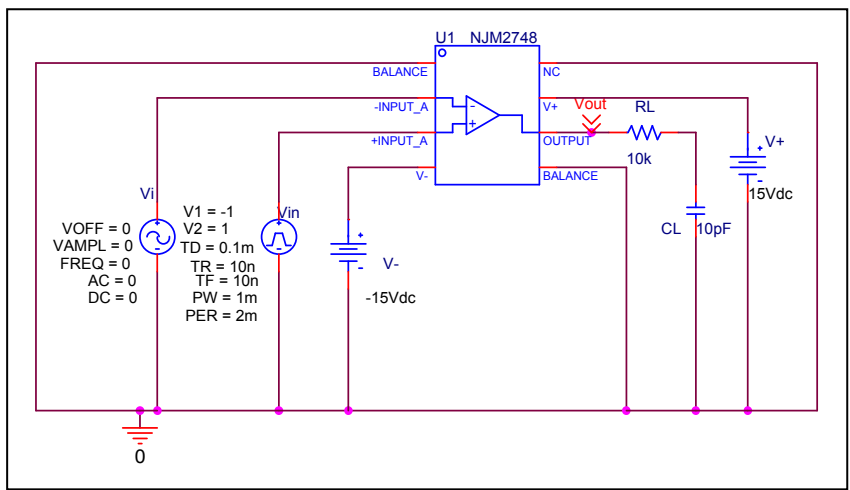
Comparison table

Slew Rate(v/us)	Measurement	Simulation	%Error
	13.000	12.460	-4.154

Input current Ib, Ibos

Simulation result
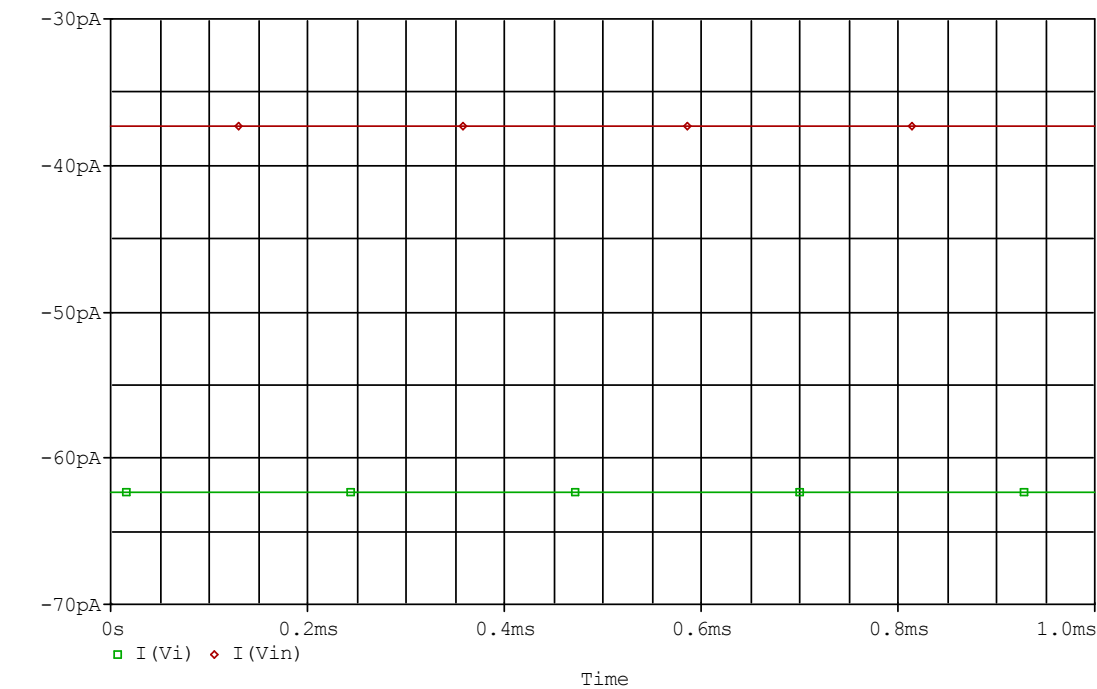
Evaluation circuit
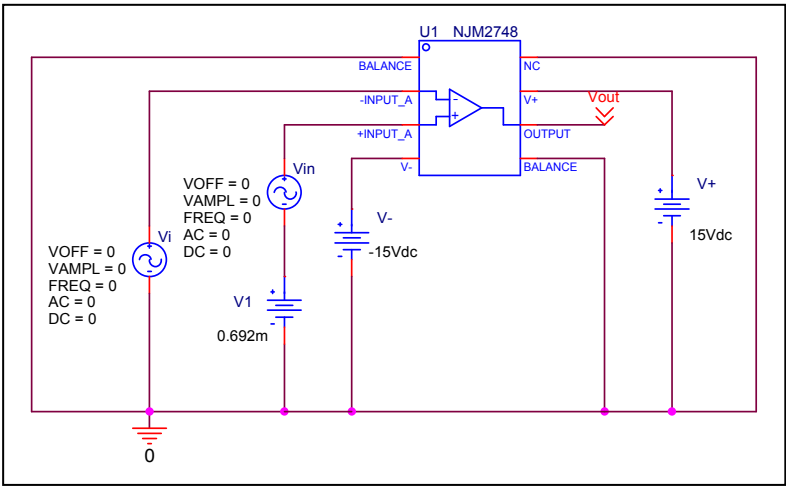
Comparison table

	Measurement	Simulation	%Error
Ib(pA)	50.000	49.831	-0.338
Ibos(pA)	25.000	24.986	-0.056

Open Loop Voltage Gain vs. Frequency , Av-dc, f-0dB

Simulation result

DB(V(Vout)/V(Vin:+))

Frequency
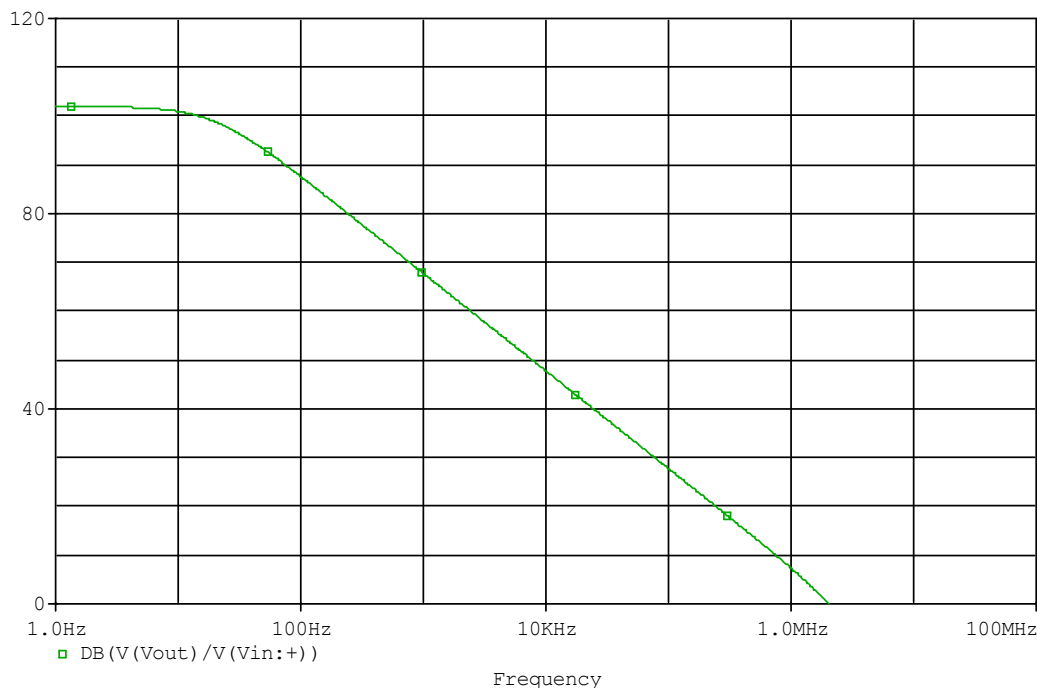
Evaluation circuit
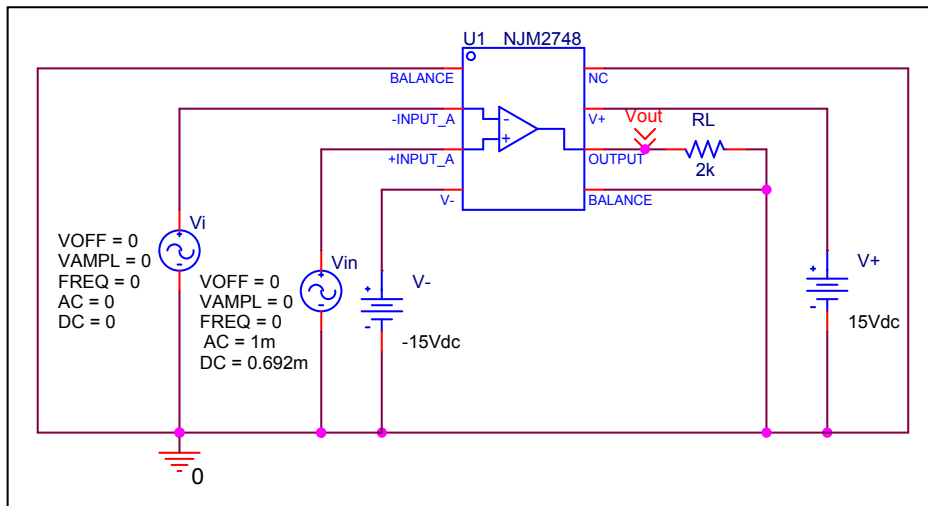
Comparison table

	Measurement	Simulation	%Error
f-0dB(MHz)	2.000	2.035	1.750
Av-dc(dB)	100.000	101.960	1.960

Common-Mode Rejection Voltage gain

□ V(Vout)

Time
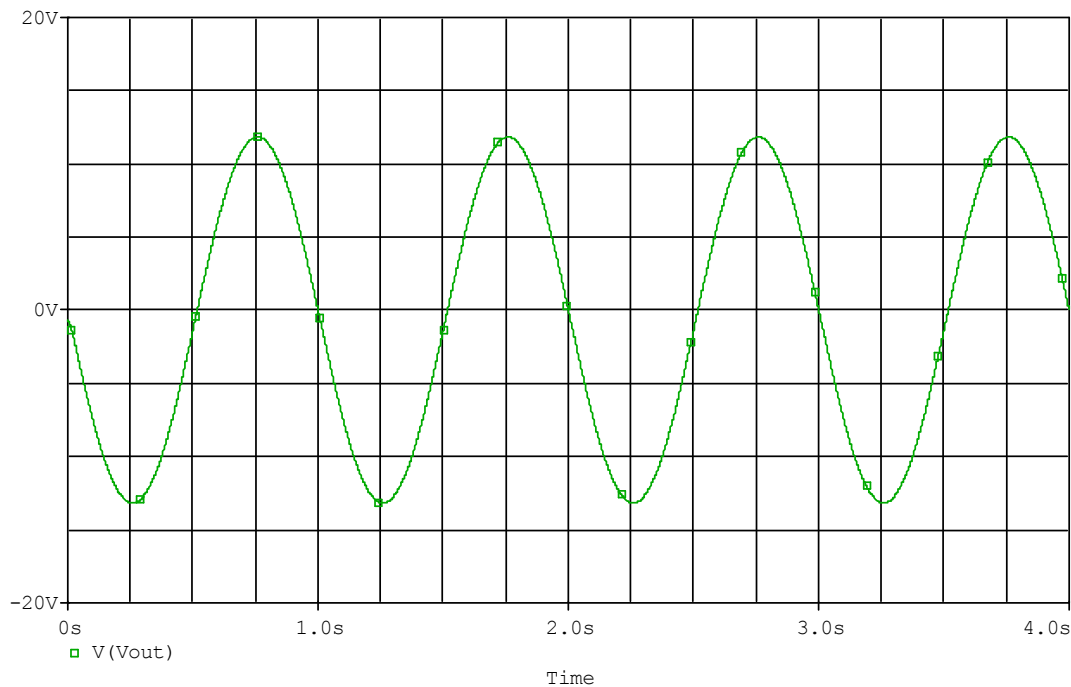
Evaluation circuit
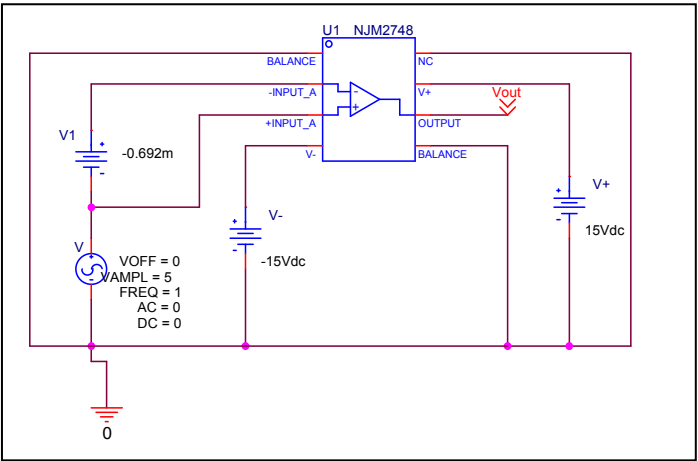
Common Mode Reject Ratio=20*LOG(101.96/(24.998/10)) = 94.001dB

CMRR (dB)	Measurement	Simulation	%Error
	92.000	94.001	2.175