[I2C Implementation]

[This document outlines the I2C implementation using RTL from an open-source core. It enables communication between devices with clock synchronization and data transfer, offering a simple integration for ASIC designs.]

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Content

I2C protocol Introduction

The I2C (Inter-Integrated Circuit) protocol is a serial communication protocol that allows multiple “peripheral” digital integrated circuits (“chips”) to communicate with one or more “controller” chips.

Here are some key features of the I2C protocol:

1. Two-Wire Interface: I2C only uses two wires to transmit data between devices: SDA (Serial Data) and SCL (Serial Clock).

2. Multiple Masters and Slaves: With I2C, you can connect multiple slaves to
a single master, and you can have multiple masters controlling single, or multiple slaves.

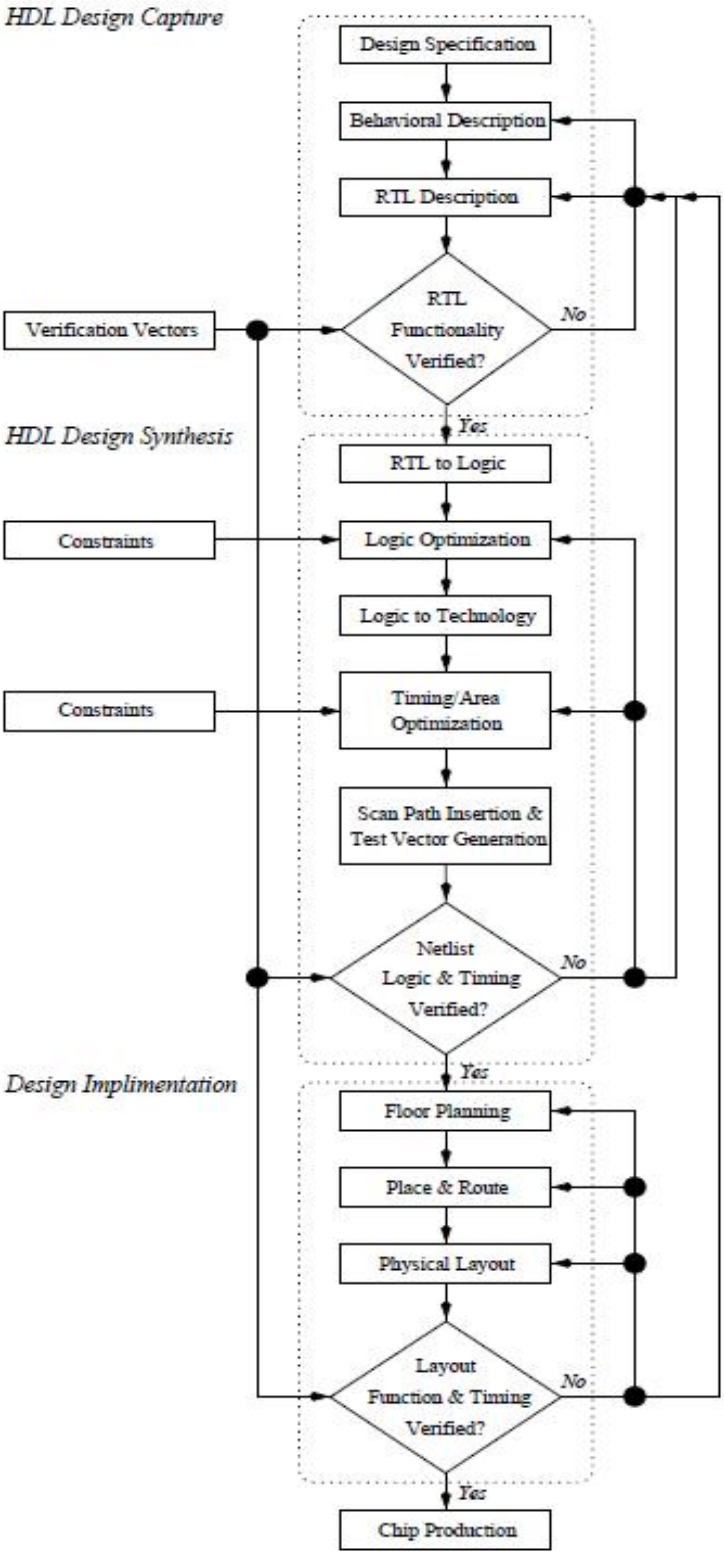
3. Addressing: Each slave device has a unique address. When the master wants to communicate with a specific slave, it sends the address of that slave to all connected devices. Only the slave with the matching address will respond.

4. Synchronous: Like SPI, I2C is synchronous, meaning the output of bits is
synchronized to the sampling of bits by a clock signal shared between the master and the slave.

5. Data Frames: Data is transferred in messages, which are broken up into frames of data. Each message has an address frame that contains the binary address of the slave, and one or more data frames that contain the data being transmitted.

I2C is commonly used in low-speed devices like microcontrollers, EEPROMs, A/D and D/A converters, I/O interfaces, and other similar peripherals in embedded systems.

ASIC Physical Design Flow



Setting Constraints

The constraints focus on defining clock periods, delays, clock jitter, and environment parameters like load capacitance and transition limits. These ensure correct timing analysis for the design while excluding false paths on asynchronous reset signals.

Steps for Design Constraints

Step	*Explanation*
Define Master Clock	Set the main clock for the design (e.g., wb_clk_i).
Define Clock Period	Set the clock period, starting with 1.111 ns.
Define I/O Delay Ratios	Set maximum and minimum input/output delay ratios.
Define I/O Delay	Calculate the maximum and minimum input/output delays.
Define Clock Jitter	Set clock uncertainty as 5% of the clock period.
Define Environment Parameters	Set load capacitance, transition, and fanout constraints.
Create Master Clock	Create the clock with the defined period and apply to ports.
Set Clock Uncertainty	Define setup and hold uncertainties for the clock.
Set I/O Delays	Set maximum and minimum input/output delays on relevant ports.
Set Load Constraints	Apply load capacitance to all output signals.
Set Signals Transitions	Define maximum and input transitions for signals.
Set False Path	Mark arst_i as a false path to avoid timing checks.
Prevent Optimization	Set the clock and reset signals as non-optimizable.

Design Constraints

1- Define Parameters

- **Master Clock**: set MASTER_CLK "wb_clk_i" , **Clock Period**: set CLK_PER 1.111
- **I/O Delay Ratios**:
  - set MAX_IN_DELAY 0.2
  - set MAX_OUT_DELAY 0.2
  - set MIN_IN_DELAY 0.2
  - set MIN_OUT_DELAY 0.2
- **I/O Delay**:
  - set max_in_delay [expr $CLK_PER * $MAX_IN_DELAY]
  - set min_in_delay [expr $CLK_PER * $MIN_IN_DELAY]
  - set max_out_delay [expr $CLK_PER * $MAX_OUT_DELAY]
  - set min_out_delay [expr $CLK_PER * $MIN_OUT_DELAY]
- **Clock Uncertainties**: set CLK_JITTER [expr $CLK_PER * 0.05]
- **Environment Parameters**:
  - **Load Capacitance**: set CAP_LOAD 50
  - **Max Transition**: set MAX_TRANSITION [expr $CLK_PER * 0.15]
  - **Input Transition**: set INPUT_TRANSITION [expr $CLK_PER * 0.03]
- **Max Fanout**: set MAX_FANOUT 10

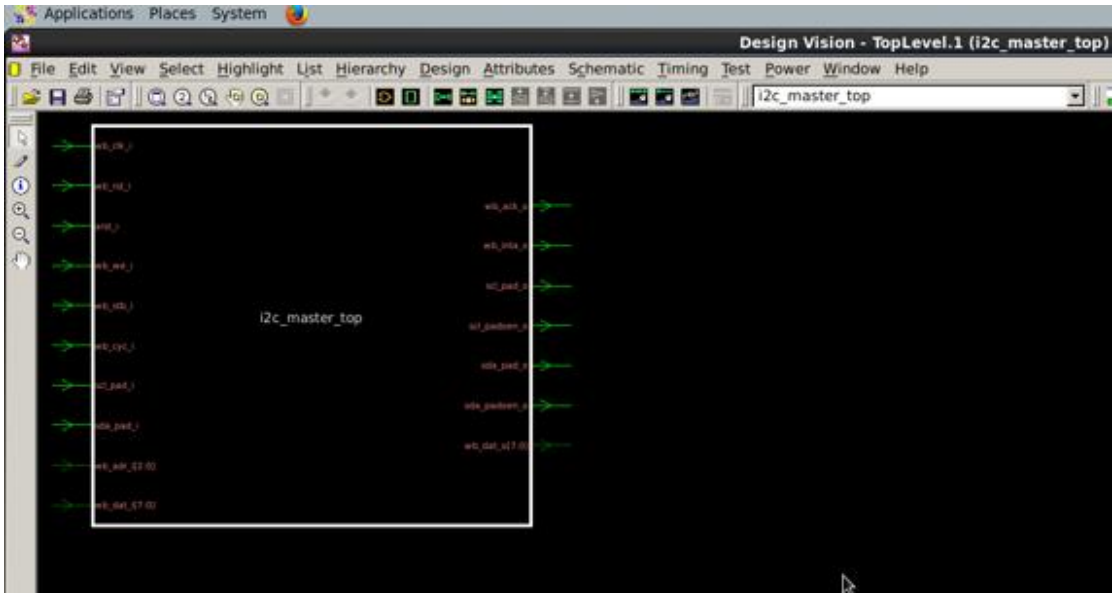
2- Define Constraints

- **Create Master Clock**:
  - create_clock -name $MASTER_CLK -period $CLK_PER [get_ports wb_clk_i]
- **Create Clock Uncertainties**:
  - set_clock_uncertainty -setup $CLK_JITTER [get_clocks $MASTER_CLK]
  - set_clock_uncertainty -hold $CLK_JITTER [get_clocks $MASTER_CLK]
- **I/O Delays**:
  - set_input_delay -max $MAX_IN_DELAY -clock $MASTER_CLK [remove_from_collection [all_inputs] [get_ports {wb_clk_i wb_rst_i arst_i}]]
  - set_input_delay -min $MIN_IN_DELAY -clock $MASTER_CLK [remove_from_collection [all_inputs] [get_ports {wb_clk_i wb_rst_i arst_i}]]
  - set_output_delay -max $MAX_OUT_DELAY -clock $MASTER_CLK [remove_from_collection [all_outputs] [get_ports {wb_clk_i wb_rst_i arst_i}]]
  - set_output_delay -min $MIN_OUT_DELAY -clock $MASTER_CLK [remove_from_collection [all_outputs] [get_ports {wb_clk_i wb_rst_i arst_i}]]
- **Load Constraints**: set_load $CAP_LOAD [all_outputs]
- **Signal Transitions**:
  - set_input_transition $INPUT_TRANSITION [remove_from_collection [all_inputs] [get_ports {wb_clk_i wb_rst_i arst_i}]]
  - set_max_transition $MAX_TRANSITION [remove_from_collection [all_inputs] [get_ports {wb_clk_i wb_rst_i arst_i}]]

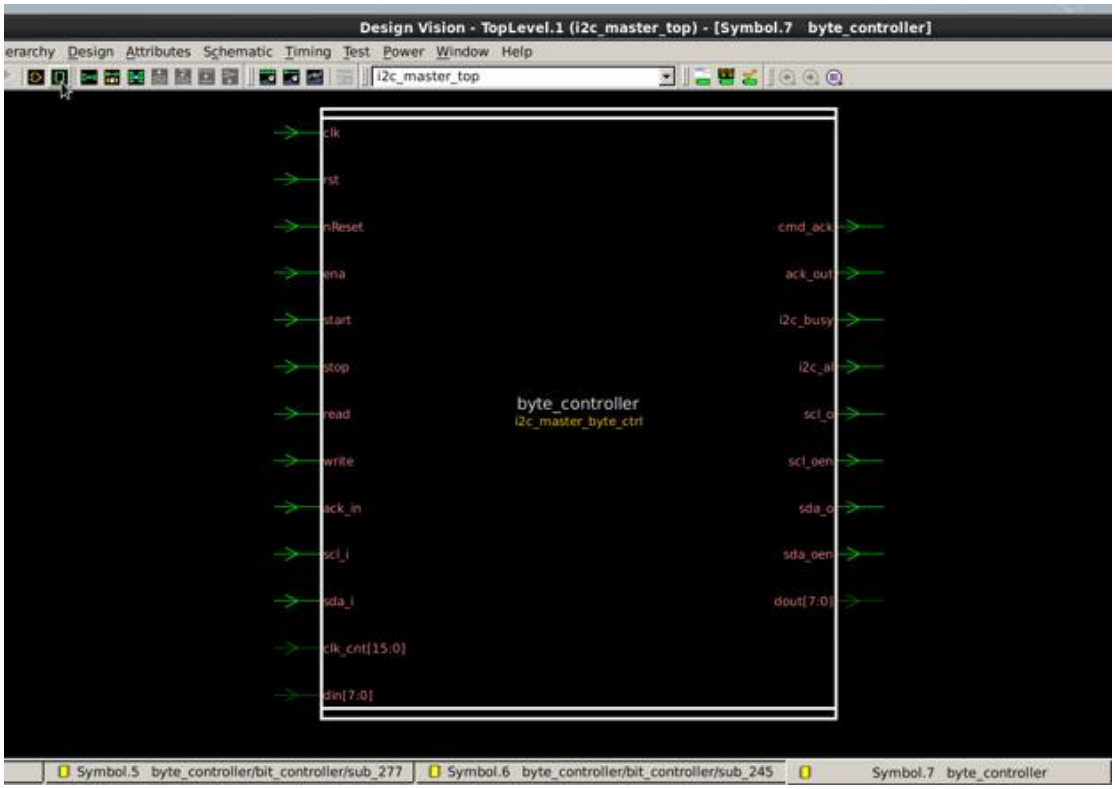
Synthesis

Blocks in design vision

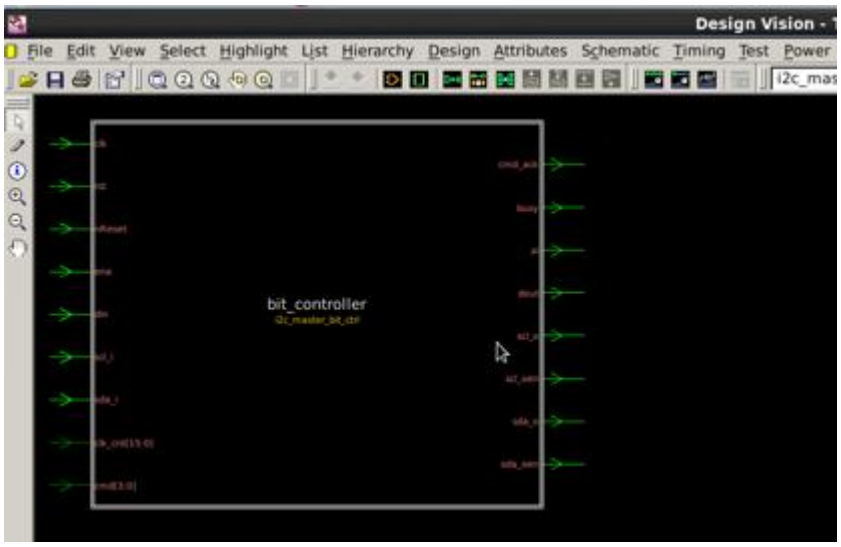
1-I2C Top



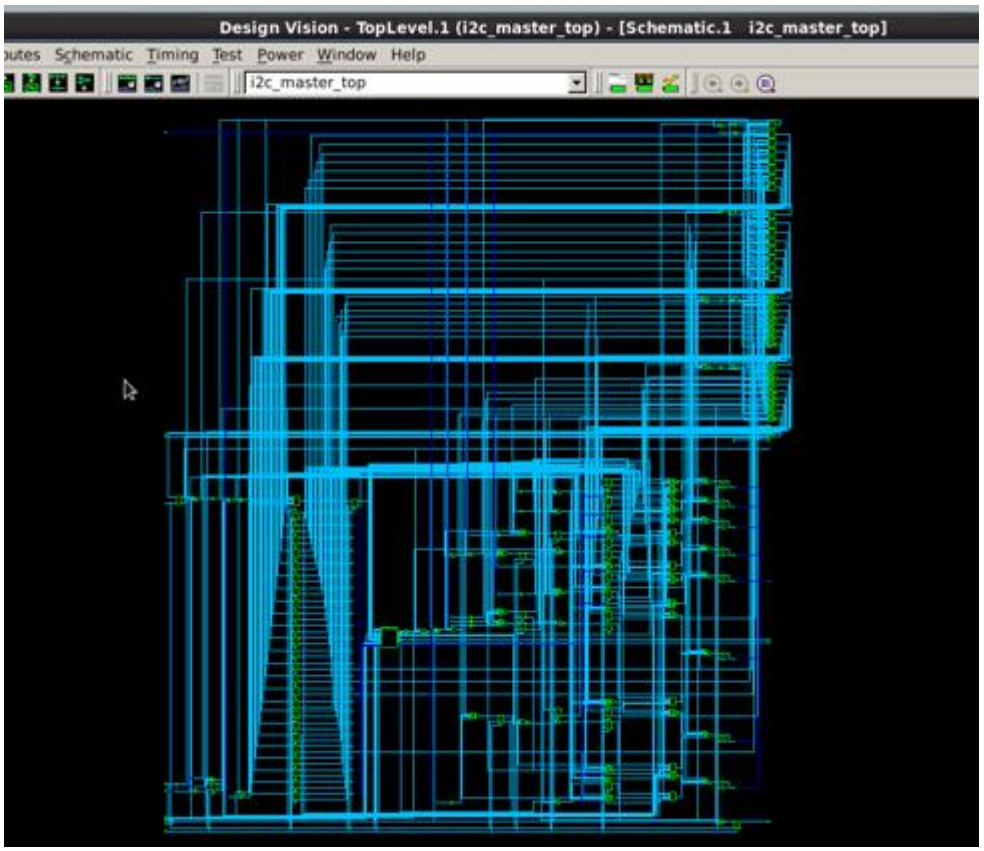
2-byte controller



3- bit controller



4- I2C Top gate level



Reports

1-QoR

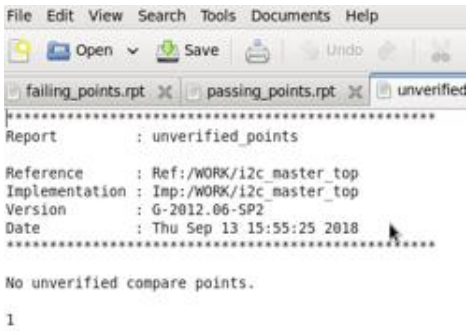
```
****************************************
Report : qor
Design : i2c_master_top
Version: G-2012.06-SP2
Date   : Thu Sep 13 13:37:51 2018
****************************************


  Timing Path Group 'wb_clk_i'
  -----------------------------------
  Levels of Logic:               16.00
  Critical Path Length:           1.00
  Critical Path Slack:            0.02
  Critical Path Clk Period:       1.11
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:           4
  Hierarchical Port Count:         146
  Leaf Cell Count:                 687
  Buf/Inv Cell Count:              116
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:        534
  Sequential Cell Count:           153
  Macro Count:                       0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:       558.866002
  Noncombinational Area:    810.502022
  Buf/Inv Area:              62.510001
  Net Area:                   0.000000
  -----------------------------------
  Cell Area:               1369.368025
  Design Area:             1369.368025


  Design Rules
  -----------------------------------
  Total Number of Nets:            811
  Nets With Violations:              0
  Max Trans Violations:              0
```

2-Setup Report

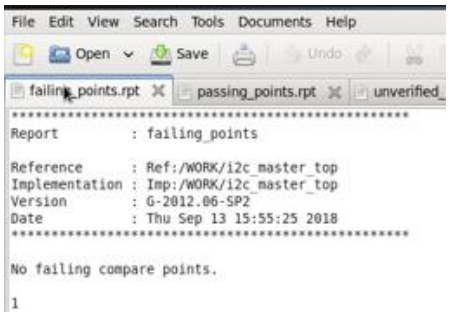
```
Startpoint: byte_controller/bit_controller/c_state_reg[8]
            (rising edge-triggered flip-flop clocked by wb_clk_i)
Endpoint: byte_controller/bit_controller/c_state_reg[13]
          (rising edge-triggered flip-flop clocked by wb_clk_i)
Path Group: wb_clk_i
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
i2c_master_top     5K_hvratio_1_1        NangateOpenCellLibrary_ss0p95vn40c

Point                                                       Incr       Path
-----------------------------------------------------------------------------
clock wb_clk_i (rise edge)                                  0.00       0.00
clock network delay (ideal)                                 0.00       0.00
byte_controller/bit_controller/c_state_reg[8]/CK (DFFR_X1)
                                                            0.00       0.00 r
byte_controller/bit_controller/c_state_reg[8]/Q (DFFR_X1)
                                                            0.08       0.08 f
byte_controller/bit_controller/U77/ZN (NOR2_X1)             0.06       0.14 r
byte_controller/bit_controller/U182/ZN (AND3_X1)            0.07       0.21 r
byte_controller/bit_controller/U200/ZN (NAND4_X1)           0.04       0.25 f
byte_controller/bit_controller/U218/ZN (INV_X1)             0.04       0.29 r
byte_controller/bit_controller/U113/ZN (AND3_X1)            0.06       0.36 r
byte_controller/bit_controller/U201/ZN (NAND4_X1)           0.05       0.40 f
byte_controller/bit_controller/U216/ZN (AND4_X1)            0.04       0.45 f
byte_controller/bit_controller/U219/ZN (NAND4_X1)           0.03       0.48 r
byte_controller/bit_controller/U221/ZN (NOR4_X1)            0.04       0.52 f
byte_controller/bit_controller/U220/ZN (OAI21_X4)           0.10       0.62 r
byte_controller/bit_controller/U10/ZN (INV_X1)              0.06       0.68 f
byte_controller/bit_controller/U13/ZN (NOR2_X1)             0.05       0.73 r
byte_controller/bit_controller/U5/ZN (INV_X1)               0.07       0.80 f
byte_controller/bit_controller/U31/ZN (NOR3_X1)             0.10       0.90 r
byte_controller/bit_controller/U167/ZN (NAND4_X1)           0.06       0.95 f
byte_controller/bit_controller/U87/ZN (OAI21_X1)            0.03       0.99 r
byte_controller/bit_controller/c_state_reg[13]/D (DFFR_X1)
                                                            0.01       1.00 r
data arrival time                                                      1.00

clock wb_clk_i (rise edge)                                  1.11       1.11
clock network delay (ideal)                                 0.00       1.11
clock uncertainty                                          -0.06       1.06
byte_controller/bit_controller/c_state_reg[13]/CK (DFFR_X1)
                                                            0.00       1.06 r
library setup time                                         -0.04       1.02
data required time                                                     1.02
-----------------------------------------------------------------------------
data required time                                                     1.02
data arrival time                                                     -1.00
-----------------------------------------------------------------------------
slack (MET)                                                            0.02
```

Formal Verification (Post-Syn)

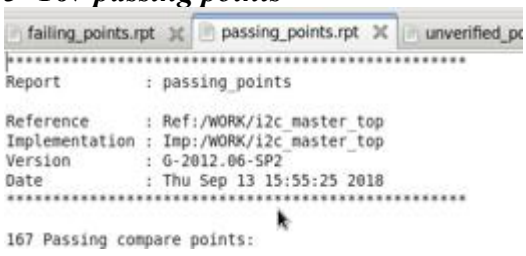
1- Unverified points



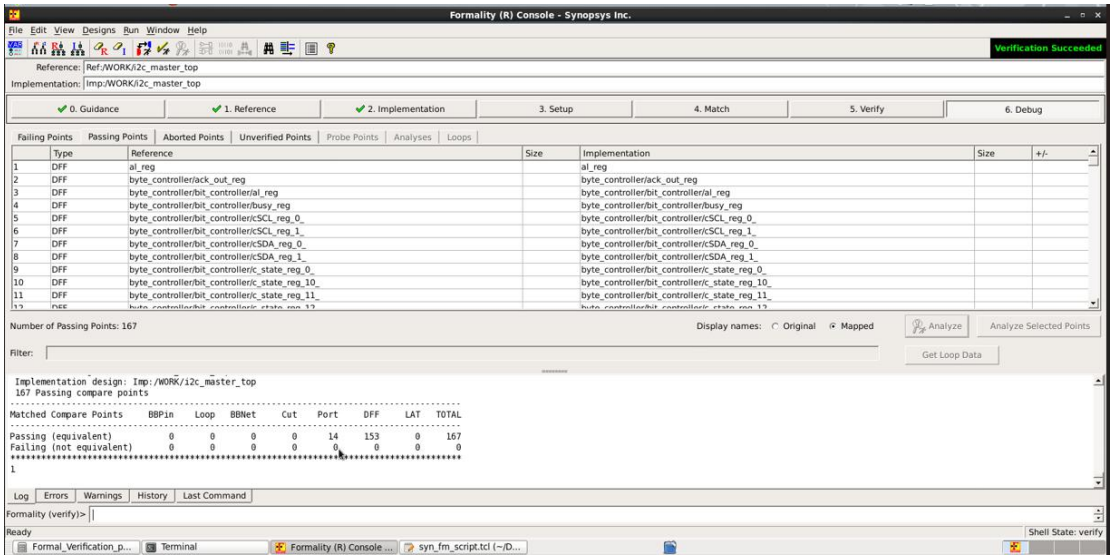
2- Failing Points



3- 167 passing points



GUI



Floor Planning

1. Core Utilization

Definition: Core utilization refers to how efficiently the core area of the die is used for placing standard cells and macros.

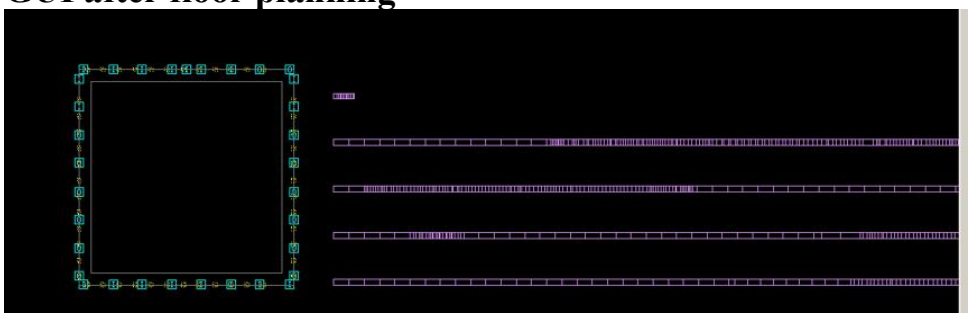
For this design, assume core utilization = 0.6 (60%).
This means that 60% of the core area is reserved for placing standard cells, while 40% is reserved for routing and any buffer insertion during optimization stages.

2. IO Spacing

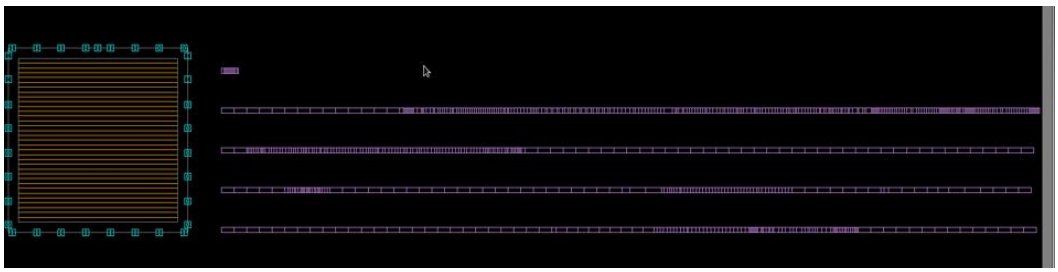
Definition: IO spacing determines the spacing between IO pads or pins around the perimeter of the die.

For this design, assume IO spacing = 20µm.
This means the IO pads are placed 20µm apart from each other.

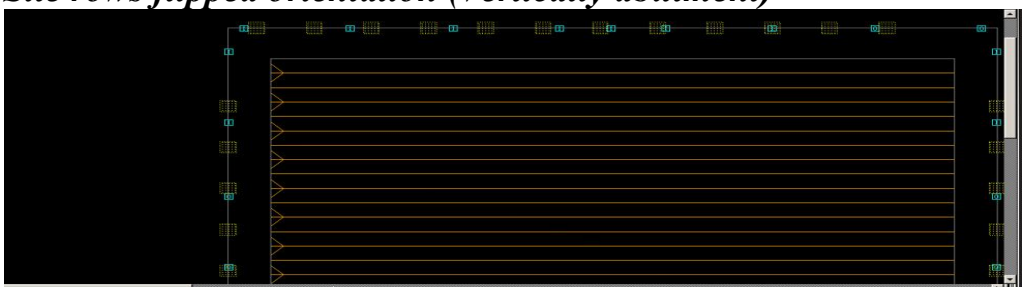
GUI after floor planning



GUI after floor planning with site rows creation



Site rows flipped orientation (Vertically abutment)



Power Planning

Definition: Power planning ensures that the design has a reliable and efficient power distribution network, including power rings and meshes.

Power Rings:

- **Configuration**: Define power rings for VDD and VSS around the core with `set_fp_rail_constraints -set_ring -nets {VDD VSS} -horizontal_ring_layer {metal5 metal7} -vertical_ring_layer {metal6 metal8}`.
- **Spacing**: Set ring spacing to 0.8µm with `-ring_spacing 0.8` and offset to 0.8µm with `-ring_offset 0.8`.

Power Mesh:

- **Layers and Constraints**: Configure power mesh on multiple metal layers with `set_fp_rail_constraints -add_layer -layer metal8 -direction vertical -max_strap 20 -min_strap 10 -min_width 0.5 -spacing minimum` and similar settings for other layers.

Virtual Power Pads:

- **Placement**: Create virtual power pads around the die edges for VDD and VSS with `create_fp_virtual_pad -net VDD -point "{i die_lly}"` and similar commands for other edges.

Analysis:

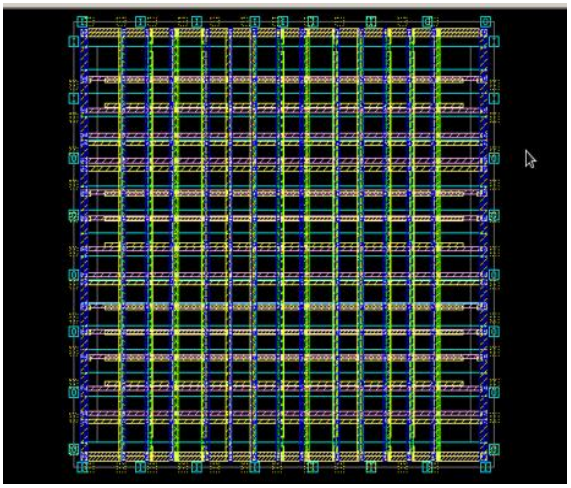
- **IR Drop Analysis**: Perform IR drop analysis with `analyze_fp_rail -nets {VDD VSS} -power_budget 500 -voltage_supply 1.1`, ensuring the max IR drop is within limits (e.g., 22mV).

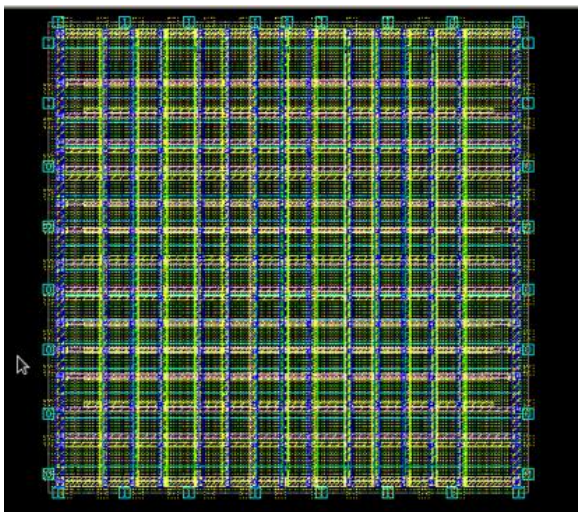
Final Steps:

- **Tap Cells**: Add well tap cells to avoid latch-up violations with `add_tap_cell_array -master TAP -distance 20 -pattern stagger_every_other_row`.

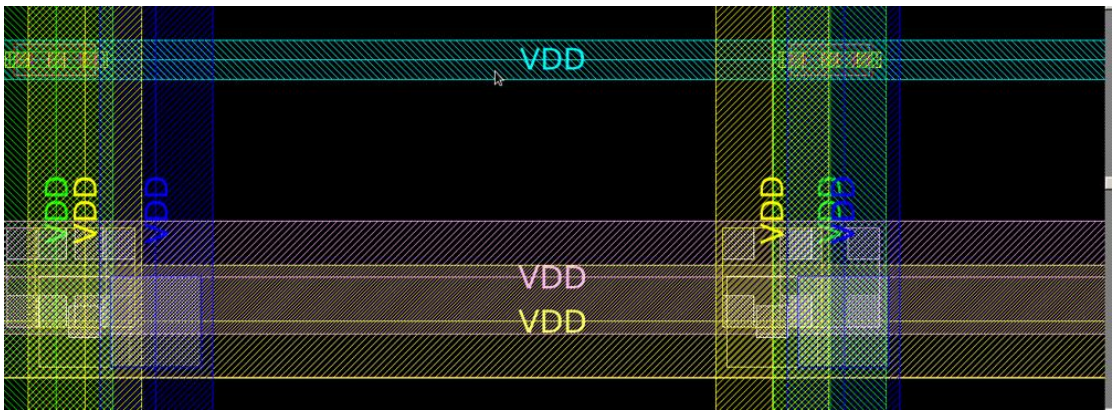
Power Planning

GUI (P/G)





Rails



Analyze IR drop

Target Value: Ensure that the **IR drop across the power grid is 2%** of the operating voltage (e.g., for a 1V power supply, the maximum allowable IR drop is 2**0mV**).

```
1
icc_shell> ## Analyze IR-drop; Modify power network constraints and re-synthesize, as needed.
icc_shell> ## Max IR is 2% of Nominal Supply. In our case, 0.02 x 1.1v= 22mv
icc_shell> commit_fp_rail
Committing the synthesized power plan ...
Done with committing power plan!
1
```

Target Vs synthesized

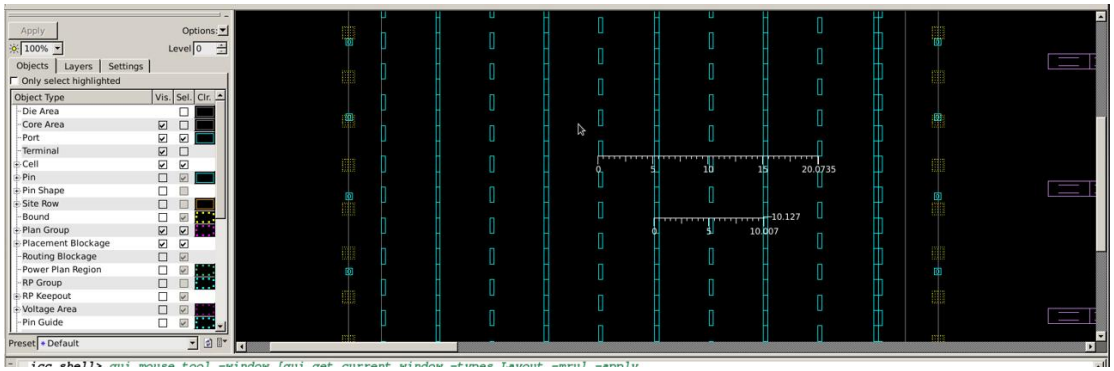
```
Target IR drop :   22.00 mV
Net name : VDD
IR drop of the synthesized net :   13.42 mV
Core ring segment: Horizontal: metal7, Width: 1.0000 microns
Core ring segment: Vertical: metal8, Width: 1.0000 microns
Layer: metal8, Direction: Vertical, # of Straps: 13, PG spacing
The maximum width of straps: 0.5000 microns
The average width of straps: 0.5000 microns
Layer: metal7, Direction: Horizontal, # of Straps: 13, PG spacing
```

Well Tap Insertion

Well tap cells are inserted using the TAP cell type with applied every other row to prevent latch-up and DRC violations.

For this design, assume distance of ***20 units*** between taps and a staggered pattern

Ensuring distance



Placement

Definition: Placement involves positioning standard cells within the core area to optimize for area, performance, and power.

Checks:

- **Pre-Placement Checks**: Verify design readiness with `check_design -stage pre_placement` and `check_placement`.

Constraints:

- **Utilization**: Set core utilization to 0.6 with `set_core_utilization -util 0.6`.
- **Row Spacing**: Configure standard cell row spacing with `set_row_spacing -spacing 50µm`.

Placement Strategy:

- **Standard Cell Placement**: Place standard cells uniformly within the core area, ensuring a 10µm spacing between rows with `place_cells -spacing 10µm`.

Analysis:

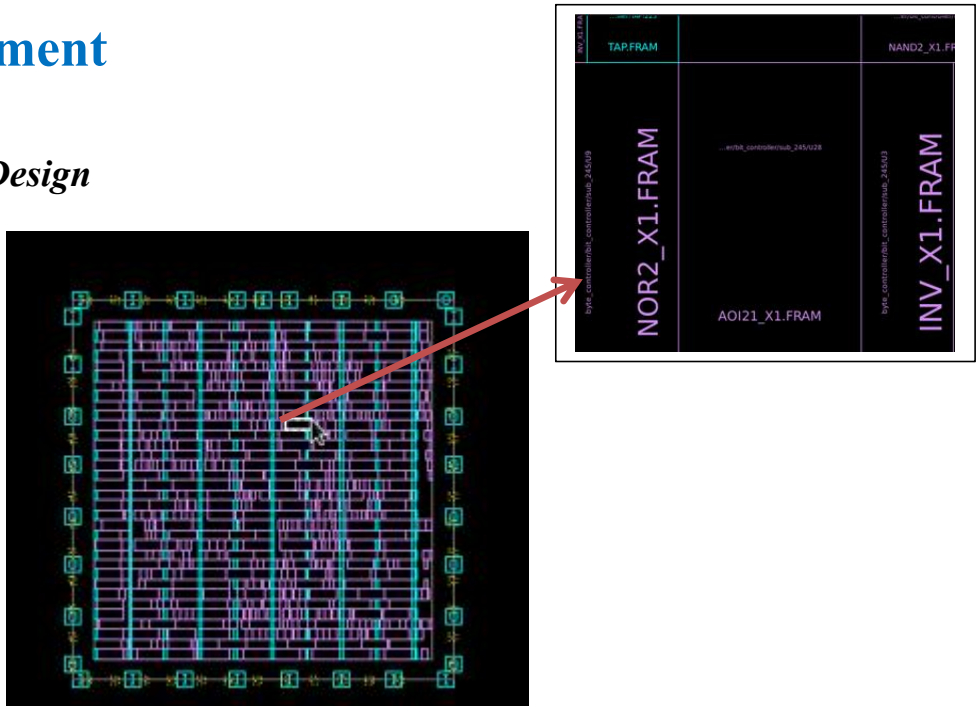
- **Reports**: Generate placement reports with `report_placement -summary` and `report_utilization`.

Additional Actions:

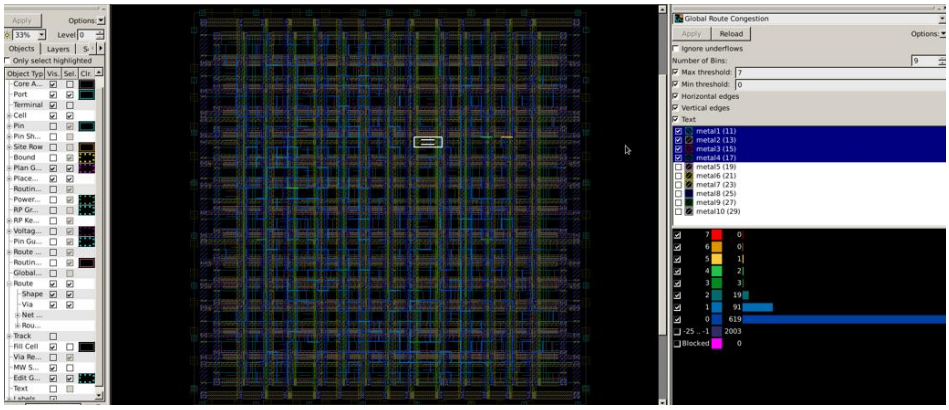
- **Optimization**: Perform placement optimization with `optimize_placement -all` to minimize wire lengths and improve timing.

Placement

Placed Design



Congestion Map



Check Legality

```
****************************************************
Check_legality: Report for Fixed Placement Cells
Information: Use the -verbose option to get details about the legality violations. (PSYN-054)
****************************************************
(fixed placement) Cells Not on Row            : 0
(fixed placement) Cell Overlaps               : 0
(fixed placement) Cells overlapping blockages : 0
(fixed placement) Orientation Violations      : 0
(fixed placement) Site Violations             : 0
(fixed placement) Power Strap Violations      : 0
****************************************************

****************************************************
Check_legality: Report for Non-fixed Placement Cells
Information: Use the -verbose option to get details about the legality violations. (PSYN-054)
****************************************************
Number of Cells Not on Row            : 0
Number of Cell Overlaps               : 0
Number of Cells overlapping blockages : 0
Number of Orientation Violations      : 0
Number of Site Violations             : 0
Number of Power Strap Violations      : 0
****************************************

  Total moveable cell area: 1367.0
  Total fixed cell area: 0.0
  Total physical cell area: 1367.0
  Core area: (30000 30000 506900 506000)
1
icc shell>
```

Timing image Post Placement (Wns)

```
 ELAPSED            WORST NEG TOTAL NEG  DESIGN
  TIME      AREA      SLACK     SLACK   RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:00:03    1369.4      0.00       0.0       0.0

Optimization Complete
---------------------


Beginning Timing Optimizations
------------------------------

 ELAPSED            WORST NEG TOTAL NEG  DESIGN
  TIME      AREA      SLACK     SLACK   RULE COST         ENDPOINT
--------- --------- --------- --------- --------- -------------------------
  0:00:03    1369.4      0.00       0.0       0.0
  0:00:03    1369.4      0.00       0.0       0.0
  0:00:03    1369.4      0.00       0.0       0.0
  0:00:03    1369.4      0.00       0.0       0.0
  0:00:03    1369.4      0.00       0.0       0.0

Optimization Complete
---------------------

WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0
Nets with DRC Violations: 0
Total moveable cell area: 1369.4
Total fixed cell area: 0.0
Total physical cell area: 1369.4
Core area: (30000 30000 506900 506000)
```

Setup Worst path after placement

```
Startpoint: byte_controller/bit_controller/c_state_reg_8_
            (rising edge-triggered flip-flop clocked by wb_clk_i)
Endpoint: byte_controller/bit_controller/c_state_reg_0_
          (rising edge-triggered flip-flop clocked by wb_clk_i)
Path Group: wb_clk_i
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock wb_clk_i (rise edge)                              0.00       0.00
clock network delay (ideal)                             0.00       0.00
byte_controller/bit_controller/c_state_reg_8_/CK (DFFR_X1)     0.00     0.00 r
byte_controller/bit_controller/c_state_reg_8_/Q (DFFR_X1)      0.08     0.08 f
byte_controller/bit_controller/U77/ZN (NOR2_X1)         0.04 *     0.12 r
byte_controller/bit_controller/U182/ZN (AND3_X1)        0.05 *     0.18 r
byte_controller/bit_controller/U200/ZN (NAND4_X1)       0.03 *     0.21 f
byte_controller/bit_controller/U218/ZN (INV_X1)         0.02 *     0.23 r
byte_controller/bit_controller/U190/ZN (AND4_X1)        0.05 *     0.28 r
byte_controller/bit_controller/U176/ZN (NAND4_X1)       0.04 *     0.32 f
byte_controller/bit_controller/U227/ZN (AND3_X1)        0.05 *     0.37 f
byte_controller/bit_controller/U219/ZN (NAND4_X1)       0.02 *     0.39 r
byte_controller/bit_controller/U221/ZN (NOR4_X1)        0.02 *     0.41 f
byte_controller/bit_controller/U220/ZN (OAI21_X4)       0.05 *     0.46 r
byte_controller/bit_controller/U10/ZN (INV_X1)          0.03 *     0.49 f
byte_controller/bit_controller/U13/ZN (NOR2_X1)         0.03 *     0.53 r
byte_controller/bit_controller/U5/ZN (INV_X1)           0.05 *     0.57 f
byte_controller/bit_controller/U31/ZN (NOR3_X1)         0.07 *     0.64 r
byte_controller/bit_controller/U165/ZN (NAND4_X1)       0.04 *     0.69 f
byte_controller/bit_controller/U85/ZN (OAI21_X1)        0.02 *     0.71 r
byte_controller/bit_controller/c_state_reg_0_/D (DFFR_X1)  0.00 *     0.71 r
data arrival time                                                  0.71

clock wb_clk_i (rise edge)                              1.11       1.11
clock network delay (ideal)                             0.00       1.11
clock uncertainty                                      -0.06       1.06
byte_controller/bit_controller/c_state_reg_0_/CK (DFFR_X1)     0.00     1.06 r
library setup time                                     -0.04       1.02
data required time                                                 1.02
-----------------------------------------------------------------------
data required time                                                 1.02
data arrival time                                                 -0.71
-----------------------------------------------------------------------
slack (MET)                                                        0.31
```

Clock Tree Synthesize

Definition: CTS involves creating a clock distribution network to ensure that the clock signal reaches all flip-flops with minimal skew and delay.

Checks:

- **Pre-CTS Checks**: Ensure design readiness with `check_physical_design -stage pre_clock_opt` and `check_clock_tree`.

Constraints:

- **Driving Cell**: Set driving cell for the clock with `set_driving_cell -lib_cell BUF_X16 -pin Z [get_ports wb_clk_i]`.
- **Clock Tree Options**: Define constraints for clock trees with `set_clock_tree_options` for delay, skew, capacitance, fanout, and transition.

Clock Tree Routing:

- **CTS Optimization**: Perform CTS with `clock_opt -only_cts -no_clock_route`.
- **Post-CTS Optimization**: Use `clock_opt -only_psyn -no_clock_route` for hold time fixes and other optimizations.
- **Clock Tree Routing**: Execute `route_group -all_clock_nets` to complete the clock tree routing.

Analysis:

- **Reports**: Generate reports for clock tree synthesis with `report_clock_tree -summary` and `report_timing`.

Global Skew before CTS (Longest & shortest path delay)

```
The longest path delay end pin: byte_controller/sr_reg_0_/CK
The shortest path delay end pin: wb_dat_o_reg_7_/CK

The longest Path:
Pin                 Cap                 Fanout    Trans     Incr      Arri
-------------------------------------------------------------------------------
wb_clk_i            0.000                    1  0.000     0.000     0.000     r
wb_clk_i            173.256                153  0.000     0.000     0.000     r
byte_controller/sr_reg_0_/CK
                    173.256                  0  0.019     0.022     0.022     r
[clock delay]                                                        0.022
-------------------------------------------------------------------------------

The Shortest Path:
Pin                 Cap                 Fanout    Trans     Incr      Arri
-------------------------------------------------------------------------------
wb_clk_i            0.000                    1  0.000     0.000     0.000     r
wb_clk_i            173.256                153  0.000     0.000     0.000     r
wb_dat_o_reg_7_/CK
                    173.256                  0  0.003     0.004     0.004     r
[clock delay]                                                        0.004
-------------------------------------------------------------------------------

1
```

Global Skew after CTS (Longest & shortest path delay)

```
The longest path delay end pin: byte_controller/bit_controller/fSCL_reg_1_/CK
The shortest path delay end pin: byte_controller/bit_controller/cnt_reg_5_/CK

The longest Path:
Pin             Cap                  Fanout    Trans     Incr      Arri
------------------------------------------------------------------------------
wb_clk_i        0.000                     1  0.000     0.000     0.000     r
wb_clk_i        230.892                 123  0.000     0.000     0.000     r
CTS_wb_clk_i_CTO_delay1/A
                230.892                   1  0.015     0.018     0.018     r
CTS_wb_clk_i_CTO_delay1/Z
                35.302                   31  0.005     0.024     0.042     r
byte_controller/bit_controller/fSCL_reg_1_/CK
                35.302                    0  0.005     0.002     0.044     r
[clock delay]                                                    0.044
------------------------------------------------------------------------------

The Shortest Path:
Pin             Cap                  Fanout    Trans     Incr      Arri
------------------------------------------------------------------------------
wb_clk_i        0.000                     1  0.000     0.000     0.000     r
wb_clk_i        230.892                 123  0.000     0.000     0.000     r
byte_controller/bit_controller/cnt_reg_5_/CK
                230.892                   0  0.014     0.017     0.017     r
[clock delay]                                                    0.017
------------------------------------------------------------------------------

1
icc_shell> report_clock_timing -type summary ; # reports for the clock tree.
```

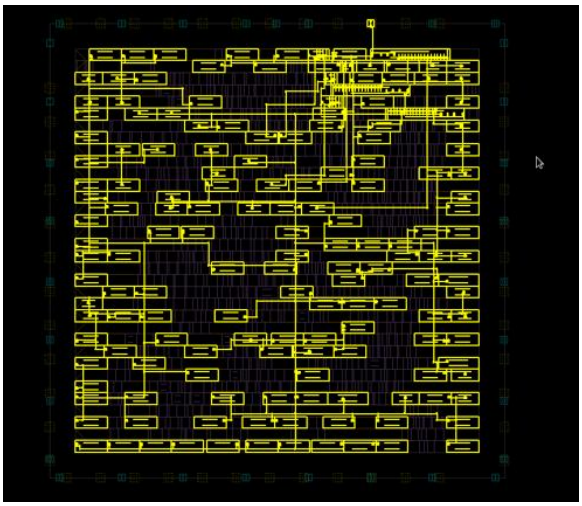
Hold Report after CTS routing

```
Startpoint: byte_controller/bit_controller/cSDA_reg_0
            (rising edge-triggered flip-flop clocked by wb_clk_i)
Endpoint: byte_controller/bit_controller/cSDA_reg_1
          (rising edge-triggered flip-flop clocked by wb_clk_i)
Path Group: wb_clk_i
Path Type: min

Point                                                   Incr       Path
------------------------------------------------------------------------------
clock wb_clk_i (rise edge)                              0.00       0.00
clock network delay (propagated)                        0.03       0.03
byte_controller/bit_controller/cSDA_reg_0_/CK (DFFR_X1)
                                                        0.00       0.03 r
byte_controller/bit_controller/cSDA_reg_0_/QN (DFFR_X1)
                                                        0.08       0.10 r
byte_controller/bit_controller/U144/ZN (NOR2_X1)        0.01 *     0.12 f
byte_controller/bit_controller/cSDA_reg_1_/D (DFFR_X1)
                                                        0.00 *     0.12 f
data arrival time                                                  0.12

clock wb_clk_i (rise edge)                              0.00       0.00
clock network delay (propagated)                        0.04       0.04
clock uncertainty                                       0.06       0.10
byte_controller/bit_controller/cSDA_reg_1_/CK (DFFR_X1)
                                                        0.00       0.10 r
library hold time                                       0.01       0.11
data required time                                                 0.11
------------------------------------------------------------------------------
data required time                                                 0.11
data arrival time                                                 -0.12
------------------------------------------------------------------------------
slack (MET)                                                        0.01
```

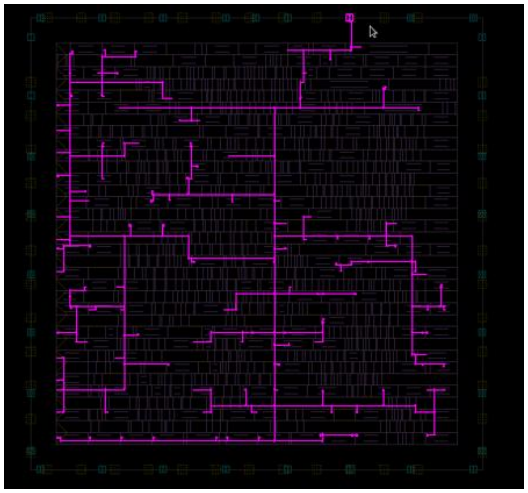
check legality after CTS

```
****************************************************
Check_legality: Report for Fixed Placement Cells
Information: Use the -verbose option to get details about the legality violations. (PSYN-054)
****************************************************
(fixed placement) Cells Not on Row          : 0
(fixed placement) Cell Overlaps             : 0
(fixed placement) Cells overlapping blockages : 0
(fixed placement) Orientation Violations    : 0
(fixed placement) Site Violations           : 0
(fixed placement) Power Strap Violations    : 0
****************************************************

****************************************************
Check_legality: Report for Non-fixed Placement Cells
Information: Use the -verbose option to get details about the legality violations. (PSYN-054)
****************************************************
Number of Cells Not on Row          : 0
Number of Cell Overlaps             : 0
Number of Cells overlapping blockages : 0
Number of Orientation Violations    : 0
Number of Site Violations           : 0
Number of Power Strap Violations    : 0
****************************************
```

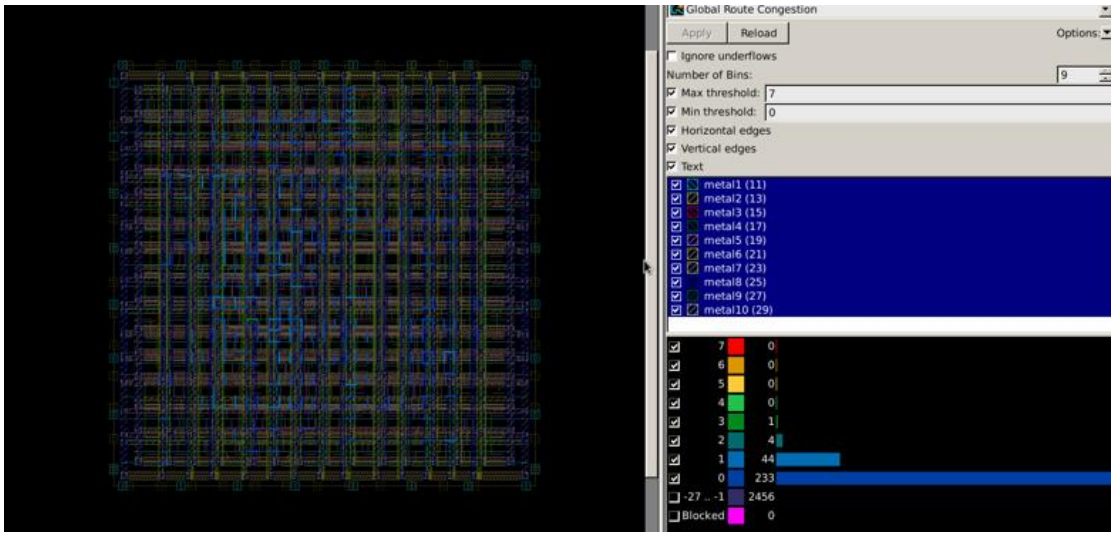
GUI



Level 0 (CLK source)



Congestion Map after CTS



Routing

Global Routing:

- **Global Routing Setup:** Perform global routing checks and optimization with `check_physical_design -stage pre_route_opt` and `check_routeability` to ensure connectivity and plan routing paths effectively.
- **Global Routing Options:** Set routing options with `set_route_options -groute_timing_driven true -groute_incremental true -track_assign_timing_driven true -same_net_notch check_and_fix` to ensure timing-driven and incremental global routing.

Detailed Routing:

- **Track and Layer Setup:** Define detailed routing parameters with `set_delay_calculation_options -arnoldi_effort low` and `set_route_options -track_width 1 -track_pitch 2` to optimize track width and pitch for routing.
- **Detailed Routing Execution:** Execute detailed routing with `route_opt -incremental` to refine the routing paths for timing and congestion.

Crosstalk Management:

- **Crosstalk Prevention:** Set options for crosstalk prevention with `set_si_options -route_xtalk_prevention true -delta_delay true -min_delta_delay true -static_noise true -timing_window true` to minimize noise and signal interference.

Hold Fix and Buffer Preference:

- **Hold Fixes:** Apply hold fixes using `set_fix_hold [all_clocks]` and prioritize buffer cells with `set_prefer -min [get_lib_cells "*/BUF_X2 */BUF_X1"]` for timing and signal integrity.

Power Grid Connection:

- **Power Grid Setup:** Define power and ground connections with `derive_pg_connection -power_net VDD -ground_net VSS -power_pin VDD -ground_pin VSS` to ensure proper power distribution.

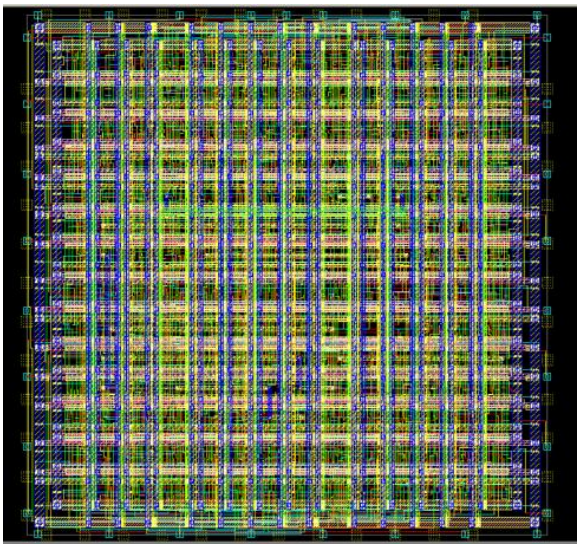
Final Verification:

- **Verify Routing:** Perform final routing verification and checks with `verify_zrt_route`, `report_noise`, and `report_timing -crosstalk_delta` to ensure the design meets all requirements and is free of issues.

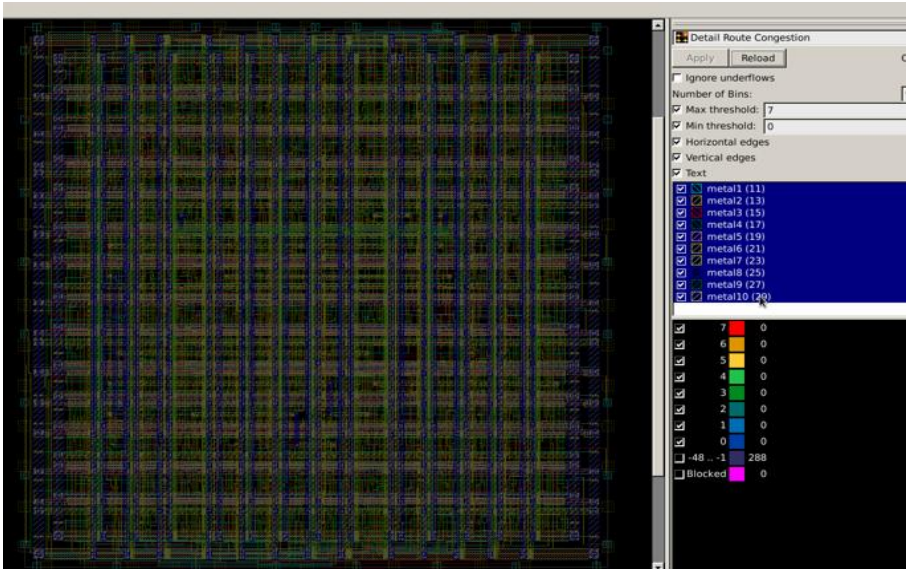
1- check routability before routing

```
icc_shell> check_routeability

Cell i2c_master_top.err existed already. Replace it ...
Warning: Cell contains tie connections which are not connected to real P

============================================
==          Check Pin-Spot Min-Grid       ==
============================================


============================================
==          Check Pin out of bound        ==
============================================


No out-of-bound error found

============================================
==              Check Min-Grid            ==
============================================

No min-grid error found

============================================
==         Check for blocked ports        ==
============================================

No blocked port was detected
```

2- chip after routing



3- Congestion Map after detail routing



4- Timing image after routing

```
full, end, only, short, start, full_clock, full_clock_expanded (CRD-031)
icc_shell> report_timing -delay_type max

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : i2c_master_top
Version: G-2012.06-ICC-SP2
Date   : Wed Sep 12 17:53:18 2018
****************************************

 * Some/all delay information is back-annotated.

Operating Conditions: worst_low   Library: NangateOpenCellLibrary_ss0p95vn40c
        Parasitic source    : LPE
        Parasitic mode      : RealRC
        Extraction mode     : MIN_MAX
        Extraction derating : -40/-40/-40

Information: Percent of Arnoldi-based delays =  0.00%
No paths.

1
icc_shell> report_timing -delay_type min

****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : i2c_master_top
Version: G-2012.06-ICC-SP2
Date   : Wed Sep 12 17:53:24 2018
****************************************

 * Some/all delay information is back-annotated.

Operating Conditions: worst_low   Library: NangateOpenCellLibrary_ss0p95vn40c
        Parasitic source    : LPE
        Parasitic mode      : RealRC
        Extraction mode     : MIN_MAX
        Extraction derating : -40/-40/-40

Information: Percent of Arnoldi-based delays =  0.00%
No paths.

1
icc_shell>
```

5- DRC

```
Verify Summary:

Total number of nets = 894, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Total number of voltage-area violations = no voltage-areas defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked

1
```

6-Noise

```
****************************************
Report : noise
Design : i2c_master_top
Version: G-2012.06-ICC-SP2
Date   : Wed Sep 12 17:35:47 2018
****************************************


slack type: area

noise_region: above_low
pin name          width     height    slack
-------------------------------------------------
U167/A            0.08      0.04      0.02

noise_region: below_high
pin name          width     height    slack
-------------------------------------------------
U167/A            0.13      0.04      0.04
1
icc_shell> report_timing -crosstalk_delta
Information: Start rc update...
```

Chip Finishing

Standard Cell Filler Insertion:

- **Filler Cells:** Insert filler cells between standard cells to maintain power and ground connections with insert_stdcell_filler -cell_without_metal {FILLCELL_X32 FILLCELL_X16 FILLCELL_X8 FILLCELL_X4 FILLCELL_X2 FILLCELL_X1} -connect_to_power VDD -connect_to_ground VSS.

```
Filling cell with master <FILLCELL_X32> and connecting PG nets...
    0 filler cells with master <FILLCELL_X32> were inserted
Filling cell with master <FILLCELL_X16> and connecting PG nets...
    The first filler cell name is xofiller!FILLCELL_X16!1
    The last filler cell name is xofiller!FILLCELL_X16!10
    10 filler cells with master <FILLCELL_X16> were inserted
Filling cell with master <FILLCELL_X8> and connecting PG nets...
    The first filler cell name is xofiller!FILLCELL_X8!1
    The last filler cell name is xofiller!FILLCELL_X8!95
    95 filler cells with master <FILLCELL_X8> were inserted
Filling cell with master <FILLCELL_X4> and connecting PG nets...
    The first filler cell name is xofiller!FILLCELL_X4!1
    The last filler cell name is xofiller!FILLCELL_X4!236
    236 filler cells with master <FILLCELL_X4> were inserted
Filling cell with master <FILLCELL_X2> and connecting PG nets...
    The first filler cell name is xofiller!FILLCELL_X2!1
    The last filler cell name is xofiller!FILLCELL_X2!898
    898 filler cells with master <FILLCELL_X2> were inserted
Filling cell with master <FILLCELL_X1> and connecting PG nets...
    0 filler cells with master <FILLCELL_X1> were inserted
=== End of Filler Cell Insertion ===
```

Redundant Via Insertion:

- **Via Redundancy:** Ensure robust connections by adding redundant vias with insert_zrt_redundant_vias to improve reliability and reduce electromigration risks.

```
Redundant via conversion report:
--------------------------------

  Total optimized via conversion rate = 93.65% (6066 / 6477 vias)

    Layer via1       = 88.00% (2750   / 3125    vias)
        Weight 1     = 88.00% (2750    vias)
        Un-optimized = 12.00% (375     vias)
    Layer via2       = 98.86% (2605   / 2635    vias)
        Weight 1     = 98.86% (2605    vias)
        Un-optimized =  1.14% (30      vias)
    Layer via3       = 99.16% (711    / 717     vias)
        Weight 1     = 99.16% (711     vias)
        Un-optimized =  0.84% (6       vias)

  Total double via conversion rate    = 93.65% (6066 / 6477 vias)

    Layer via1       = 88.00% (2750   / 3125    vias)
    Layer via2       = 98.86% (2605   / 2635    vias)
    Layer via3       = 99.16% (711    / 717     vias)


Verify Summary:

Total number of nets = 908, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Total number of voltage-area violations = no voltage-areas defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked

1
```

Layout vs. Schematic (LVS) Check:

- **LVS Verification:** Run an LVS check to ensure the layout matches the design schematic using `verify_lvs -ignore_floating_port -ignore_floating_net -check_open_locator -check_short_locator` to detect any shorts or open circuits.

```
        Potential connection region ((26, 46), (31, 50)).
ERROR : There are more errors than default Max Error Number
** Total OPEN Nets are 20.
** Total Electrical Equivalent Error are 0.
** Total Must Joint Error are 0.

-- LVS END : --
Elapsed =    0:00:00, CPU =    0:00:00
Update error cell ...
1
```

Opens Violations

Shoving opens by route eco

Verify lvs after eco routing

```
** Total SHORT Nets are 3.
** Total OPEN Nets are 0.
** Total Electrical Equivalent Error are 0.
** Total Must Joint Error are 0.

-- LVS END : --
```

Shorts

Highlight shorts to solve them manually

LVS Clean

```
** Total OPEN Nets are 0.
** Total Electrical Equivalent Error are 0.
** Total Must Joint Error are 0.

-- LVS END : --
Elapsed =    0:00:00, CPU =    0:00:00
```