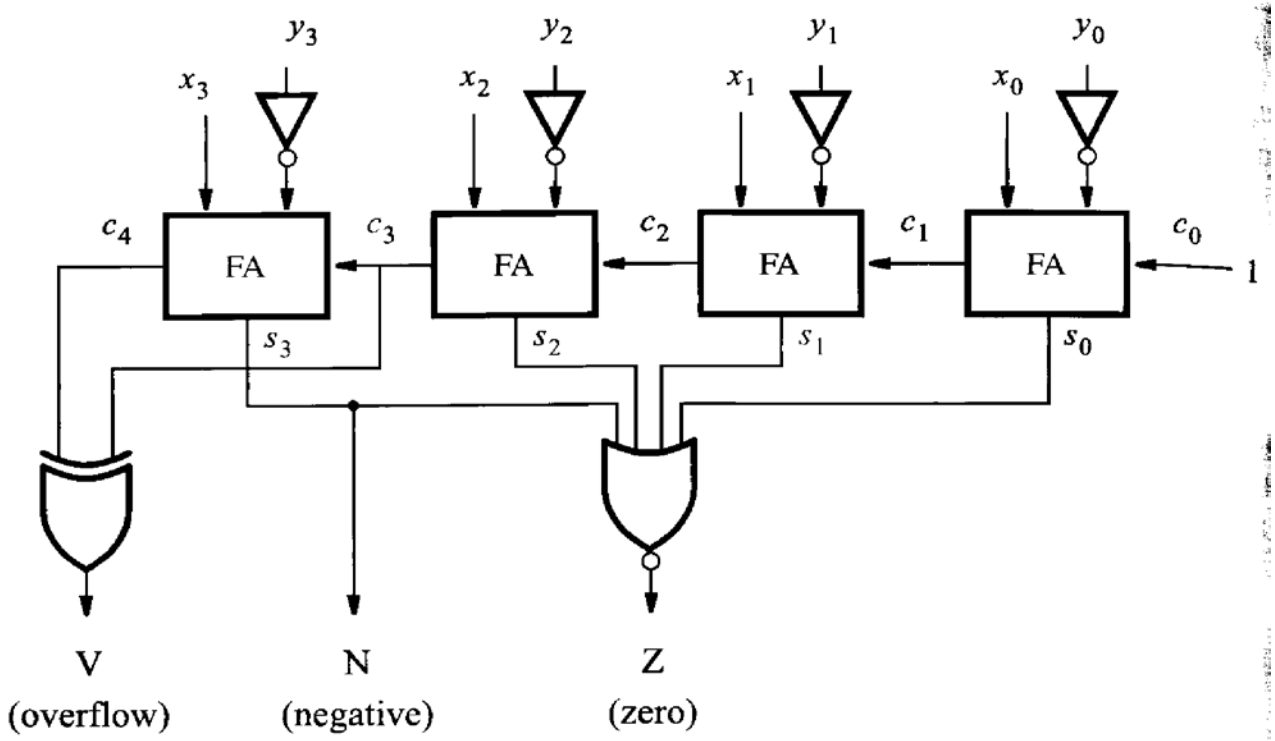
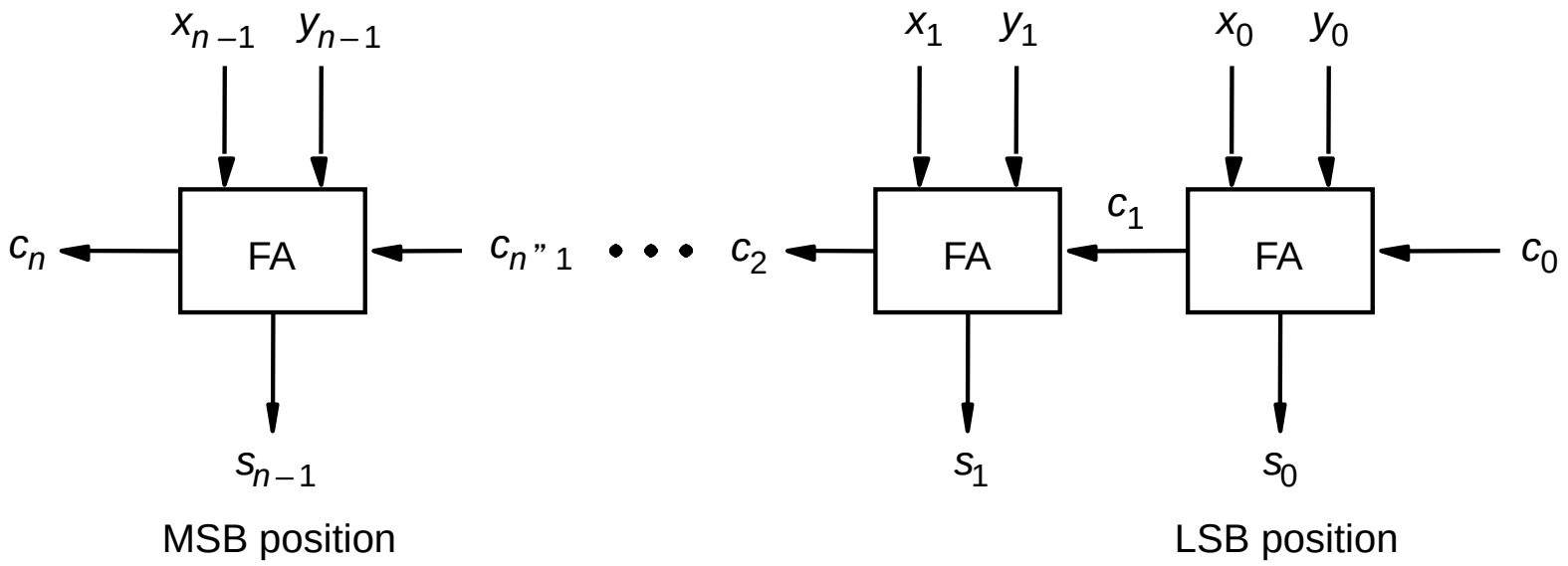
Cs 343
Spring 2017
Lab 1
Part 3
Using the procedure described in Comparator Tutorial Lab
Design:

- Using 1 bit Full-adder and gates DESIGN (write VHDL CODE) for 4 bit subtractor unit as shown in the figure below.
- In addition to the arithmetic result of the subtraction, you have to display a bit Z=1 if the result is zero, N=1 if the result is negative, and V=1 if the result is overflow.
- Create a component for this unit and include in your package.
- Verify all your designs in simulation
- Program the FPGA board and verify it works correctly.
- Using the component you have designed above and gates, multiplexers,, design 8 bit adder/ subtractor unit. Verify it in simulation and program the board.
- Write a detailed report following format given to you.


y_3
y_2
y_1
y_0
x_3
x_2
x_1
x_0
c_4
c_3
c_2
c_1
c_0
FA
FA
FA
FA
1
s_3
s_2
s_1
s_0
V
(overflow)
N
(negative)
Z
(zero)

An *n*-bit ripple-carry adder



Denote by Δt time 1-Bit Full adder computes addition of two bits and carry.

Question: How much time it takes to compute the sum of two 32 bits words ?