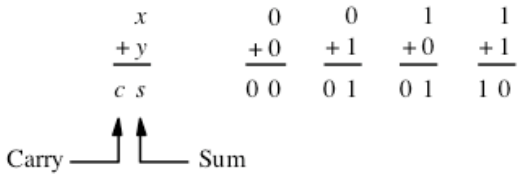
Cs 343
Spring 2017
Lab 1
Using the procedure described in Comparator Tutorial Lab
Design:

- Half adder
- Full-adder using gates
- Full-adder using Half adder as a component
- 4 bit adder using 1bit Full adder as a component
- Verify all your designs in simulation
- Program the FPGA board and verify it works correctly.
- Write a detailed report following format given to yiou.

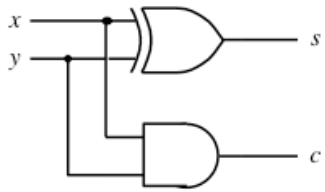
HALF-Adder



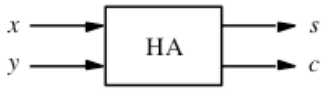
(a) The four possible cases

x	y	Carry c	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b) Truth table

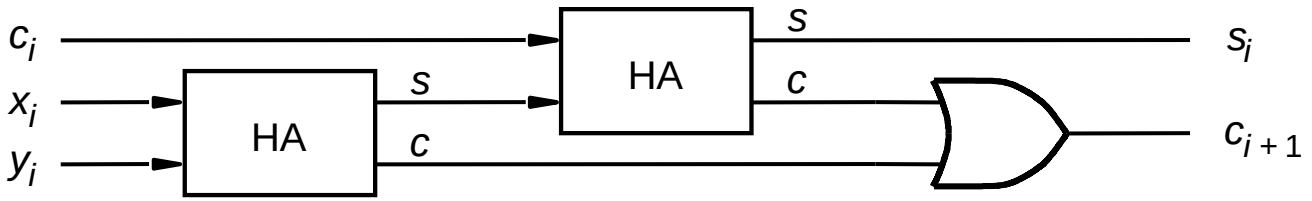


(c) Circuit

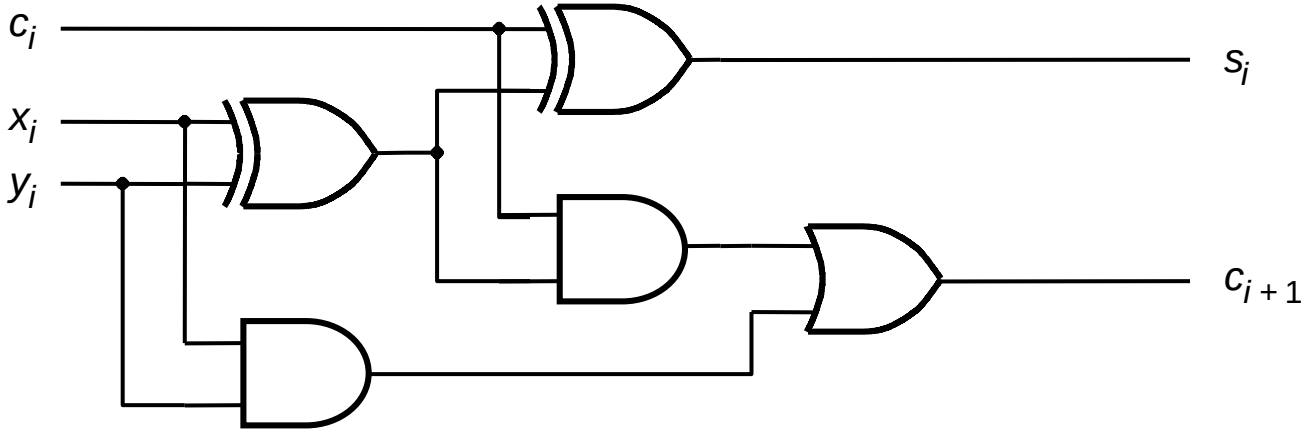


(d) Graphical symbol

Full Adder Circuit

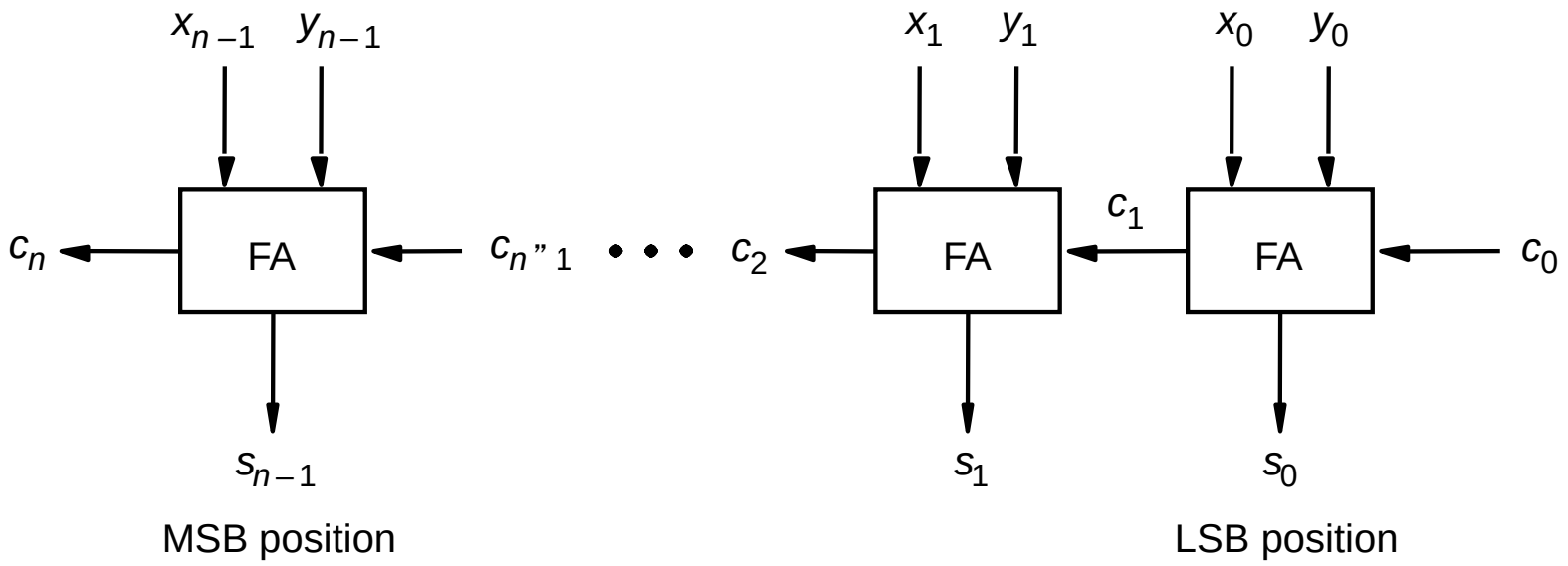


(a) Block diagram



(b) Detailed diagram

An *n*-bit ripple-carry adder



Denote by Δt time 1-Bit Full adder computes addition of two bits and carry.

Question: How much time it takes to compute the sum of two 32 bits words ?