Laboratory Project 2
Introduction to VHDL,
ModelSim and Quartus CAD software tools
using as an example digital Comparator circuits

(Detailed version)

Instructor: Professor Izidor Gertner

February , 2017

Objective:

1. Introduction to Hardware Description Language –VHDL.
2. Introduction to ModelSim CAD software tool for digital circuit simulation.
3. Testing digital circuits using a ***test bench*** file written also in VHDL using MODELSim.
4. Introduction to QUARTUS CAD software tool to design digital circuits and thereafter program Field Programmable Gate Array Device (FPGA CHIP) hosted on a DE2 board (no use of board until Part 6 in this tutorial)
5. Your task:
    a. Design digital comparator circuit to compare (1-bit, 2-bit, 8-bit) words.
    b. You have to describe comparator circuit using VHDL (we provide the working source code in VHDL).
    c. You have to write test_bench code in VHDL to test your design (we provide as an example working VHDL code) Simulate your design using ModelSim CAD software tool manually and using test_bench.
    d. Create new QUARTUS project using the using the VHDL code you simulated and verified for correctness using ModelSim Software.
    e. Make pin assignments of actual switches, keys on the DE board to input/ output ports in your design.
    f. Program FPGA device on the DE board using QUARTUS software and USB cable.
    g. Verify the correctness of your design on the FPGA device.
    h. Write a detailed report
    i. Create a video no longer than 2 min. The video should have a title page with identifying information, then your live face: you should say your name and what you are going to show. You have to be able to describe items a) through g) within 2 min.

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Remarks:
VHDL is intended for describing and modeling a digital system at various levels and is an extremely complex language. Then, we will use the design simulation tool ModelSim to design, and verify our VHDL designs. Modelsim is widely used in industry. Finally, we will run our designs in Quartus to program a FPGA device on the DE2 board.

To accomplish this goal we will use as an example
comparators (1-bit, 2-bit, 8-bit), described Hardware Description Language VHDL.

NOTE: In this lab you will design 1-bit, 2-bit and 8-bit comparators;

However, we will only show you how to do the simulation, testing and loading onto the DE2 board for the 1-bit comparator.

YOUR GOAL IS TO EXTEND 1-BIT COMPARATOR DESIGN CODE, SIMULATION PROCEDURE, and FPGA programming TO 2-BIT AND 8-BIT COMPARATORS

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1. INTRODUCTION TO VHDL

VHDL stands for VHSIC (Very High Speed Integrated Circuits) Hardware Description Language. It is a language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. For VHDL primer please refer to this link

http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html

Basic VHDL Example:

1-BIT COMPARATOR

One-bit Comparator Design

A one bit comparator is a circuit that can be used to compare two one-bit signals. The comparator outputs a '1' if the input signals are equal; otherwise, the comparator outputs a '0'.

As introduction to this course, we use a simple comparator to illustrate the skeleton of a VHDL program. The description uses only logical operators and represents a gate-level combinational circuit, which is composed of simple logic gates.

Input		Output
i0	i1	Eq
0	0	1
0	1	0
1	0	0
1	1	1

Figure 5. Truth table of a 1-bit comparator

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The truth table as shown in Figure 5 can be written using Boolean equation

$$Eq = (i_0 \; and \; i_1) OR \; (\overline{i_0} \; and \; \overline{i_1})$$

The complete VHDL code for the 1-bit comparator digital circuit is shown below:

equal.vhd

```
 1 Library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity equal is
 5         port ( I0, I1 : in std_logic;
 6                  Eq    : out std_logic);
 7 end equal;
 8
 9 architecture arch of equal is
10         signal p0, p1 : std_logic;
11         begin
12         EQ <= p0 or p1;
13         p0 <= (not I0) and (not I1);
14         p1 <= I0 and I1;
15 end arch;
```

As we said before, VHDL is case insensitive, which means that upper and lowercase letters can be used interchangeably, and free formatting, which means that spaces and blank lines can be inserted freely.

Lines 1 and 2 tell the compiler (in our case Quartus and ModelSim) which libraries to use. The libraries contain precompiled VHDL code. For example ieee.std_logic_1164.all contains the code for the 'or' function, and without it the VHDL compiler would generate and error on line 12.

Lines 4 to 7 are the entity declaration statements. The entity declaration outlines the input and output signals of the circuit. The mode term can be in or out, which indicates that the corresponding signals flow "into" or "out of" of the circuit. It can also be ***inout***, for bidirectional signals.

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Lines 9 to 15 are the architecture statements. The architecture body describes functions of the circuit. The architecture may include signals which we have used in line 10. We need the signals to store the value of first product and second product. You will understand signals more as you do more coding. The main description, encompassed between **begin** and **end**, contains three concurrent statements. Unlike a program in C language, in which the statements are executed sequentially, concurrent statements are like circuit parts that operate in parallel. The signal on the left-hand side of a statement can be considered as the output of that part, and the expression specifies the circuit function and corresponding input signals.

Notice that to translate our equation into VHDL code, we represented the term ***i0 . i1*** as ***p0***, and the term ***i0' . i1'*** as term **p1**. Then we say ***Eq = p0 + p1***. We can, of course, represent the equation in just one line of VHDL code; however, as our codes grow larger, it is better to break our assignments to make the code more readable and modular. This notion will become apparent as you work on bigger projects.

NOTE: Just like we have an *Eq* output, we can also have a *notEq* output that notifies when the inputs being compared are not equal. This is left for you as an exercise after you complete the tutorial part of this lab. See the YOUR TASK section towards the end of this lab for further explanation.

2. INTRODUCTION TO MODELSIM CAD Software Tool

2.1 ModelSim installation:

ModelSim is a multi-language HDL simulation environment by Mentor Graphics, for simulation of hardware description languages such as VHDL and Verilog. Simulation is performed using the graphical user interface (GUI), or automatically using scripts.

For this part you must have ModelSim installed in your computer. Altera gives you the choice to download ModelSim as bundle when you download Quartus from their website.

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- If you followed our tutorial on installing Quartus and ModelSim, you are ready to go and you can ignore the bullet point bellow. (Alternatively, if you haven't installed any of these programs, please follow our tutorial on Quartus and ModelSim download and setup, then come back to this lab).

- If you have Quartus installed but not ModelSim, you can download it independently from their website, just make sure you choose the same version of Quartus you already have in your computer before starting download. Go to:

  http://dl.altera.com/?edition=subscription&product=modelsim_ae#tabs-2

  The following shows the download page from Altera. It is important that you know which version of Quartus you have installed in your computer. If you don't know, open up Quartus, then go to **Help > About Quartus II**

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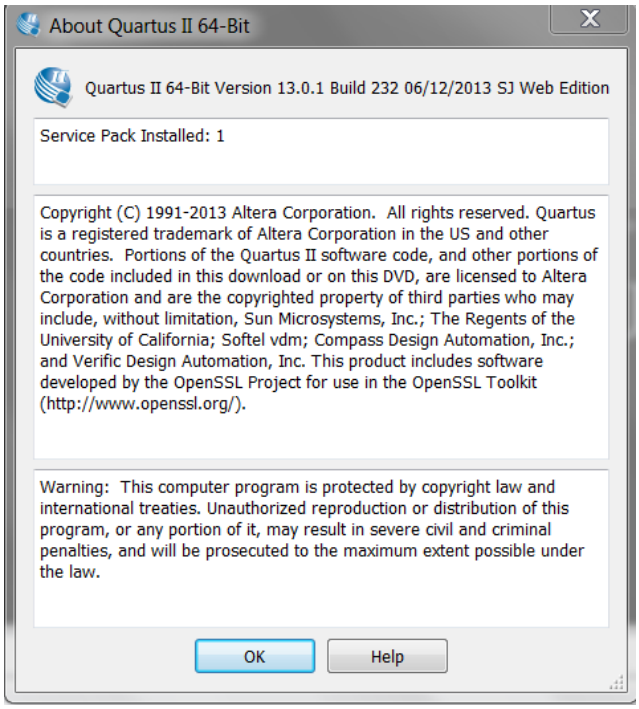

Figure 6. Screenshot of our Quartus version.
Our version is 13.0 service pack 1, yours may be different.

The next screenshot shows the download page for the Quartus software. Notice that at the top it says Subscription Edition although you may have downloaded the Free Web edition. This is irrelevant: it doesn't matter if it is part of the FREE or SUBSCRIPTION edition, ModelSim as a component is the same for both editions. Make sure you are logged into your Altera account (since you installed Quartus, we assume you have an account already with them).

CS 343, Spring 2017

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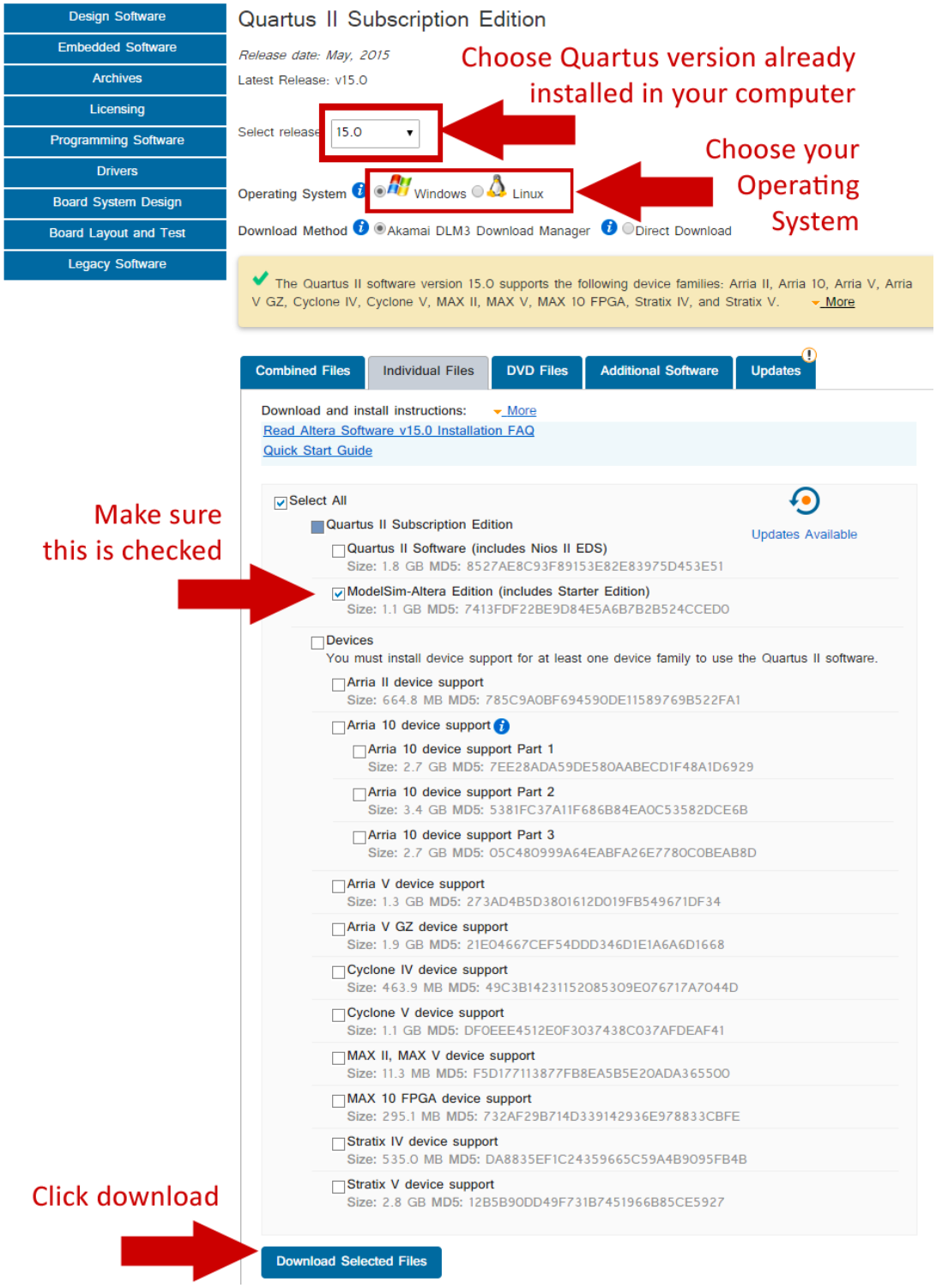

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Figure 7. ModelSim download page

2.1 ModelSim basics:

1. Open ModelSim. To run ModelSim, go to terminal and type vsim. This tutorial was done on a Windows environment, so we will show the corresponding Windows system screenshots but other operating systems should follow similar steps.

   If you are on Windows go to **Start > Run**. Type in “cmd” (without quotes) in the input field, then hit **Enter**. Alternatively, you could also search for Command Prompt in the search field in the Start Menu.
   If you are on Linux, right click your desktop and click Terminal.

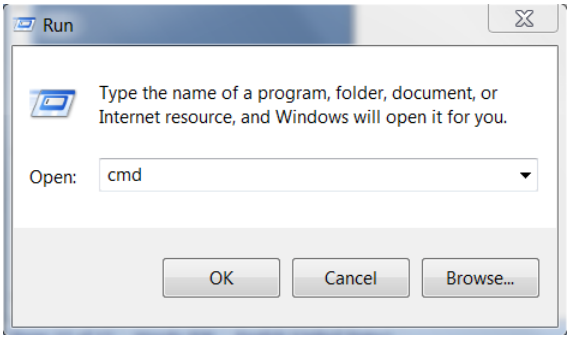

Figure 8. Run Command in Windows

2. In terminal type “vsim” (without the quotes).

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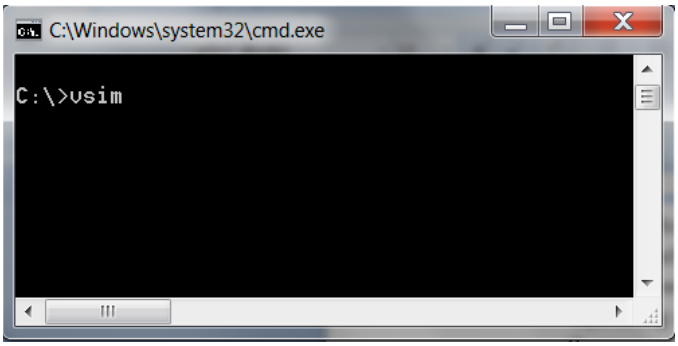

Figure 9. Terminal and ModelSim start command

You are now taken to the main screen of ModelSim, a Welcome splash screen will appear and you are now ready to start testing your circuit designs.
The initial screen of ModelSim is shown below:

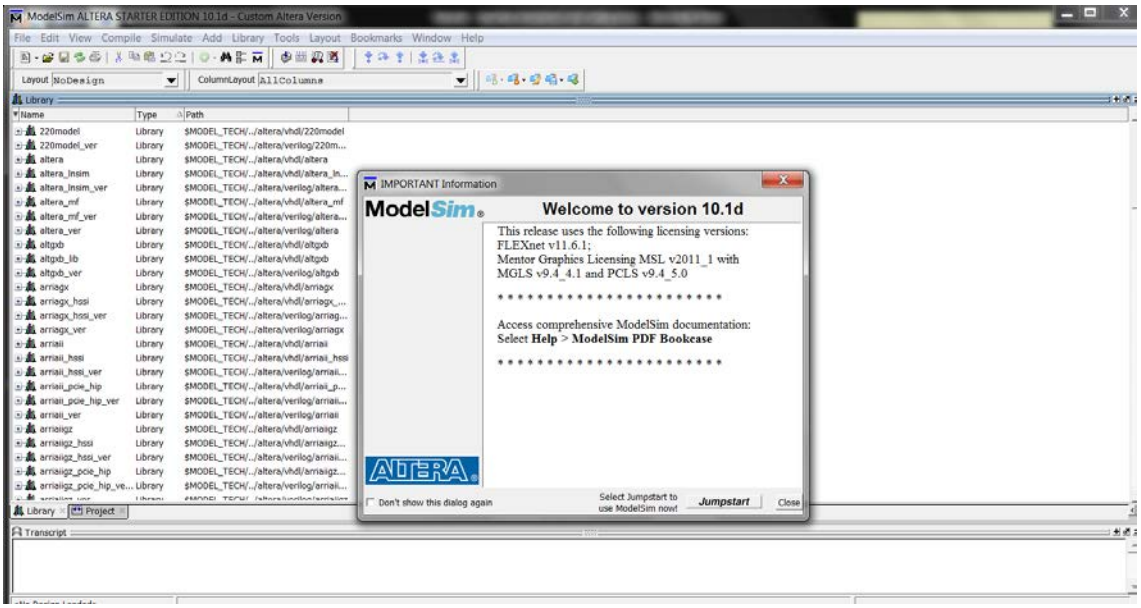

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Figure 10. ModelSim Welcome screen

3. When the Welcome screen appears, hit Close. Now go to Now go to File > New > Project. If a message appears asking if you want to close the current project just accept.
4. The Create New Project dialog appears, enter a name for your project, you can call it **one_bit_comparator**. See figure 11.
5. Browse a location for your new project.
6. In the Default Library Name, if empty, call it **work**.

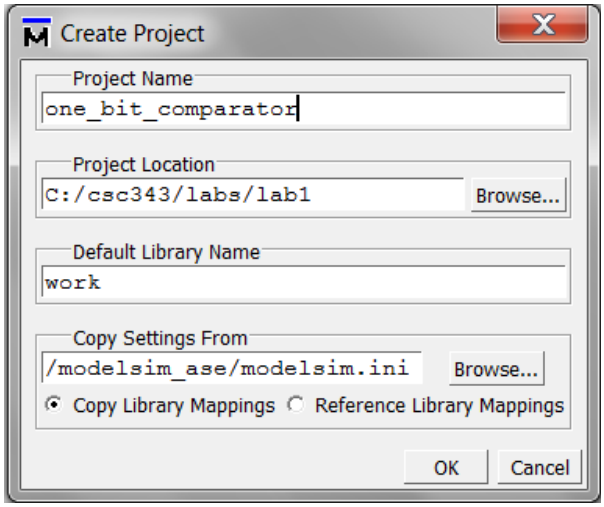

Figure 11. Create New Project dialog in ModelSim

7. The Add items to project dialog appears (See figure 12). In the previous section we described the comparator we are going to implement and we gave you the VHDL code for it. Right now we are going to create a new VHDL file and copy-paste the given code to it. Click **Create New File**.

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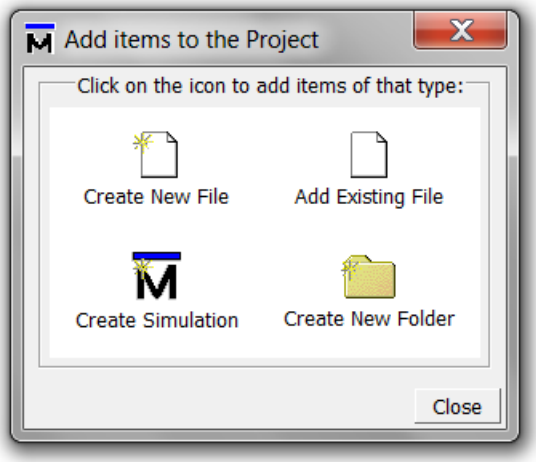

Figure 12. Add items dialog

8. The Create Project File dialog appears, see figure below. In the File Name field enter **equal**, then hit OK.

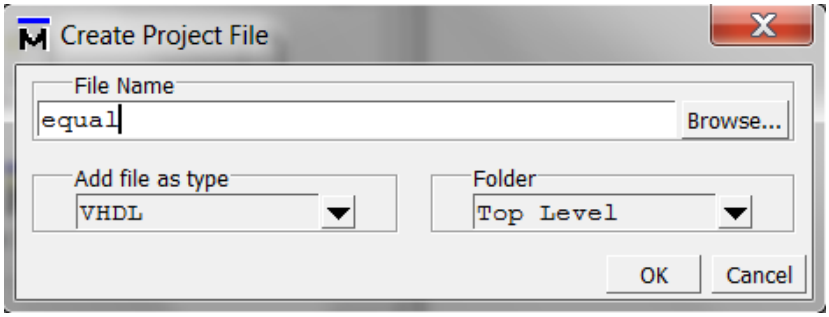

Figure 13. Create Project File dialog

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9. Right click the file equal.vhd you just included, and then choose **Edit**.

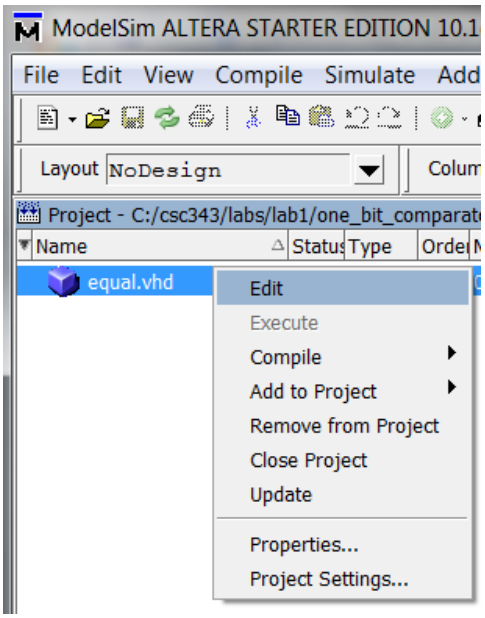

Figure 14. Project navigator in ModelSim with the equal.vhd file

10. A panel with a code editor appears. Copy and paste the code given in the previous section of this lab for the one-bit comparator, called equal.vhd
11. Save this file by going to **File > Save**.
12. In the project navigation panel, right click the equal.vhd file and choose **Compile > Compile Selected**

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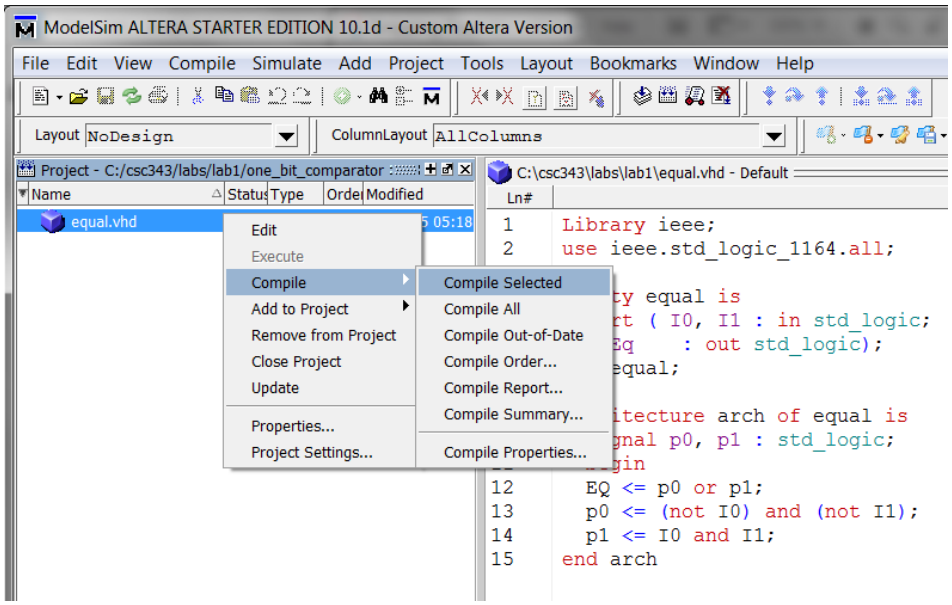

Figure 15. Code editor in ModelSim and Compilation options

13. At the bottom of the main ModelSim window you should see a Transcript panel, it will output a message to notify you if the compilation was successful or of any errors. Also, next to the name of your file you should see a **Green Checkmark** if the file is compiled or a **Blue Question Mark** if it is not.

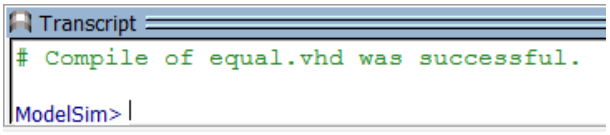

Figure 16. Transcript panel – Compilation successful

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14. Go to **Simulate > Start Simulation…**

15. A dialog appears, browse the "work" Library which is (by default) the library we told ModelSim to store the file we wanted to have imported. Select the **equal** entity and click OK.

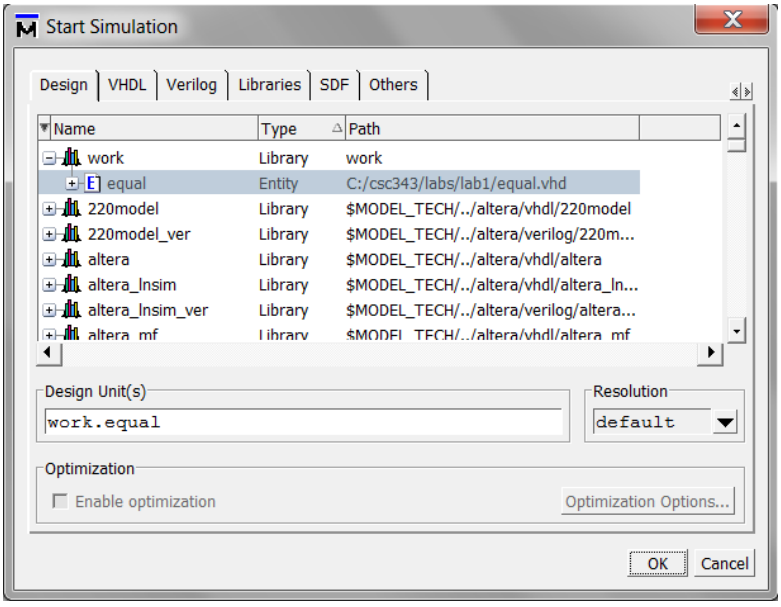

Figure 17. Choosing equal entity which will be simulated

Note: at this stage you are allowed to select multiple files, let's say if you had a one-bit-comparator and a two-bit comparator and want to simulate and compare both, if you have the VHDL files ready in your work Library you can select both and they will be included in your simulation configuration. For now we only have a equal.vhd file which is our one-bit comparator, so we are adding only one file.

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16. ModelSim should arrange its layout automatically to allow for simulation. At this point you should have something similar to figure 18. With your mouse, select the one-bit comparator inputs (i0 and i1) and output (Eq) and drag them to the wave panel as you see in the picture:
17. If you do not see **wave panel go to VIEW -> wave and select wave.**

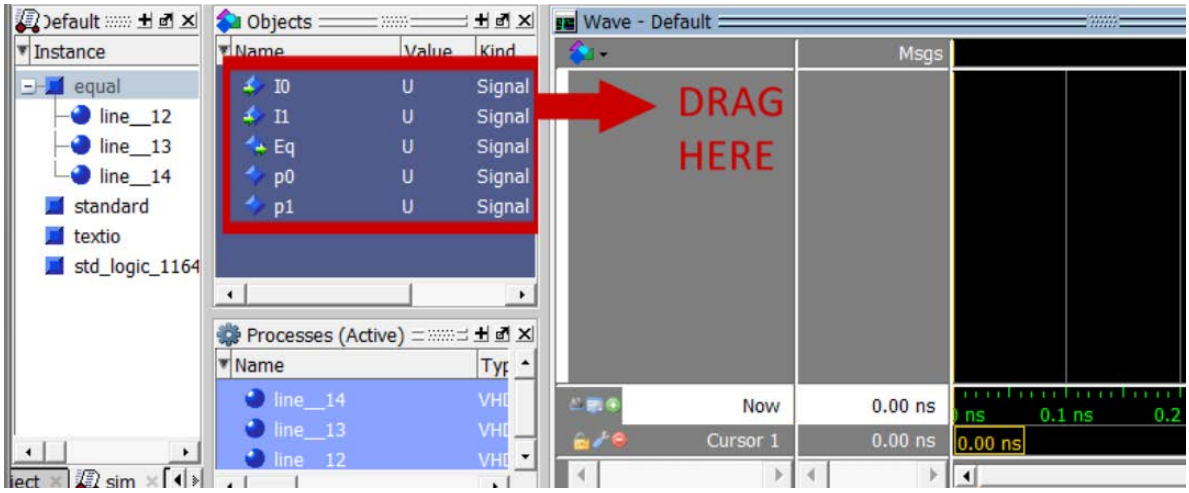

Figure 18a. Dragging inputs and outputs to waveform panel

After the move you should see something like

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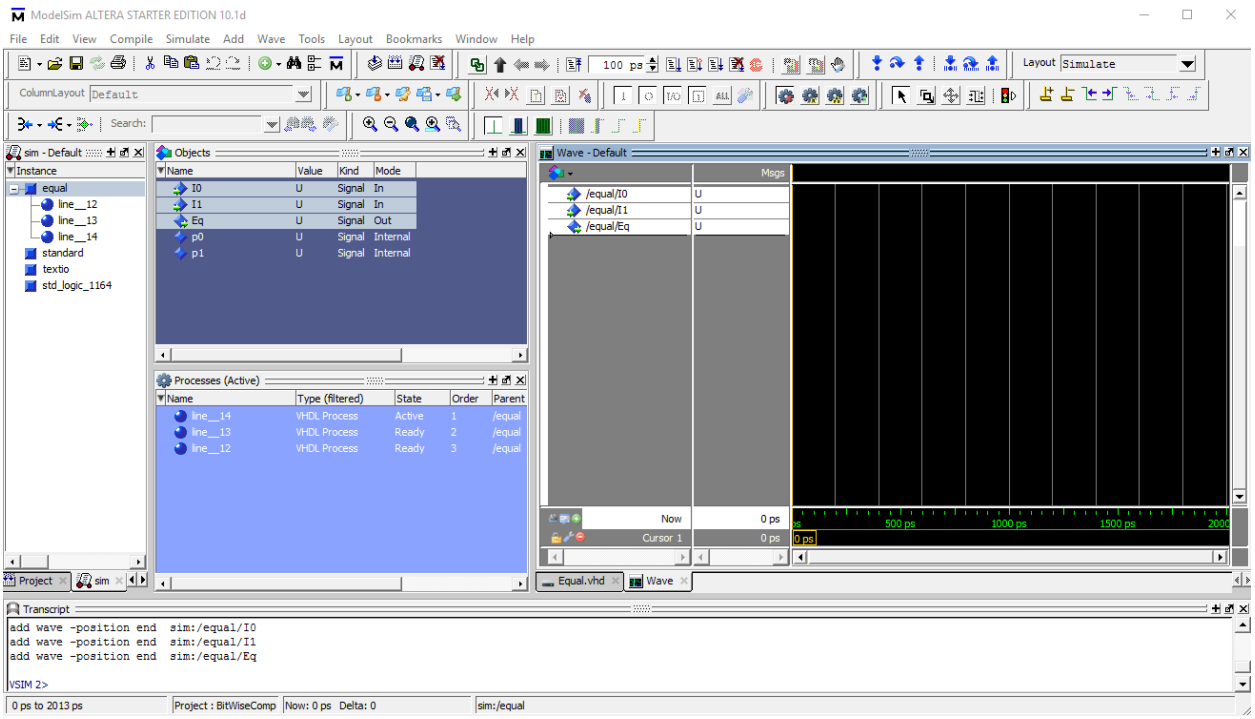

Alternatively, you could also right click on the name of the VHDL file as shown in Figure 18b and click **Add Wave**

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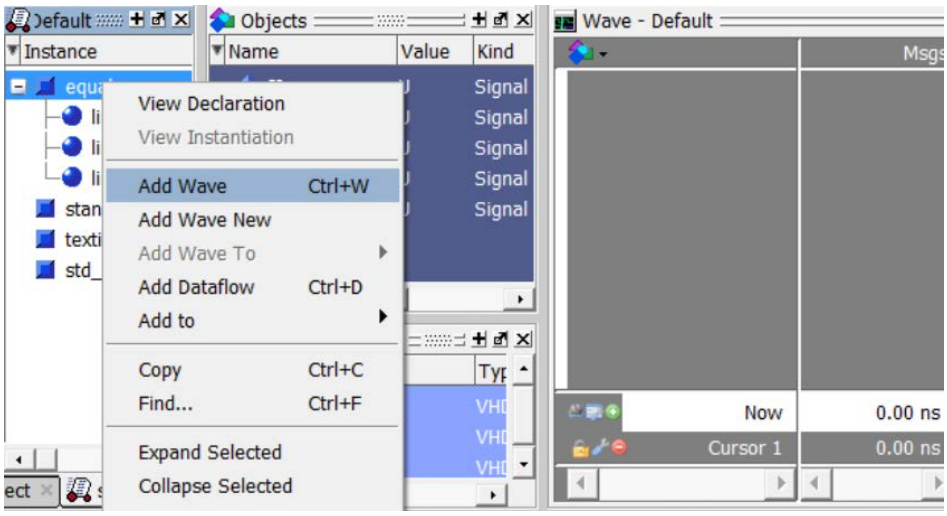

Figure 18b. Adding inputs and outputs through menu to waveform panel

18. Now that you have your inputs and outputs in the waveform, it is time to give them values to simulate. Note that a "U" (Undefined) appears to every input/output of your wave list. This means that no value has been set for these. To give a value to an input signal, right click the first input (i0) then select **Force**.

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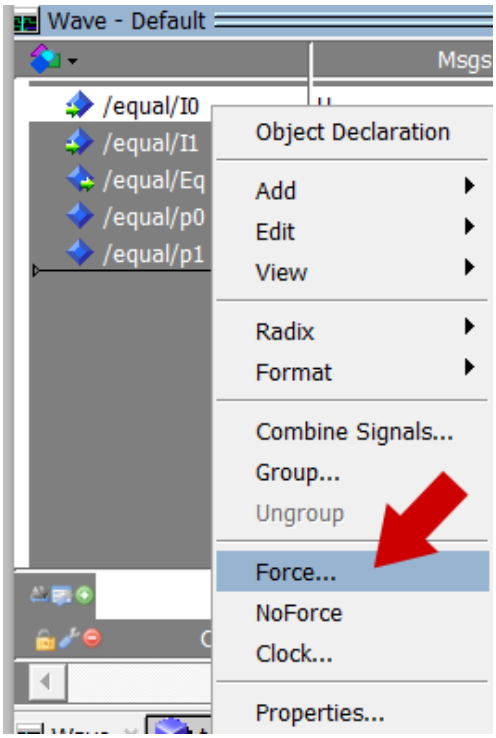

Figure 19. Force values option

19. When the dialog appears, change the Value from U (undefined) to 0. Click OK.

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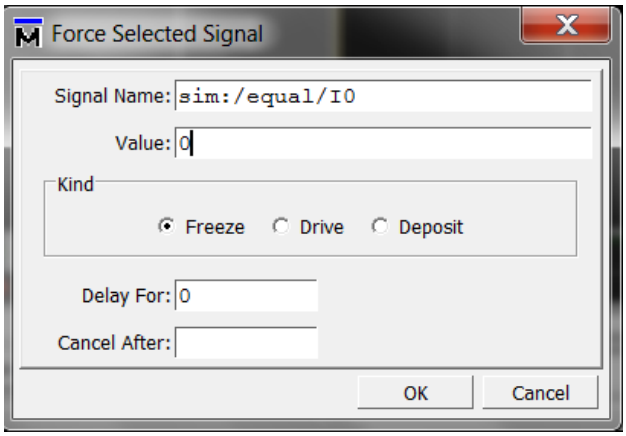

Figure 20. Force Selected Signal dialog

20. Do the same for input i1. Right click it, choose **Force**, and give it a value of 0 as well.

21. Next, it is time to simulate given the initial values of i0=0 and i1=0. Hit F9, hit the Run button (not Run All) or go to **`Simulate > Run > Run 100`**.

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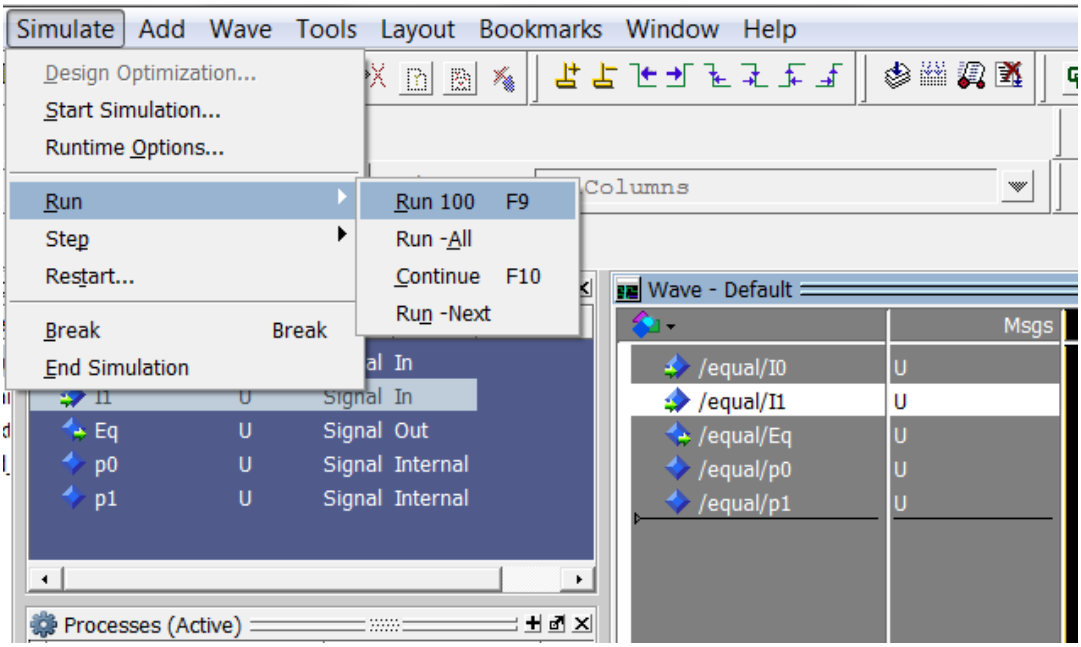

Figure 21. Run options

In case you need to restart your simulation, and thus, clear the input values you assigned, you can do so by clicking the Restart button. When the restart dialog appears hit **OK**.

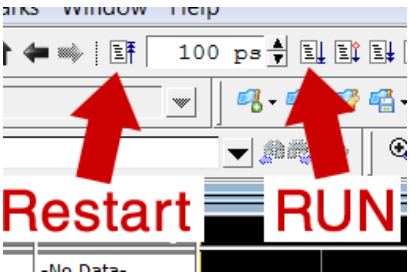

Figure 22. Run/Restart buttons in Menu bar

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22. You should obtain the following result in the waveform panel after your first 100ps run shown in figure 23. Notice how i0 and i1 have a value of 0, Eq has a value of 1 now, which is expected since in this case i0=i1.

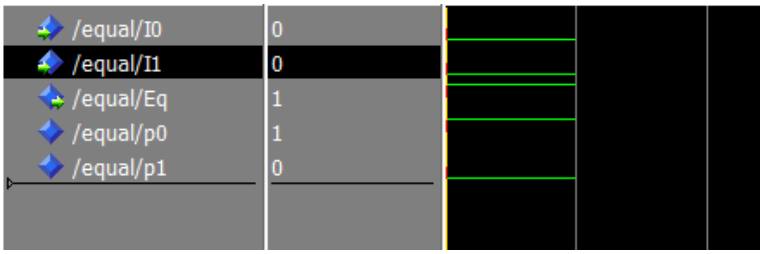

Figure 23. Result of first run after forcing values i0=0, i1=0.
Note Eq=1 since the values of the inputs are equal

23. Keep running the simulation with different values. This time right click on i0, select **Force** and give it a value of 1. Then hit F9 or hit the run button. You should obtain the following waveform:

Figure 24. Waveform result after second run

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Note that i0 has the value of 1 that we assigned, i1 kept its value of 0 from the prior stage of the simulation that we did in the previous step, and Eq has a value of 0 now, which is expected since i0 and i1 do not match.

24. Finish the simulation by testing all possible value combinations of i0 and i1 according to the truth table given at the beginning of this lab. We are now going to create a test file in ModelSim, so do not close your project.

25. Close the simulation by going to **Simulate > End Simulation**.

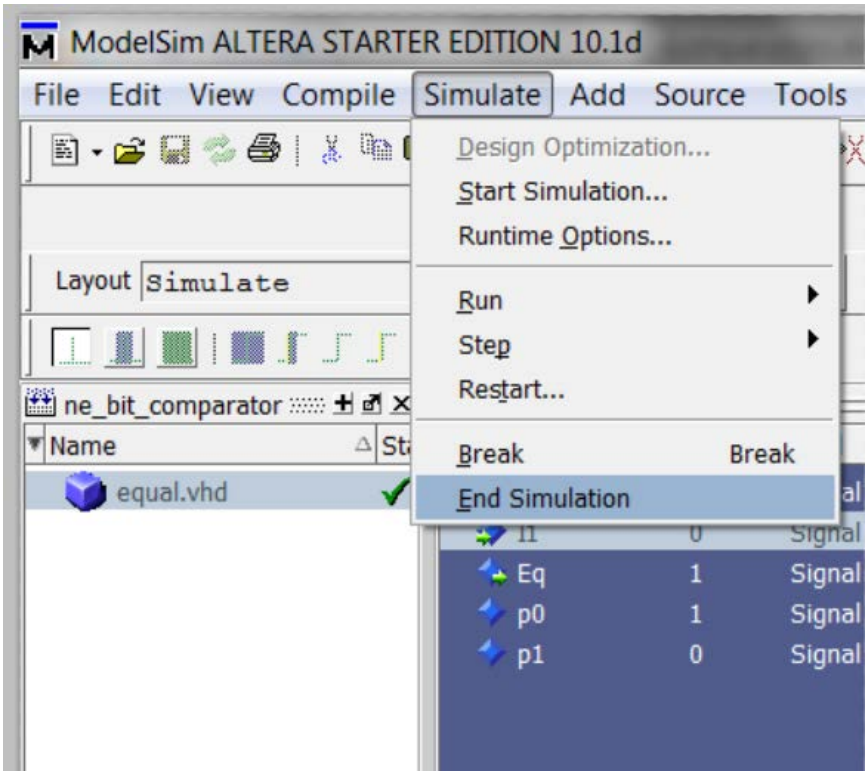

Figure 25. Ending simulation

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3. USING A TEST BENCH FILE IN MODELSIM

3.1 Test bench idea

After the code is developed, it can be simulated in a host computer to verify the correctness of the circuit operation and can be synthesized to a physical device (DE2 board for example). As we showed you in the previous section, a simulation can be done without a test bench but it is more professional and exact to use a test bench because you will have better control over your simulation.

3.2 Test file

We create a special program, known as a **test bench,** to imitate a physical lab bench. Here's the test file for the one-bit comparator:

test_equal.vhd

```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity test_equal is
 5 end test_equal;
 6
 7 architecture arch_test of test_equal is
 8 component equal
 9 port ( I0, I1 : in std_logic;
10        Eq    : out std_logic );
11 end component;
12
13 signal p1, p0, pout : std_logic;
14 signal error        : std_logic := '0';
15 begin
16 uut: equal port map (I0 => p0, I1 => p1, Eq => pout);
17 process
18 begin
19 p0 <= '1';
20 p1 <= '0';
21 wait for 1 ns;
22 if (pout = '1') then
```

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```
23          error <= '1';
24  end if;
25  wait for 200 ns;
26  p0 <= '1';
27  p1 <= '1';
28  wait for 1 ns;
29  if (pout = '0') then
30          error <= '1';
31  end if;
32  wait for 200 ns;
33  p0 <= '0';
34  p1 <= '1';
35  wait for 1 ns;
36  if (pout = '1') then
37          error <= '1';
38  end if;
39  wait for 200 ns;
40  p0 <= '0';
41  p1 <= '0';
42  wait for 1 ns;
43  if (pout = '0') then
44          error <= '1';
45  end if;
46  wait for 200 ns;
47
48  if (error = '0') then
49          report "No errors detected. Simulation successful" severity
50  failure;
51          else
52                  report "Error detected" severity failure;
53  end if;
54
55  end process;
56  end arch_test;
```

Read and try to understand the test file as much as you can. This test file declares “equal” (line 8) as a component and uses it without defining – it assumes that “equal” is defined somewhere else and we are just using this functionality (line 16) to test for specific cases or values. For example, you see that p0 and p1 are given specific values at certain time intervals and, assuming we know what value that should be produced, we test the result for the opposite value. If that incorrect result is reached, then we know we have an error and a message is displayed to the user.

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3.3 Running the simulation

1. With the one_bit_comparator project open, click on the Project tab (see figure26). Afterwards, Right click on an empty space in the project navigation panel. Then select **Add to project > New File…**

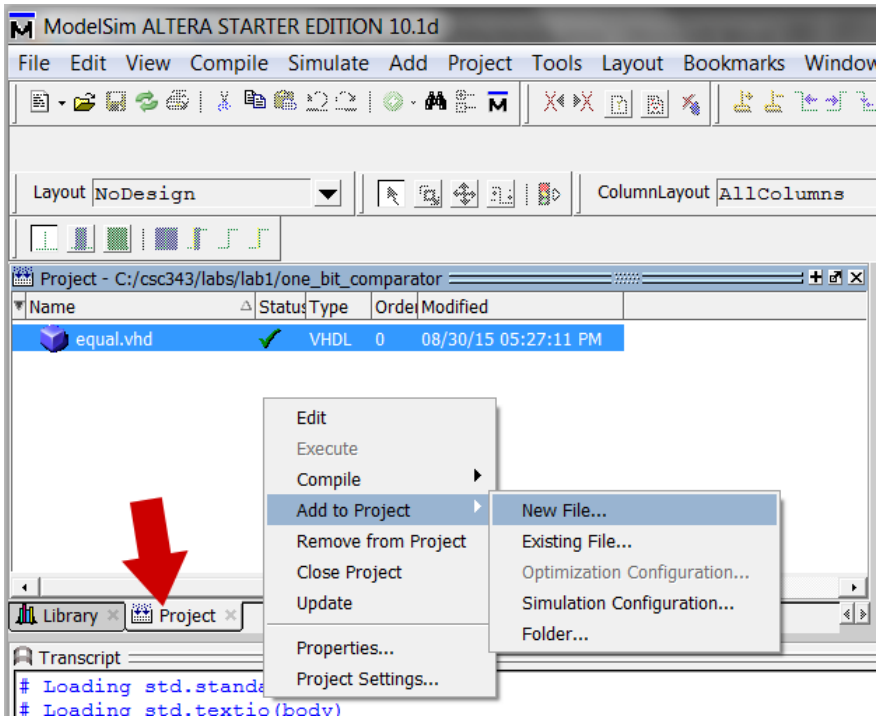

Figure 26. Creating a new VHDL file

2. The Create Project file dialog appears. In the input field for File Name enter **test_equal**, then hit OK.

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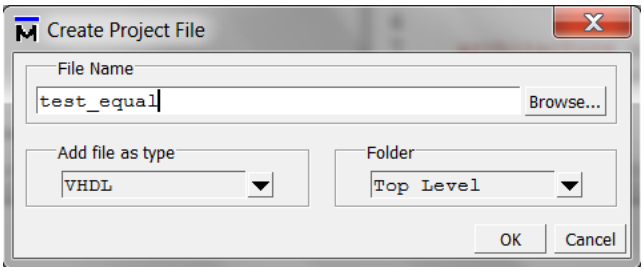

Figure 27. Giving a name to our new file

3. The newly created file appears in the project panel. Right click the test_equal file and choose **Edit**.

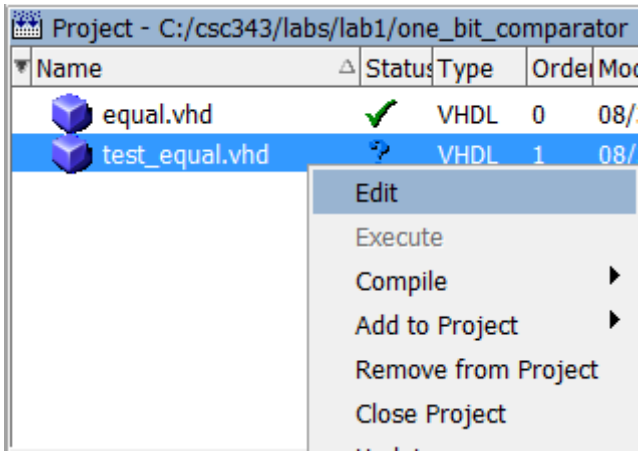

Figure 28. Editing the file

4. The code editor panel appears, copy and paste the code we gave you for the test_equal.vhd file.

5. Save the changes to this file. Go to **File > Save**.

6. Before we simulate, we need to compile this file. **Right click** on test_equal.vhd, then choose **Compile > Compile Selected**.

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7. The question mark that was there previously has turned into a green checkmark. This means our file has been compiled correctly and you should be ready for simulation. If you run into compilation problems, make sure you are copying the code correctly.

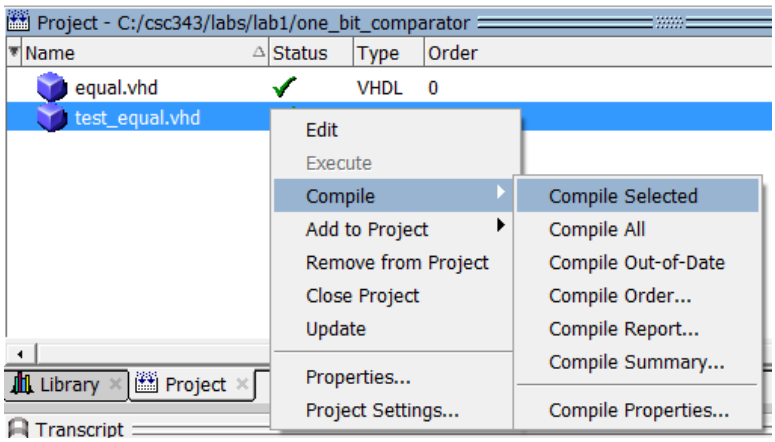

Figure 29. Compiling the test_equal.vhd file

8. Time to simulate. Go to **Simulation > Start Simulation**. The Simulation dialog appears so you can choose which entity to simulate. Expand the work library we created in the previous section, then select test_equal and click **OK**.

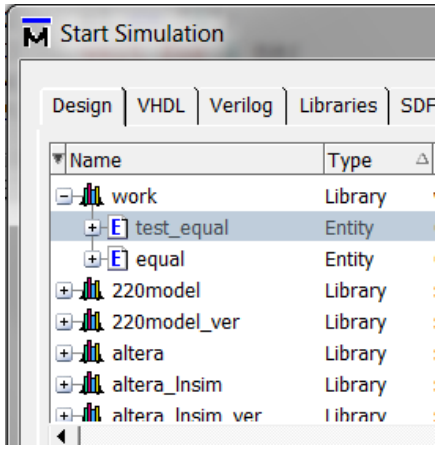

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Figure 30. Choosing the test_equal entity

9. Starting the simulation will configure ModelSim to the simulation layout. This will give you the screen shown below:

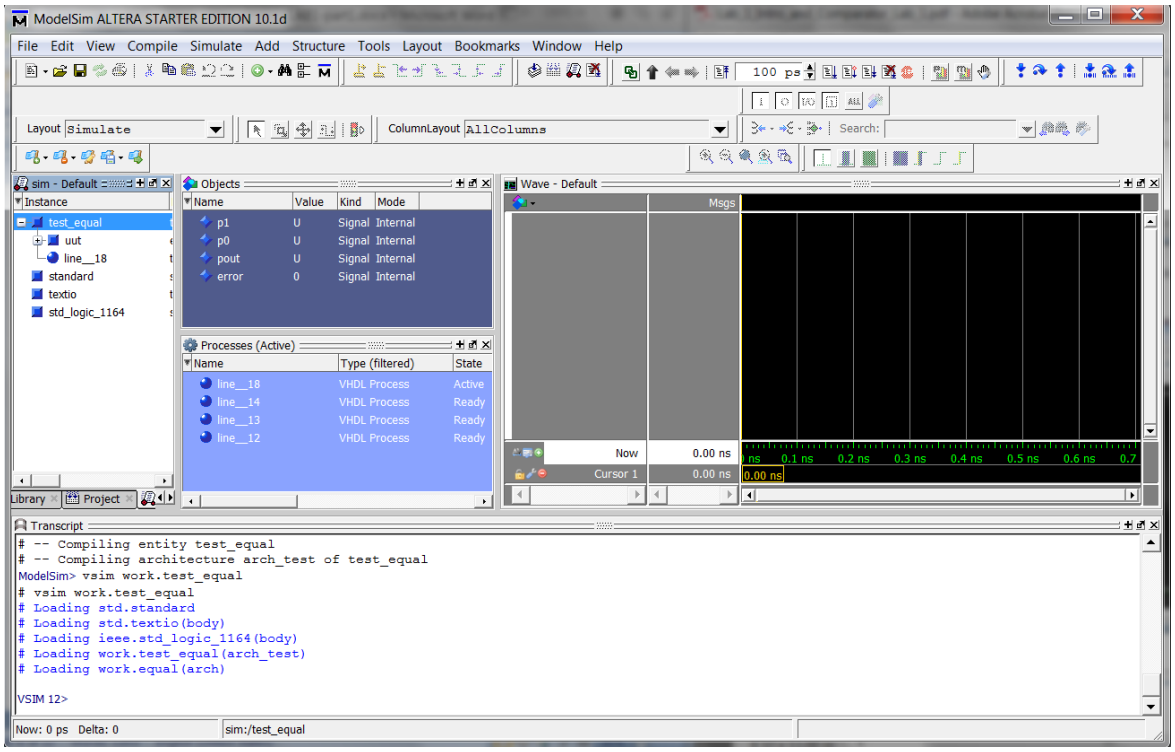

Figure 31. Simulation environment for test_equal

10. This should be familiar to you now. It is time to add the inputs and outputs as we did for equal.vhd file. Right click on test_equal in the instance window and select **Add Wave**. Alternatively, you can also right-click **test_equal** and do select **Add to > Wave > All items in region**. Your screen should look similar to the picture below with inputs and outputs populating the waveform screen on the right pane.

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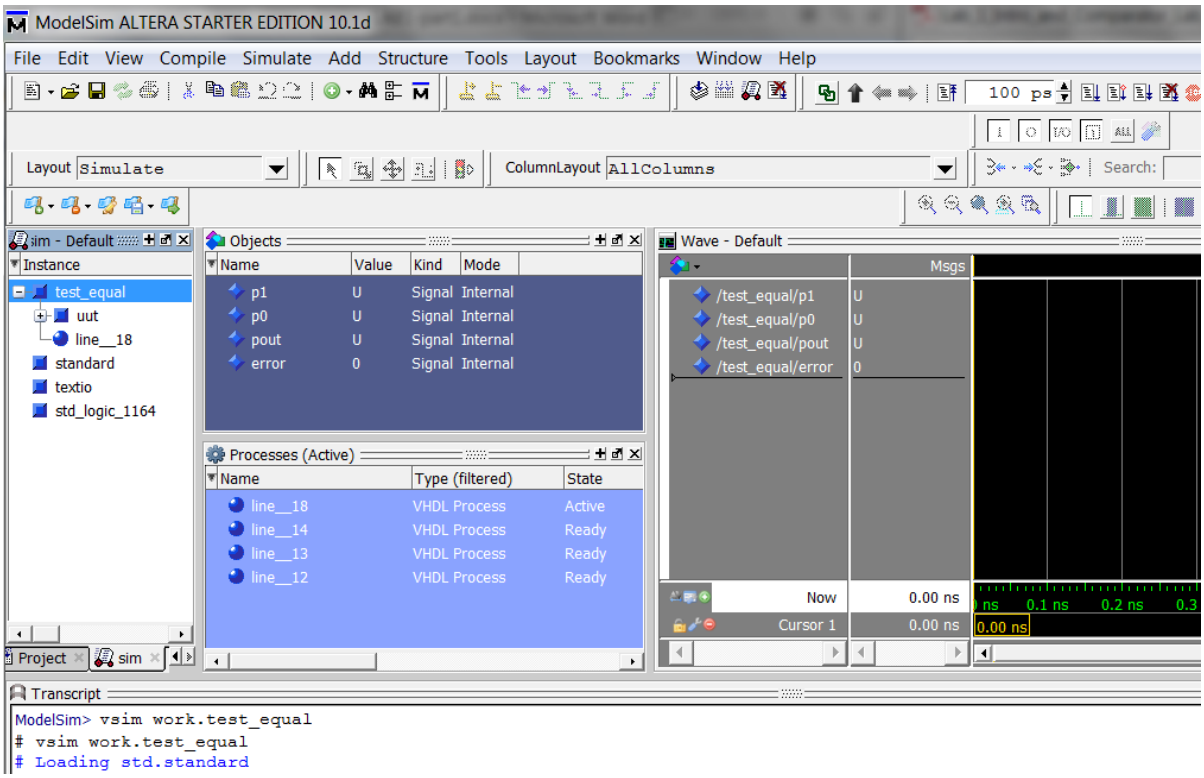

Figure 32. Inputs and outputs added for simulation

11. To run the simulation, click on the “Run All” icon. Normally a simulation will run until the “Break” icon is pressed, however in our test file the simulation is forced to terminate after a short period of time.

Figure 33. Run All and Break buttons in Main ModelSim Menu bar

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12. After simulating your design you will see a waveform in the wave window, you may have to close the ModelSim text editor to see it, or click on the Wave tab at the bottom of the pane (see figure below). You can zoom in or zoom out to observe your results. To see all the values of your run right click anywhere in the black pane and choose **Zoom Full** (see figure).

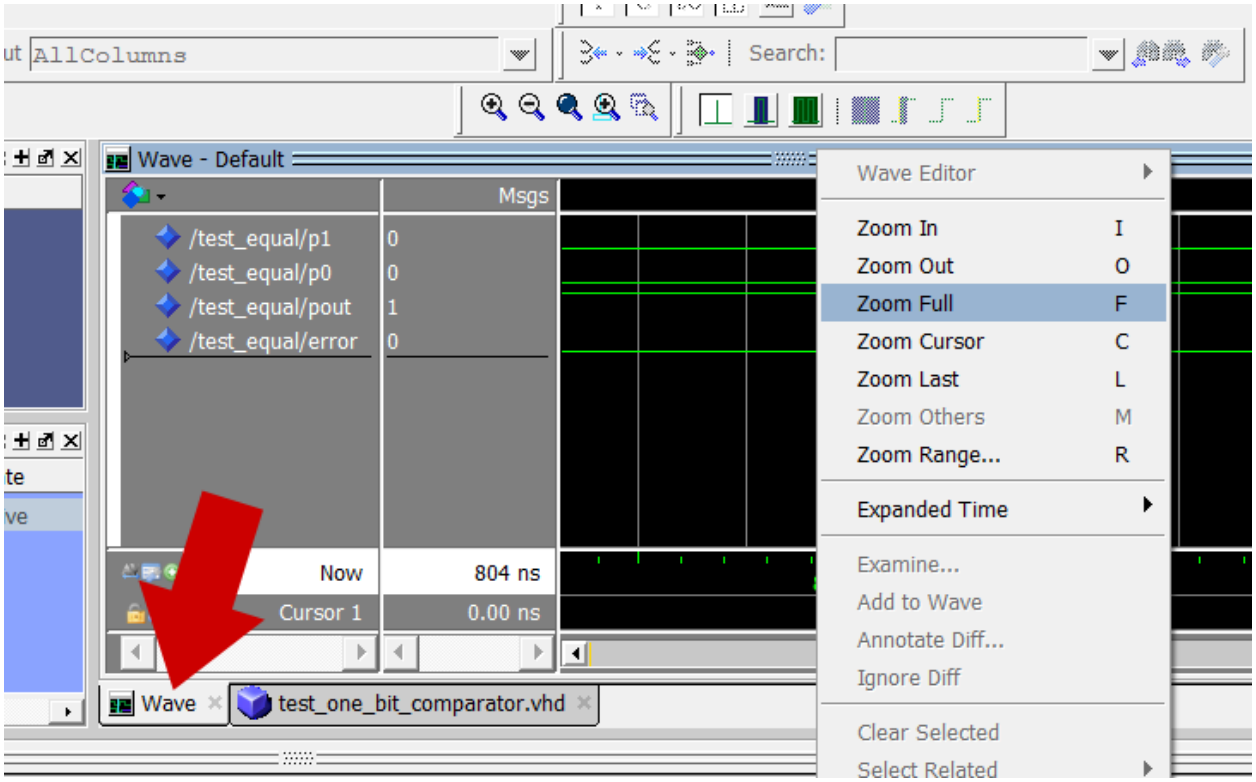

Figure 34. The Wave tab and full zoom of your waveform

The values you have gotten may not be exactly like the picture below. Analyze that your results are correct based on the truth table. Use the yellow scrollbar to scroll through the values. In the Msgs section you see the values each input/output takes (0 or 1) as you scroll through the waveform.

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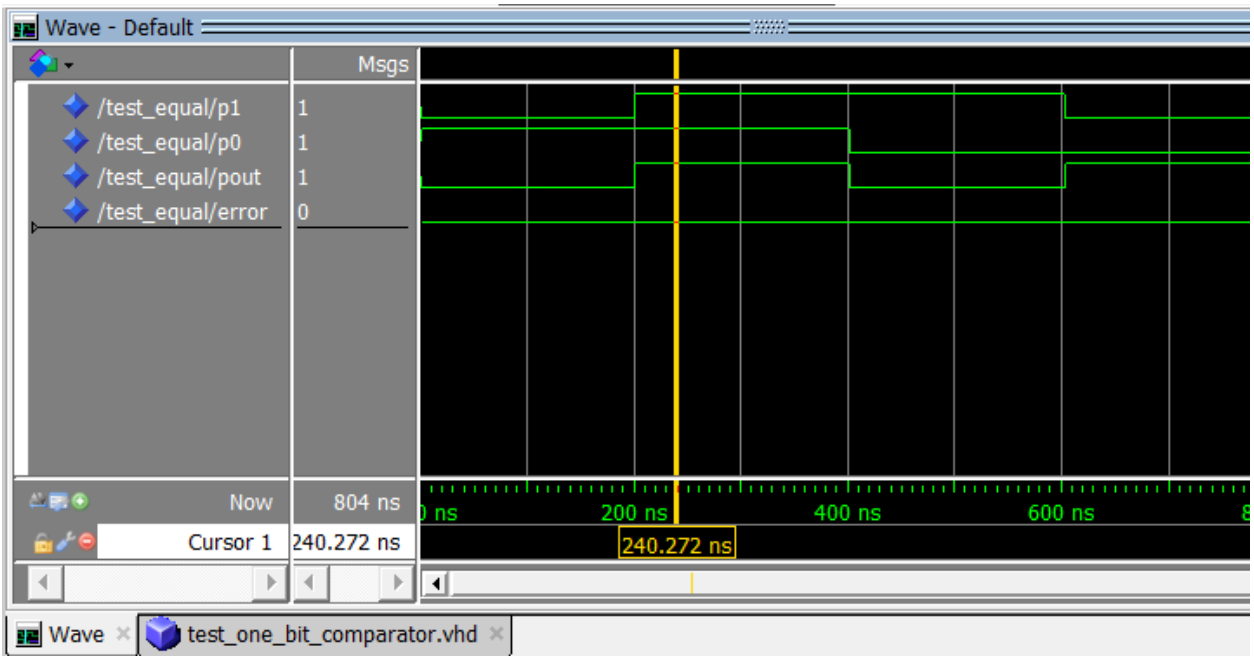

Figure 35. Completed waveform simulation of Test bench

The test code also produces a report in the transcript window on the bottom of the screen. If no errors are found it report that simulation was successful, else is report that an error was detected. You can use the error signal in the waveform to see at what exact point the error was found. Here is how a successful simulation would look like.

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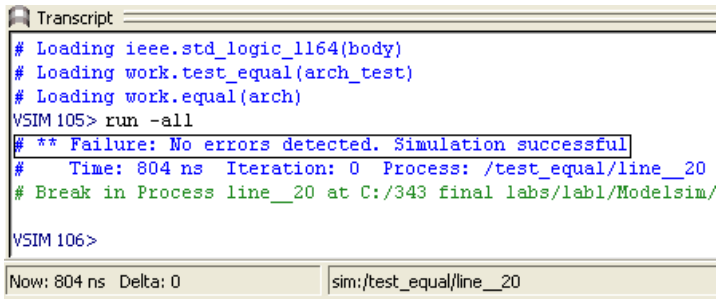

Figure 36. Successful simulation transcript

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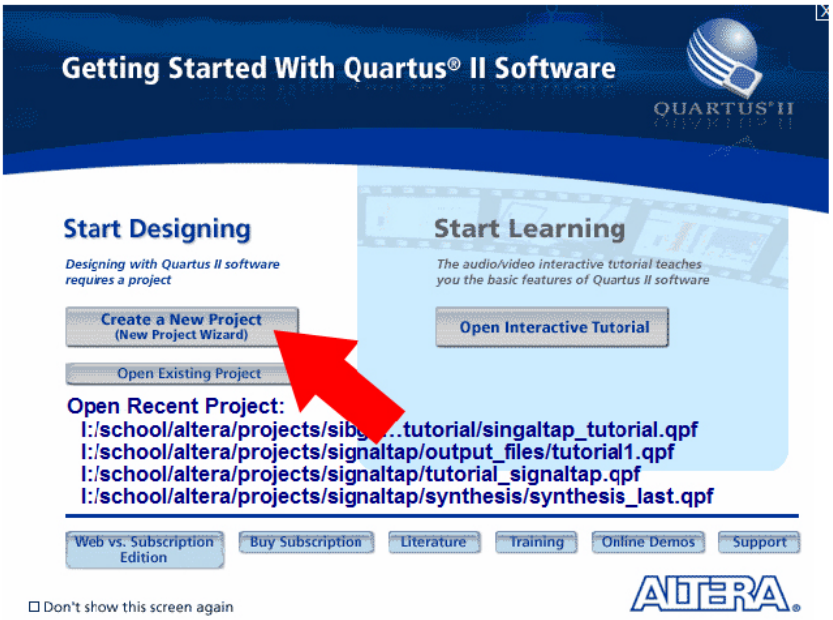
4. USING QUARTUS TO PROGRAM YOUR DESIGN ONTO FPGA DEVICE HOSTED on DE2

4.1 Creating a new Quartus project

Now that we have our code working and tested for correctness, it is time to load our design into the DE2 board.

Start the Quartus software from your program files. Quartus creates a shortcut in your Desktop during installation). The Quartus program starts up with the following screen with the options to create a new project or open an existing project. Click Create new Project



Alternatively, you can create a new project by going to **File > New…**

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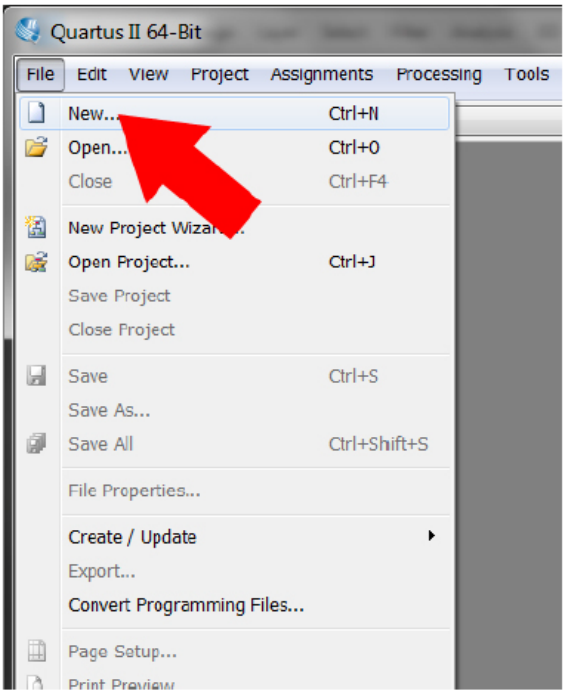

The following window appears, select **New Quartus II Project** option

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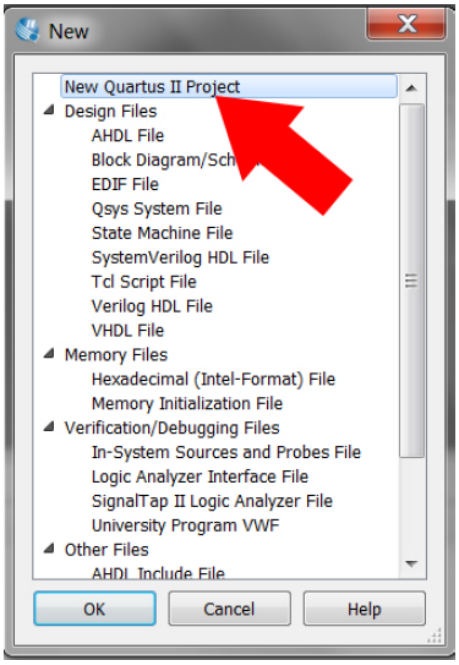

Once you create a project, the following screen for project wizard appears. Click **Next**

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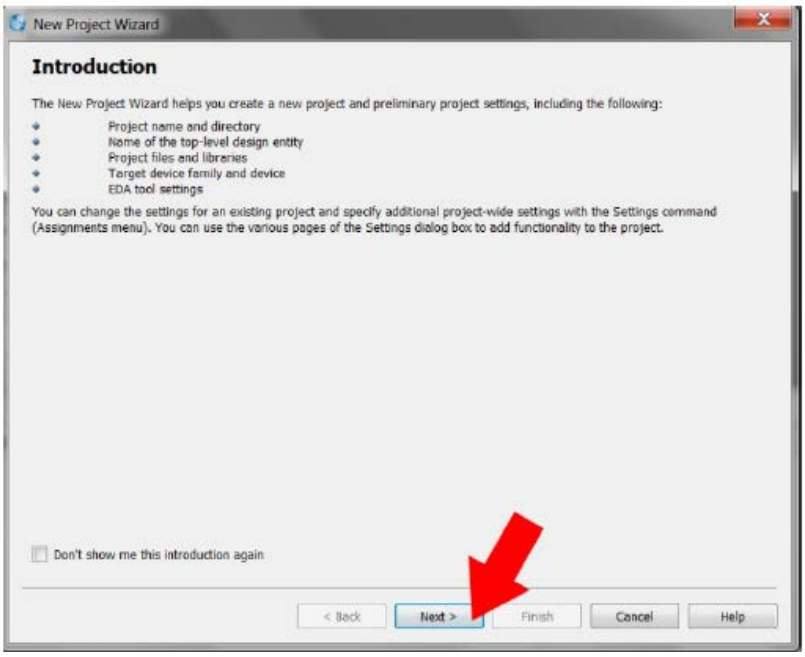

The screen for setting up your project location and name appears. The working directory in the picture below was chosen by preference. The default location would have been in the installation directory. Each version upgrades of Quartus creates a separate installation folder. Hence, it is advisable to have a separate folder for Quartus projects. This choice is left to the user. Enter the project name, in our case we decided to call it **comparator** (you can call it any name you prefer). Do not worry about filling up the field for the top-level design entity for now. For now we will let Quartus take the project name as the top-level design for your project by default.

Once you fill up the required info indicated by the arrows below, hit **Next**. If Quartus asks you if you want to create a new folder if the location does not exist, click Yes. Skip the next screen on adding files and proceed to the screen on setting family and device settings.

When choosing the working directory for your project in Quartus you can choose the same project you created for doing your simulations in ModelSim or you can create a new one, it is a matter of preference.

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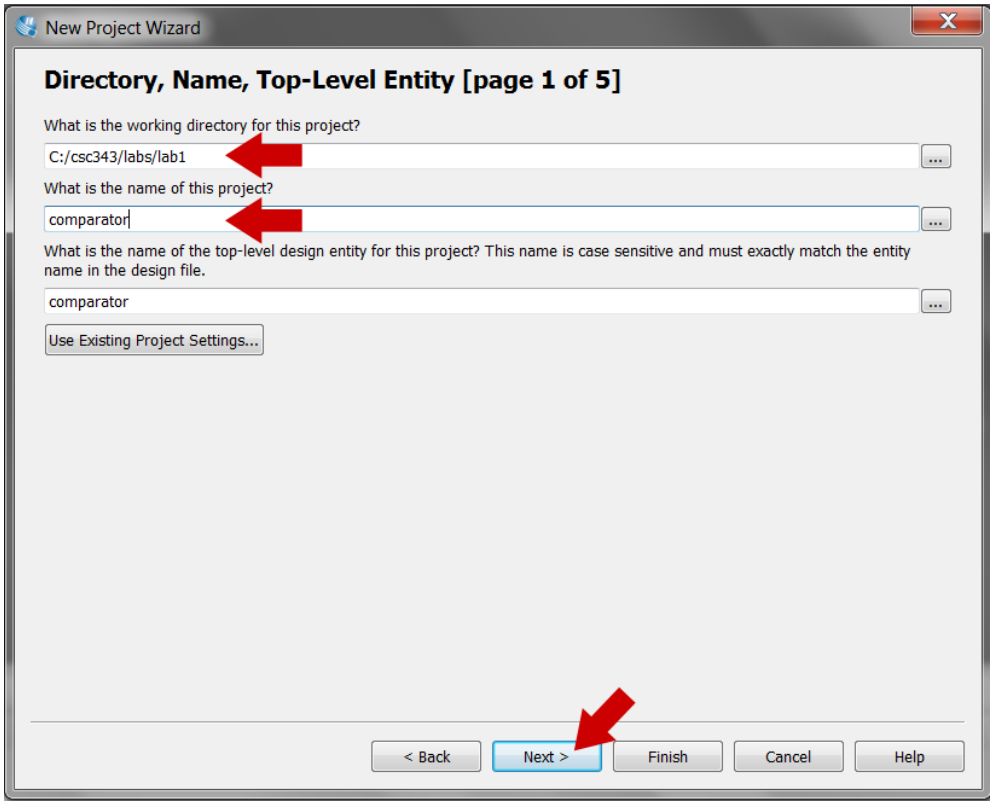

Altera has a long list of FPGA chips including Flex10k, Max7000, Stratix, Cyclone (I, II, III). In our labs we will use the DE2 board which comes with the Cyclone II chip on it. For this lab and all subsequent assignments in this series, please choose the following:

- In the Device Family dropdown menu:

  Cyclone II

- In the Available Devices box:

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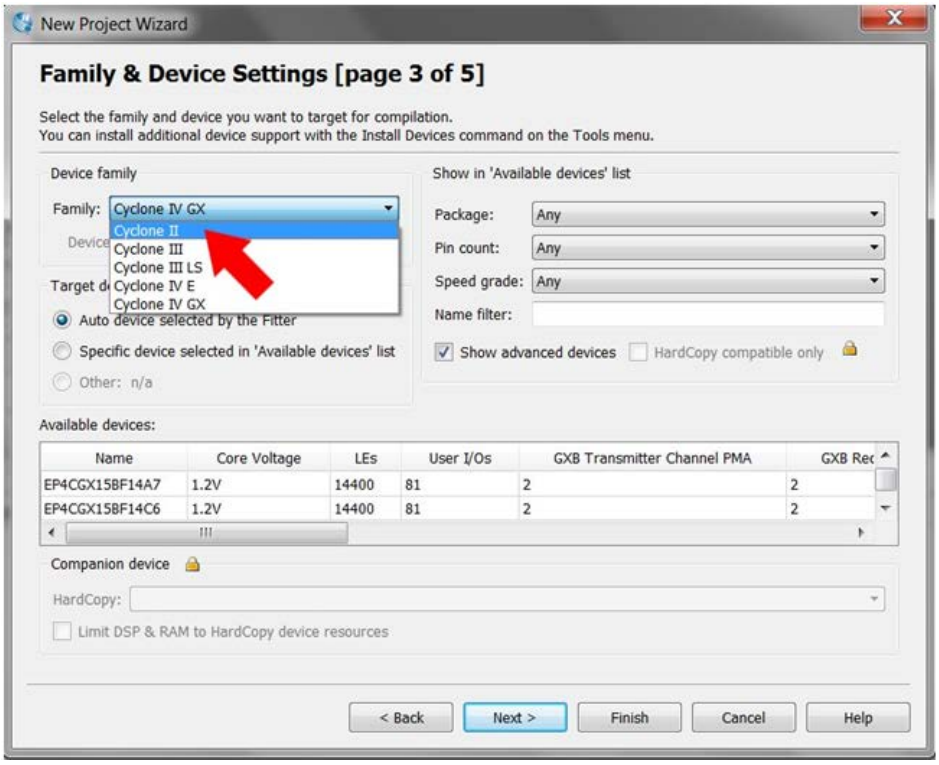

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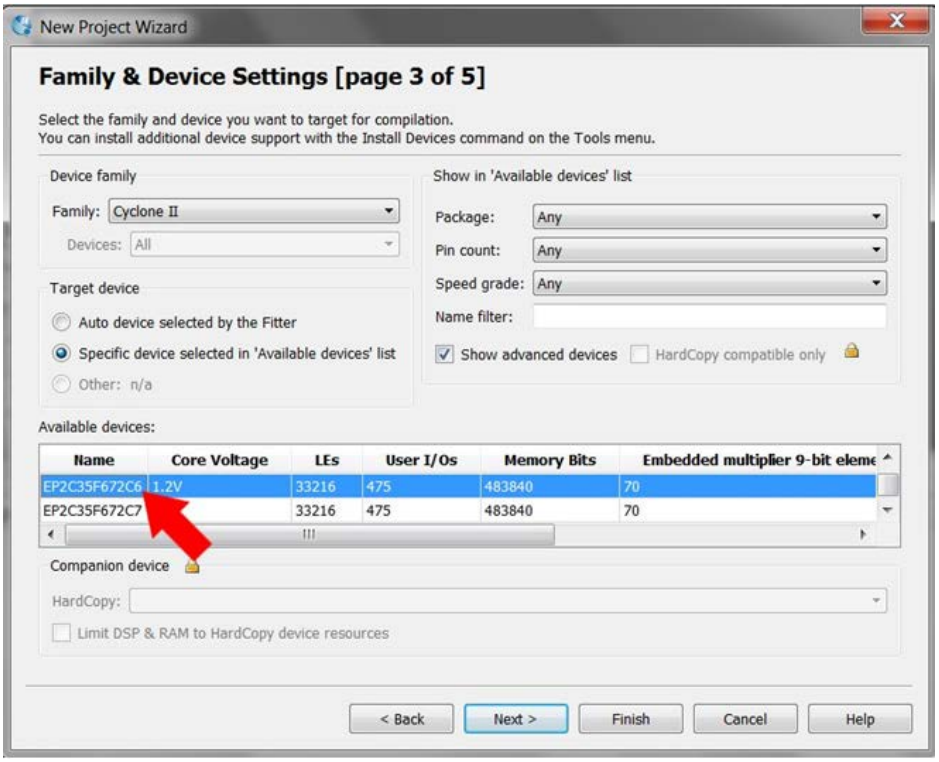

After you are done selected your options for the device, click **Next**. You are presented with a screen for EDA Tools Settings. We do not need these tools for our tutorials. Make sure that the options in your screen look similar to the picture below. If you have ModelSim Altera in your Simulation field, change it to **None**. Now we are done setting up our project. Click **Finish**.

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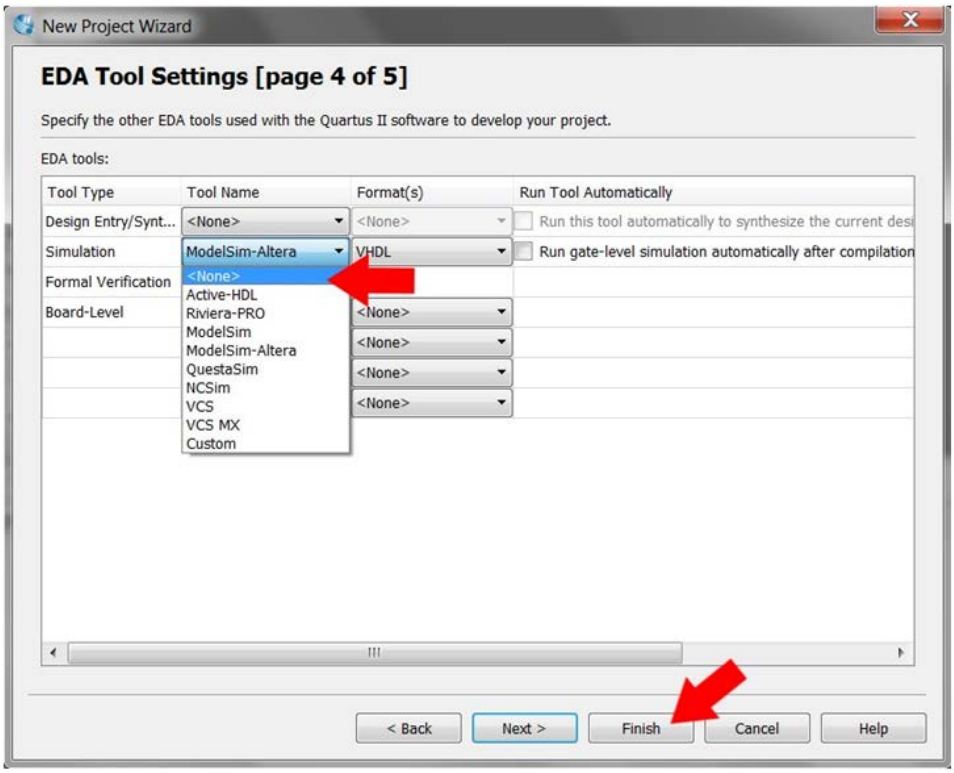

We are ready to start implementing our digital circuit. At this point we can either create new files from scratch, in this case equal.vhd for the one-bit comparator, or we can include the file from ModelSim in this Quartus project. Sometimes you may have a file already created somewhere else and just want to add it to Quartus for simulation on DE2 board; sometimes you may have to create one from scratch. For the sake of completeness of this tutorial, we will show you both ways:

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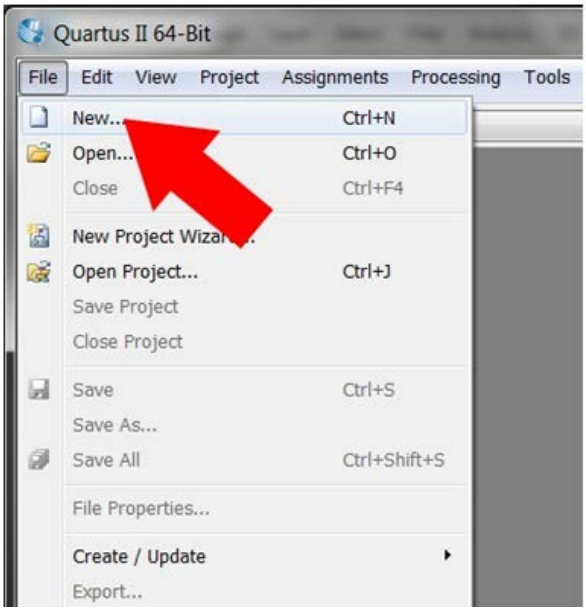
4.2 Creating a new VHDL file

To create a new VHDL file, click **File > New…**



The following window appears. Select **VHDL File** option to proceed with the design.

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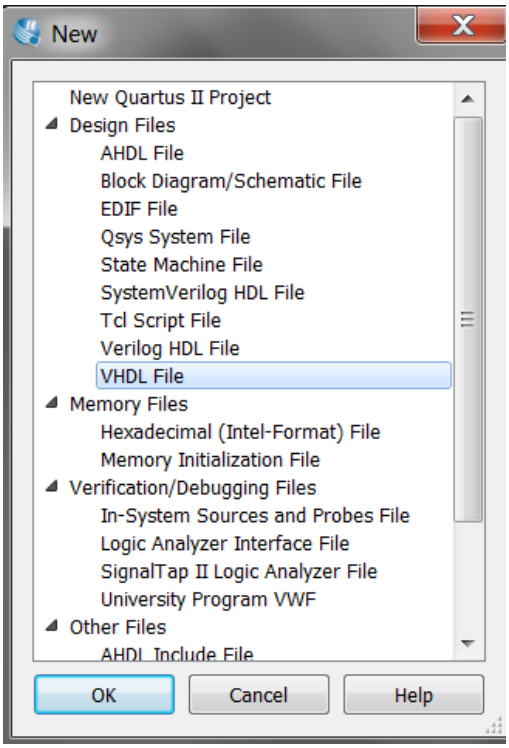

A blank VHDL code window appears. Copy the code given for the one bit comparator into this window. Then save this file by going to **File > Save As…**

Note that in the code of the 1-bit comparator, on line 4, the entity is named "equal". We can give entities any name we want but whatever name we assign, the VHDL file in Quartus must have the same name, otherwise you will experience compiling errors.

So go ahead and save this file as **equal.vhd**

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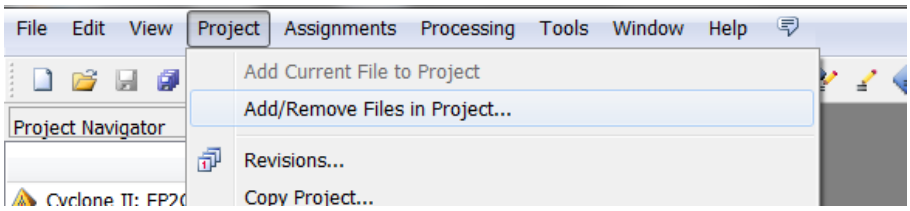
4.3 Adding an existing VHDL file to project

1. Click on **Project > Add/Remove Files in Project**



2. Click the Browse button noted by the arrow in the figure below, then browse for the file you want to add. After this, click **Add**, then hit **OK**.

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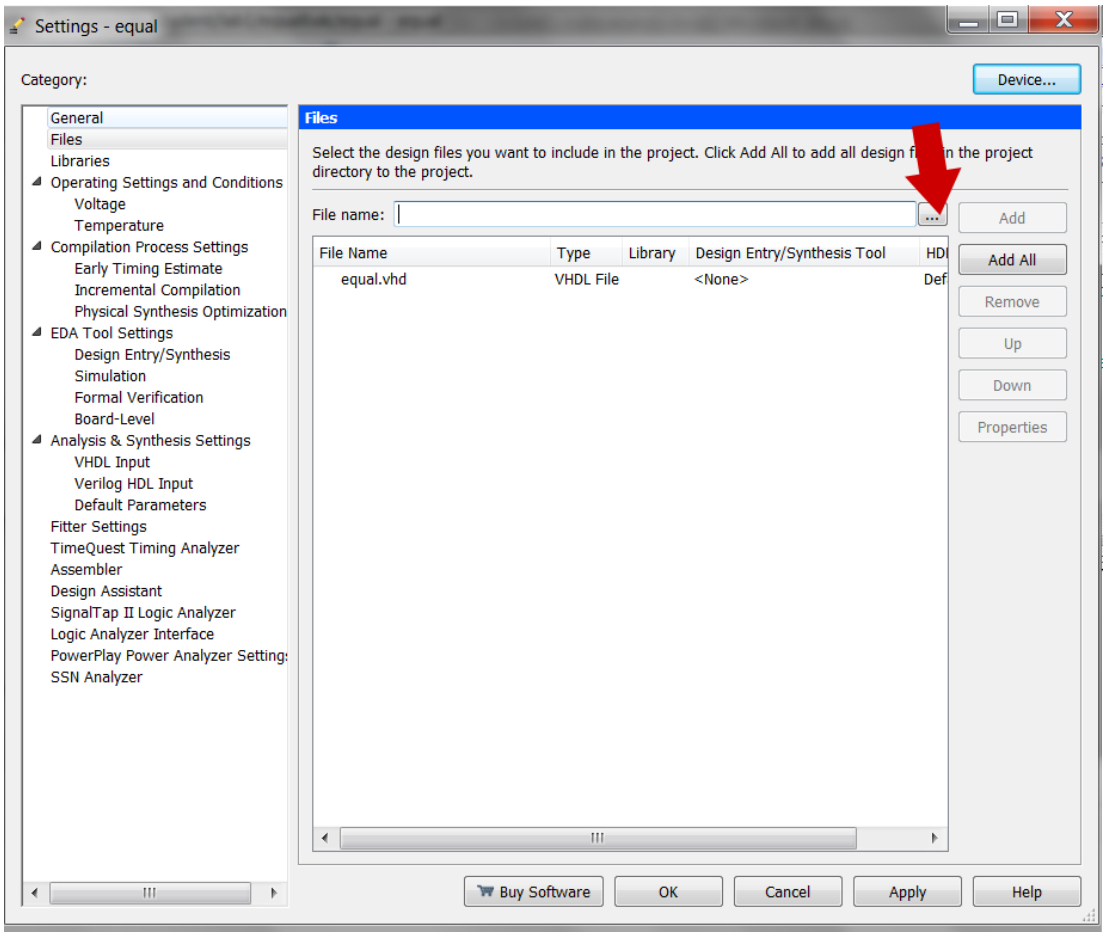

4.4 Compiling your VHDL design

Click the Files tab as shown in the picture below. This will show the project navigation panel. Here **right-click** the name of the file equal.vhd and select **Set as Top-Level Entity**.

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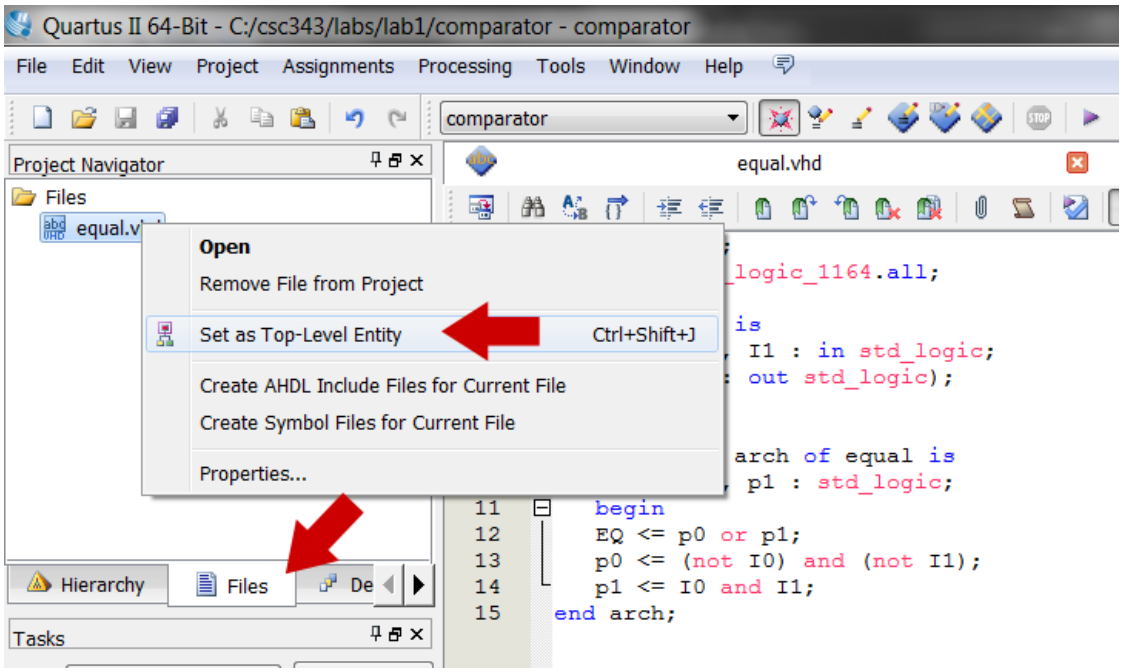

To verify that your code has no errors you should compile the project, click on **Processing > Start Compilation**. You can also compile by hitting the **Start Compilation** button in the menu bar. This would carry out a series of steps from Analysis and Synthesis, Fitter (Place & Route), Assembler and Timing Analysis.

The bottom panel shows the compilation messages. If there are any messages in **red**, they need to be fixed. **If you have a compilation error, it is most likely of an error in your design diagram due to a typo,**

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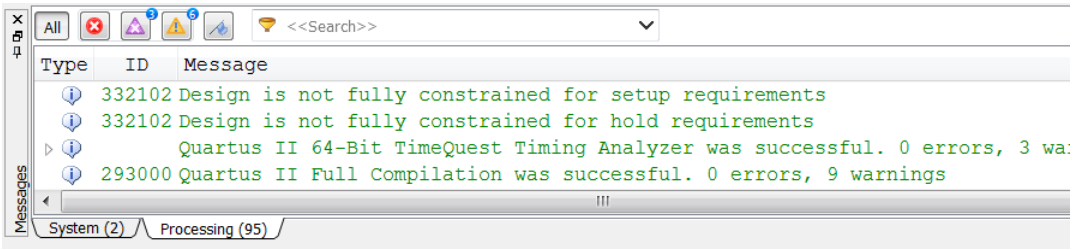
missing colon, semicolon, etc. The time it takes to compile your design depends on the speed and configuration of your computer.



We should now be ready to load the circuit design onto the DE2 board.

You should note the summary of compilation window:, and NOTE the device name used!! Is on the board you are using.

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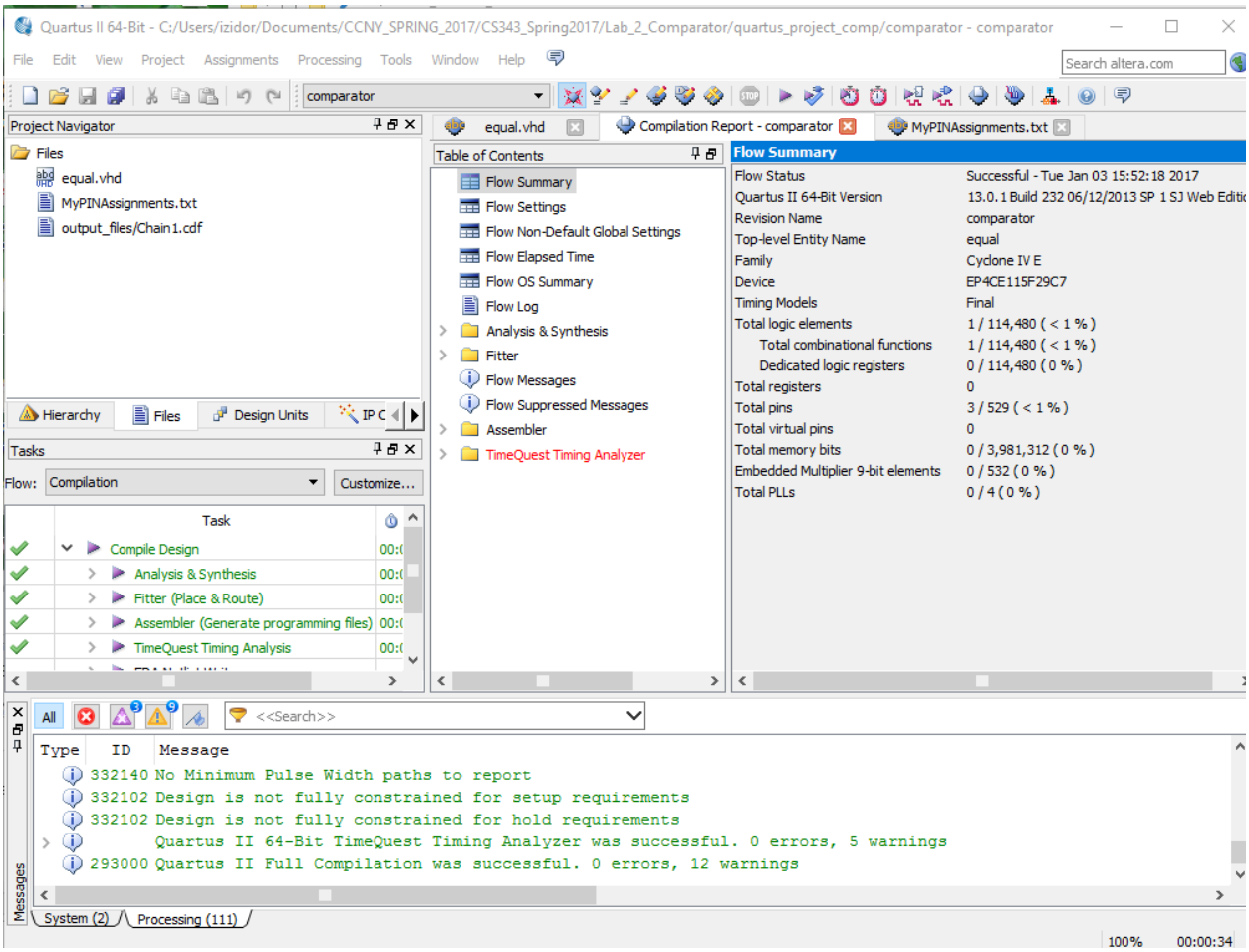

Generally, you should write a text file with the names of your inputs and the **names of the pins in the board you want them to be mapped to.**
We will explain how this is done but first, you should get familiar with the most common elements found in the DE2 board and how you can use them.

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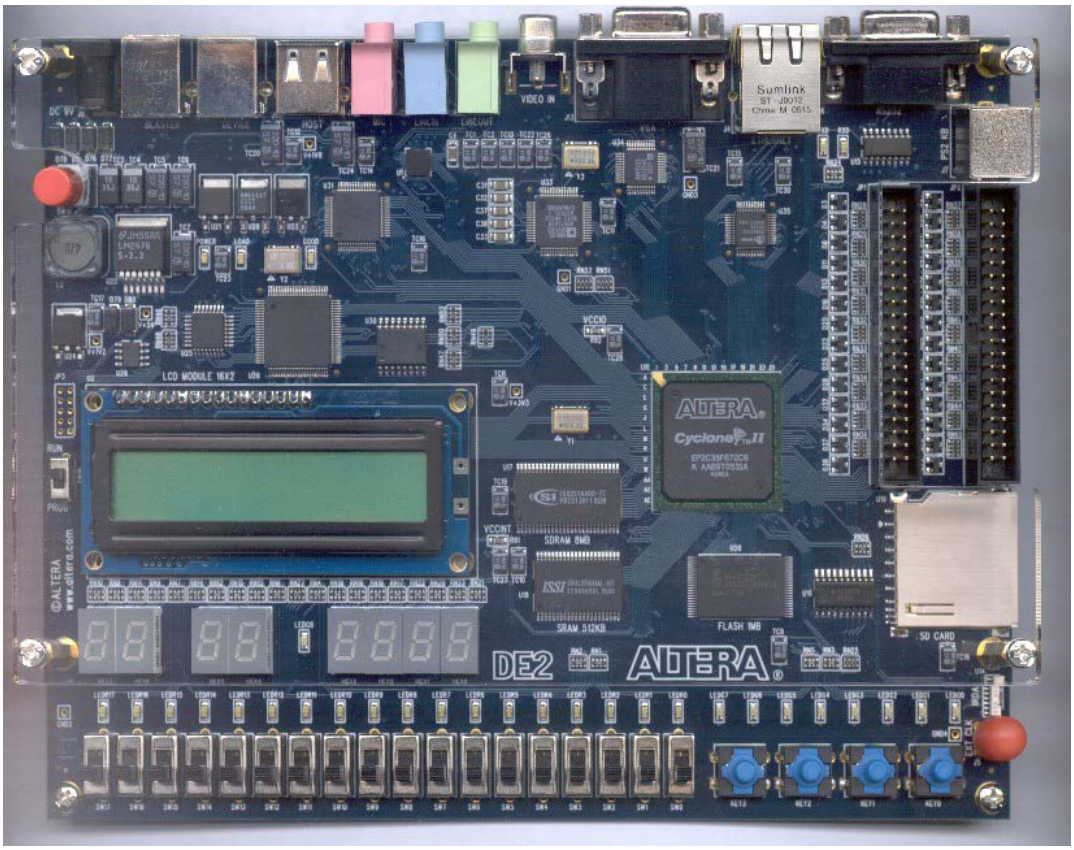

OUTPUTS

Seven Segment Display:

The DE2 Board includes several seven-segment displays that you can use to display your outputs.

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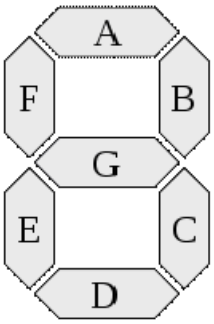
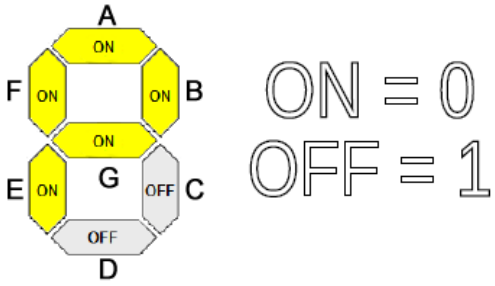
As you can see from the figure below, each segment is labeled with a letter. The segments are labeled in the order that the board needs to be set in. Setting it to a low 0 can turn on a segment of the display and vice versa.



For example, if we would like to display the letter P, this should be the setup:



The binary code to get the display to show a P is ABCDEFG = “0011000”

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LED:
The DE2 Board also includes LEDs in red and green.

The figure above shows most of the LEDs on the DE2 Board. You can use the LEDs to display the value of a single output bit. An output of 1 will turn the LED on, while an output of 0 will leave the LED off.

INPUTS

Switches:
The DE2 Board includes 18 switches that you can use to give your circuit input values.

The figure above shows all 18 of the switches available on the DE2 board. By setting a switch in the low position, as pictured, the switch will send an input value of a low 0. Flipping the switch up will send an input value of a high 1.

Pushbuttons:

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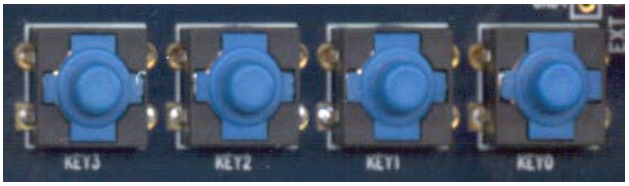
The DE2 Board also includes 3 pushbuttons that you can use to give your circuit input values. While the button is not being pressed, the input value will be a high 1. Pushing the button down will send a low 0 value for as long as it's being pressed.



Clock:

The DE2 Board has 2 built in clocks: A 50-megahertz clock, and a 27-megahertz clock. You can use these clocks to send an automatic pulse of values to your circuit.
The pin assignments to the clock are:

CLOCK_27: PIN_D13
CLOCK_50: PIN_N2

PIN ASSIGNMENTS

You can view the pin assignments for the DE2 Board from this link.
You can put your pin assignments in a text file and **save the file with any name you want.**

```
To, Location
my_pin_name, PIN_N1
my_vector_name[0], PIN_P1
my_vector_name[1], PIN_P2
my_vector_name[2], PIN_P3
my_bus_name[0], PIN_Q1
my_bus_name[1], PIN_Q2
another_vector[0], PIN_R1
another_vector[1], PIN_R2
```

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The figure above shows how you would write your pin assignments file. You start the file with "To, Location." On each line, you put the name of the pin you want to assign to the left, and the pin code of the DE2 Board to the right, separated by a comma.

If the pin you want to assign is a bus or vector, you can assign each bit of the bus by writing the name of the bus with the bit you want to assign in square brackets.

Usually, when you assign an input pin, it will be assigned to the switch or pushbutton. An output pin would usually be assigned to an LED or the seven-segment displays.

The pin assignment text file for our 1-bit comparator circuit will look like this for de-70 board with CYCLONE II chip:

```
To, Location
I0, PIN_N25
I1, PIN_N26
Eq, PIN_AE23
```

Here, inputs i0 and i1 are mapped to PIN_N25 and PIN_N26, which refer to the rightmost switches in the DE2 board. The output Eq is mapped to the rightmost RED LED light (PIN_AE23).
The pin assignment text file for our 1-bit comparator circuit will look like this for DE2-115 board with CYCLONE IV chip:

```
To, Location
I0, PIN_AB28
I1, PIN_AC28
EQ, PIN_G19
```

To use the pin assignments text file that you wrote, you need to import it to your project.
In Quartus go to: **Assignments > Import Assignments…**

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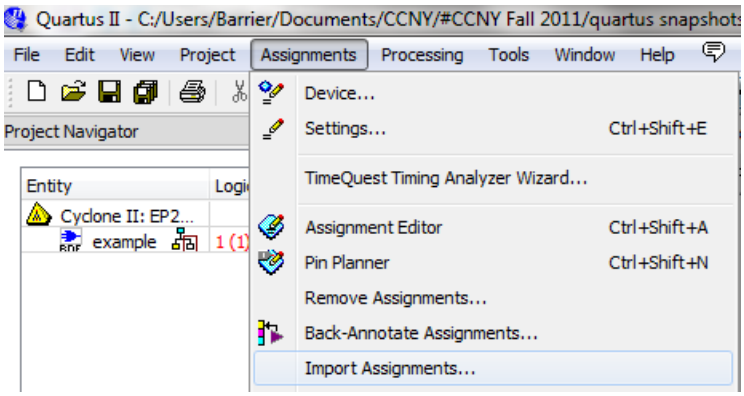
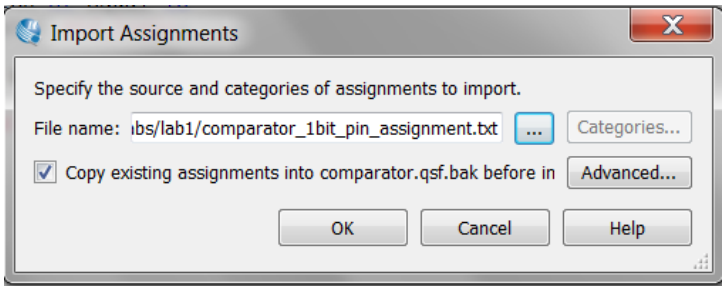


After opening the dialogue for importing assignments, browse for the file location of your pin assignments text file and press **OK**.



After you design, simulate and test your VHDL file you are ready now to PROGRAM the FPGA device CYCLON II on the DE board. Compile your project after you do the pin assignments.

You can now load your circuit onto the DE Board

==========

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IMPORTANT:

If it is your first time connecting the board to your computer, you might

need to install the drivers for the Board. To do this follow the next steps

1. Plug the USB-Blaster II cable into your PC. (connected to the board)
2. Open the **Device Manager**, and right-click on the **Unknown device** under the **Other devices** branch.
3. Select **Update Driver Software**.
4. Select **Browse my computer for driver software**.
5. Enter the location of the Quartus Prime software USB-Blaster II driver files directory (<***Path to Quartus Prime installation>\drivers\usb-blaster-ii***) in the **Search for driver software in this location** field. (For example my directory was: C:\altera_lite\16.0\quartus\drivers\usb-blaster-ii)
6. Click **Next**.
7. Click **Install** in the **Would you like to install this device software?** Windows security dialog box.
8. Close the **Update Driver Software - Altera USB-Blaster II (Unconfigured)** successful installation notification. The Device Manager now shows a new branch called **JTAG cables** with an **Altera USB-Blaster II (Unconfigured)** node.

==========

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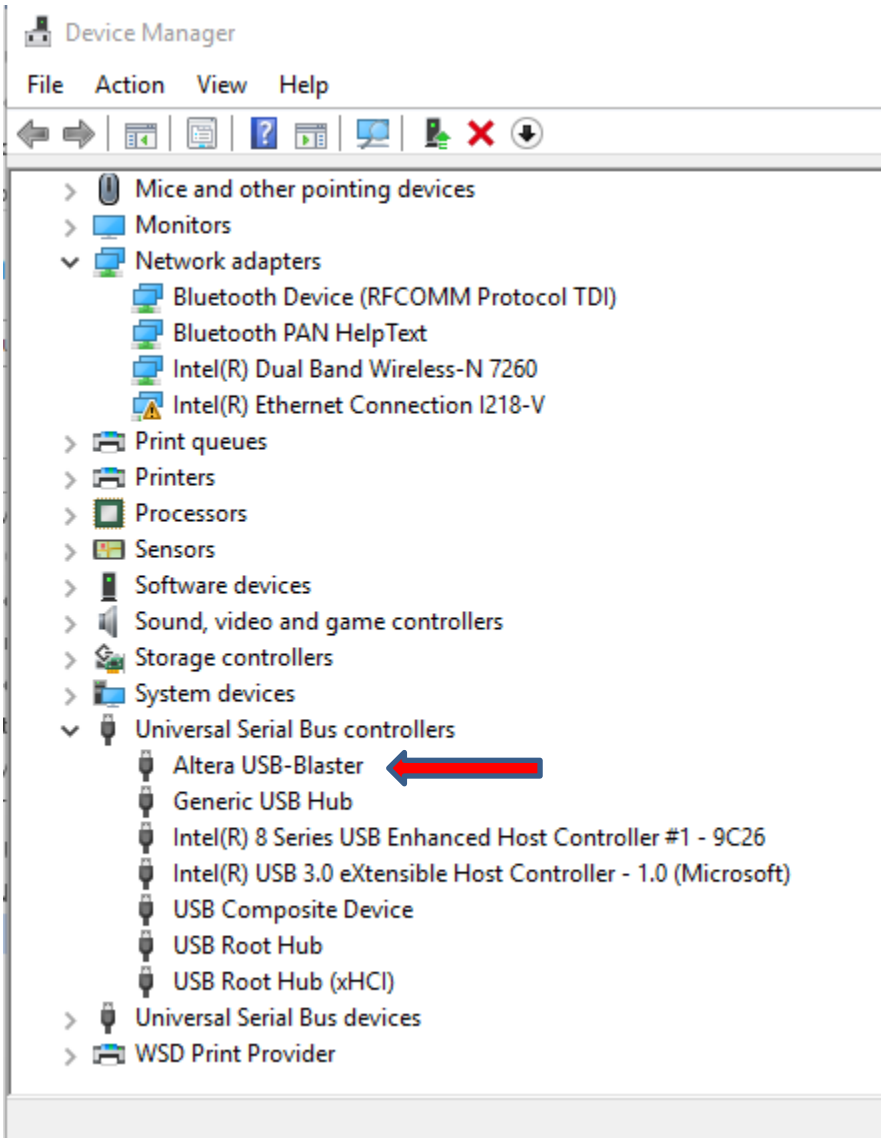

You can now load your circuit onto the DE2 Board by going to: **Tools > Programmer.** Press start to load the design, see figure below:

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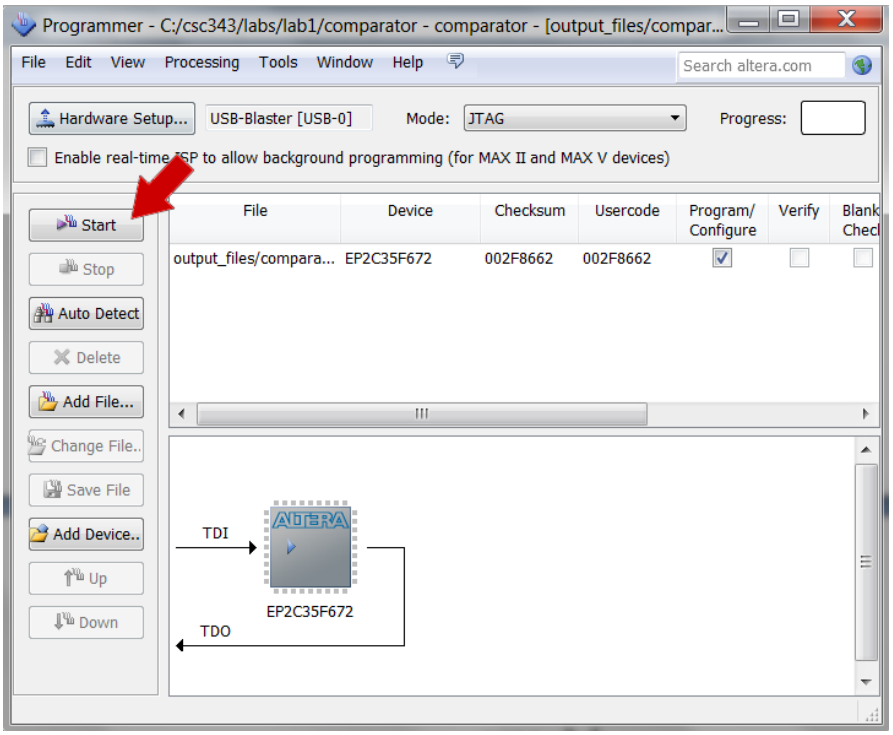

Click **AUTO_DETECT** and select your device and press OK.

You get the following window

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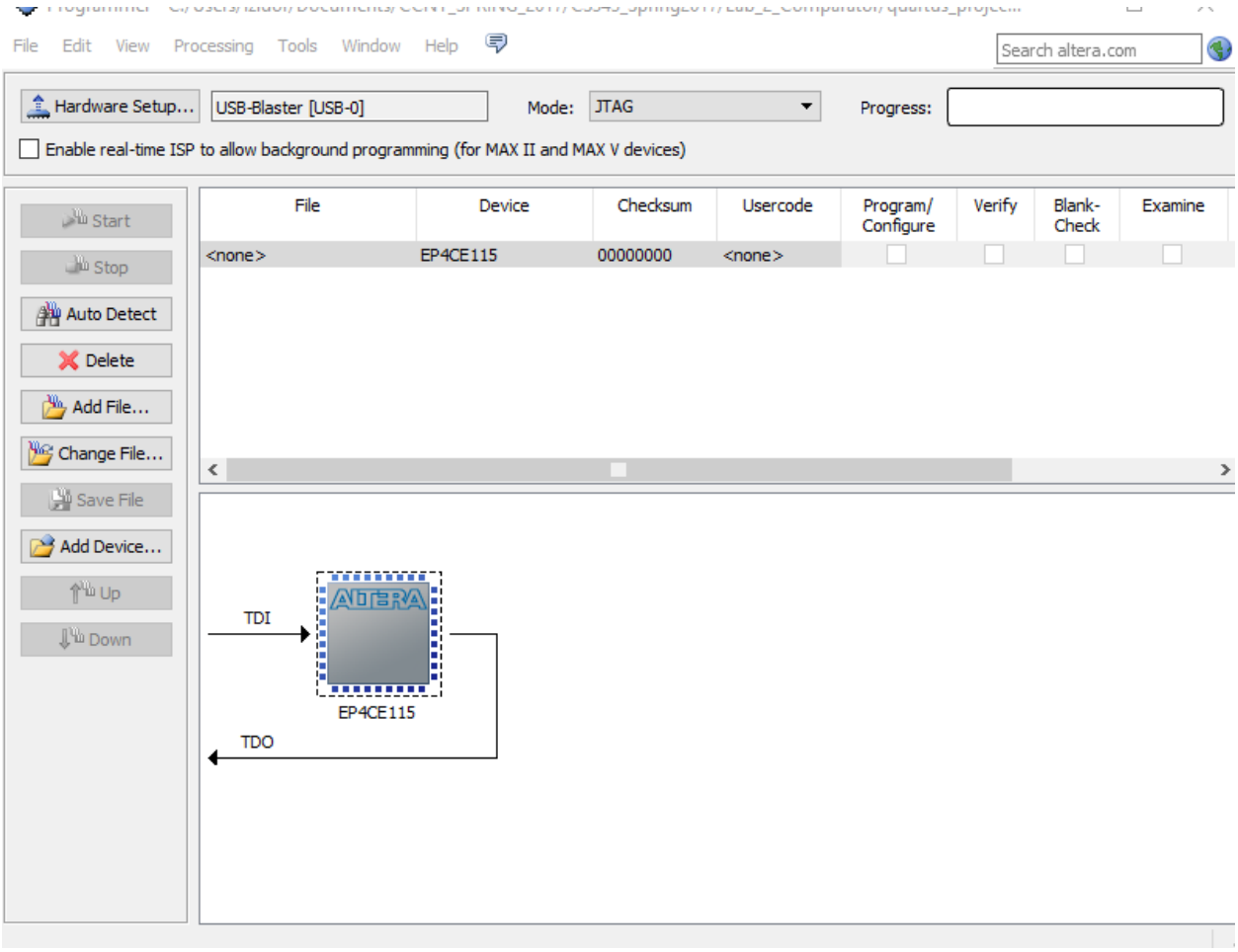

Now right click on the line, the one with the Device name EP4Ce115 (note the device name on the FPGA chip on the board!) and click on **Change File**

You will get the following window. Notice the directory, it is the directory for our project. Now go to the **output_files** folder

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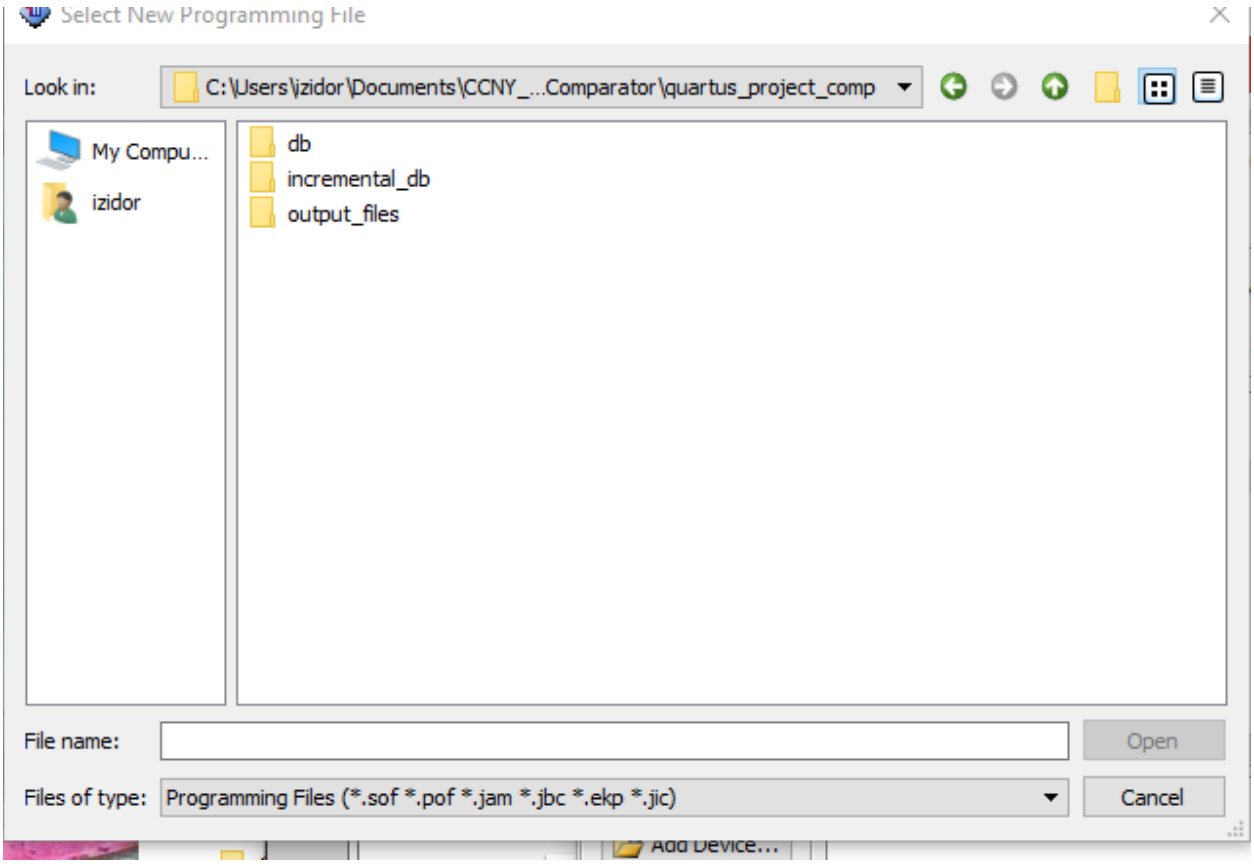

In the **output_files** directory select **comparator.sof** file.

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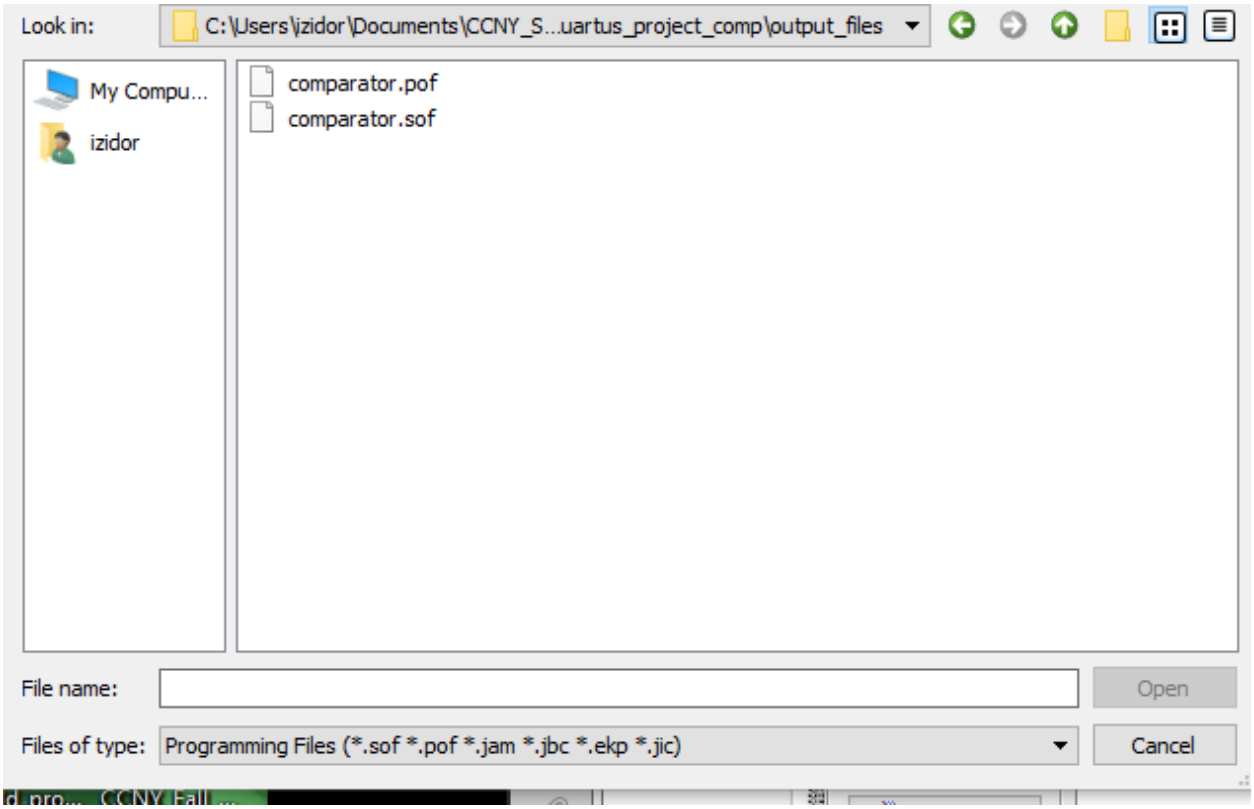

Click OPEN

You should get the window:

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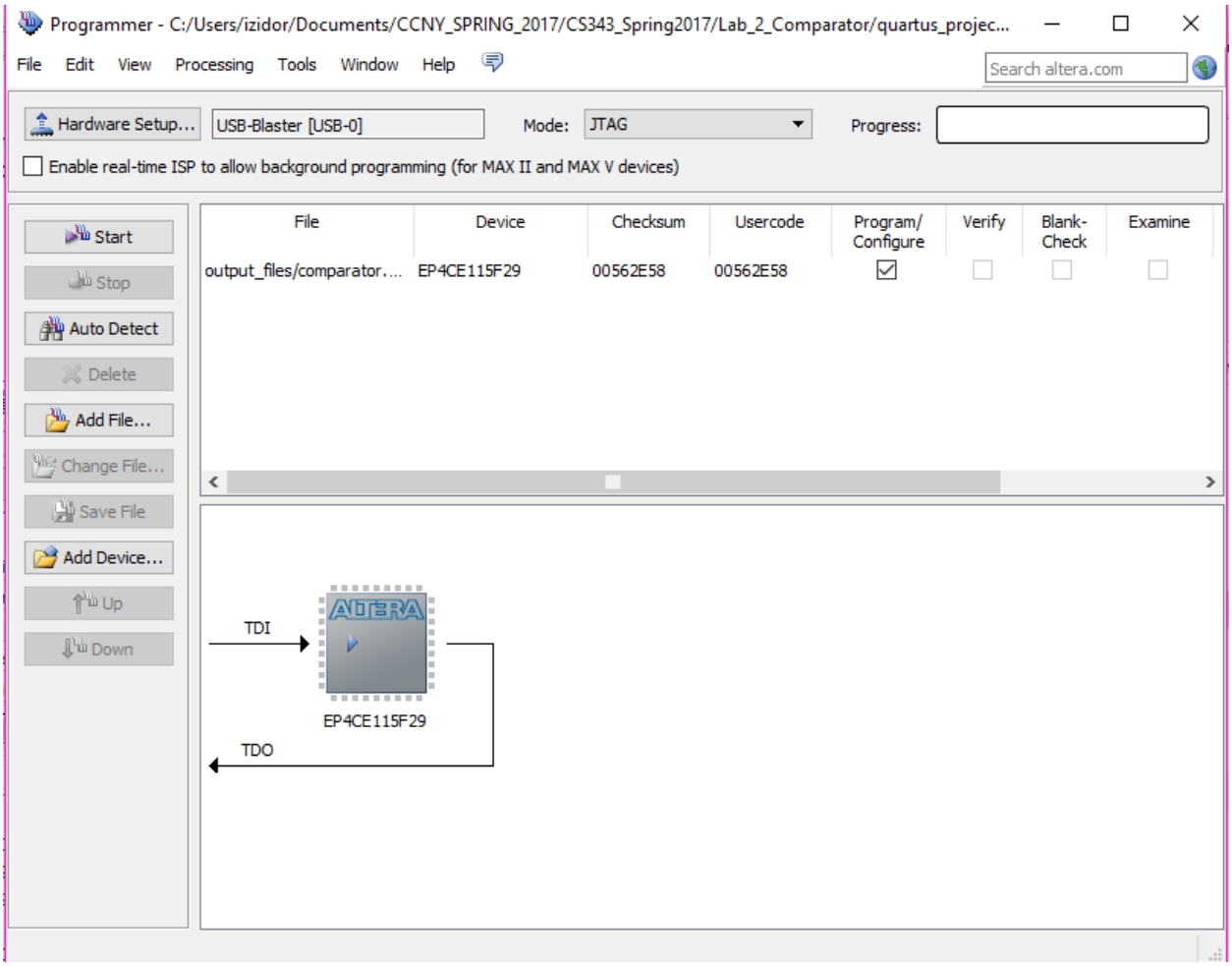

CHECK program/configure as shown in the image above..

Cick the START b button..

If the **Start** button for some reason appears disabled, you may be experiencing a problem with the driver in the computer or your project may need to be compiled. If it still doesn't work, try restarting Quartus.

An example of the behavior of the circuit in the board is shown below:

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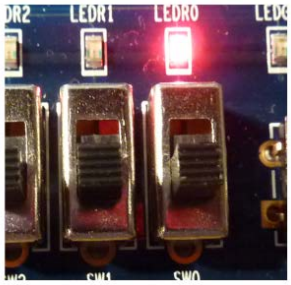
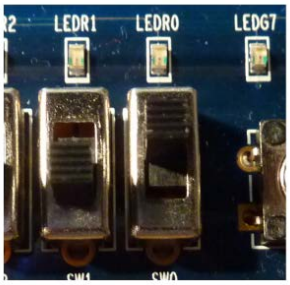
i0=0
i1=0
Eq=1





i0=1
i1=0
Eq=0

i0=0
i1=1
Eq=0

i0=1
i1=1
Eq=1

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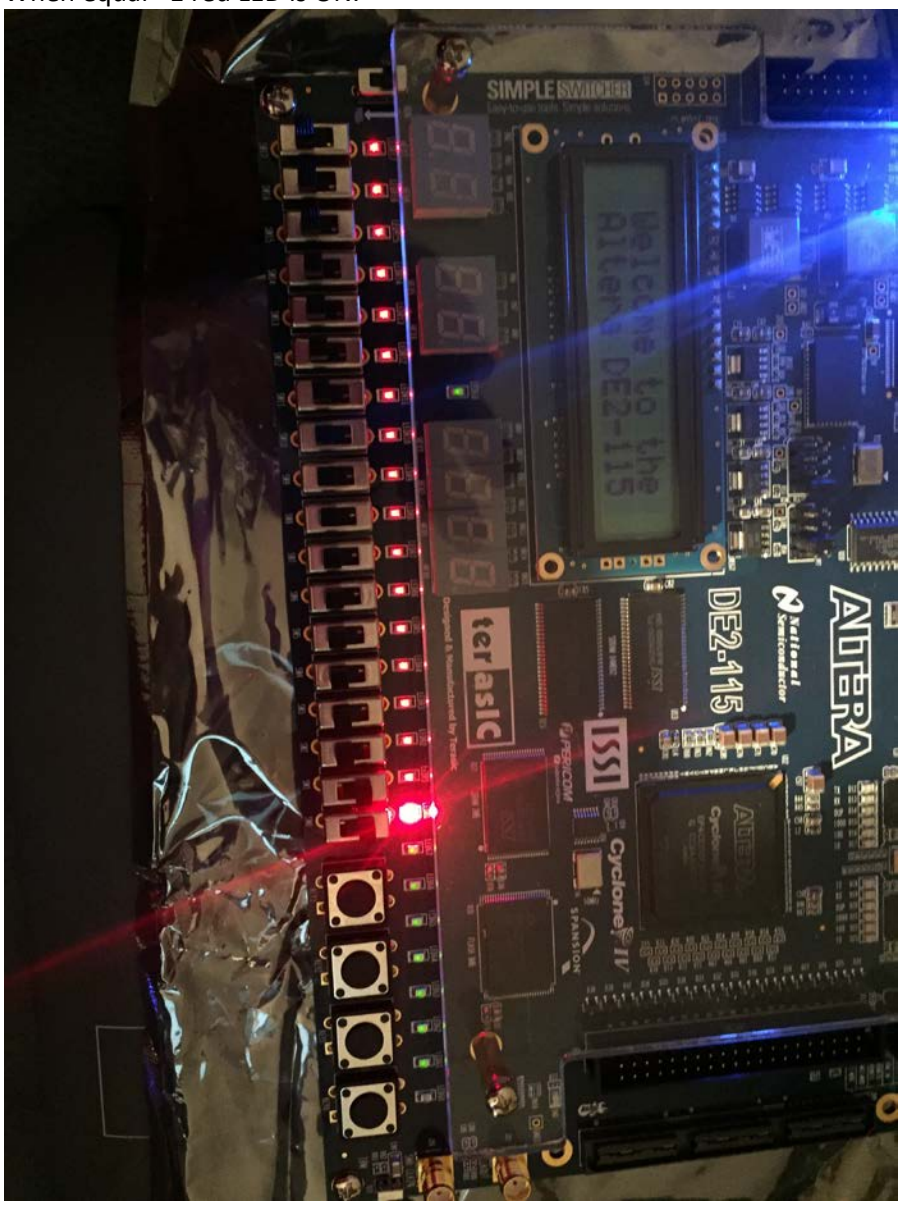
When equal =1 red LED is ON.



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When not equal the green LED is ON.

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2-BIT COMPARATOR

Now that we have written our first piece of VHDL code we want to make it a bit more complicated. Now we want to make a two-bit comparator. The program will take two 2-bit inputs and compare them and check if their equal or not. This can be done in two ways:

- Logic (logic-vector) inputs/outputs
- Port Maps

You will implement the two-bit comparator in both ways and at the end you will understand their differences.

Note: For the 2-bit and 8bit comparator you will perform the exact same procedure we showed for the 1-bit comparator. You will write your VHDL code, run the waveform simulation and test in ModelSim, mount your design in Quartus, etc.

Using Logic Vectors:

If you draw out the truth table for the two-bit comparator you will be able to derive the logical statement given below:

aeqb = (a1'.b1').(a0'.b0') + (a1'.b1').(a0.b0) + (a1.b1).(a0'b0') + (a1.b1).(a0.b0)

Fill out the missing parts in the code below using the logical expression above - notice that aeqb can be expressed as aeqb = p0 + p1 +p2 +p3

two_bit_equal.vhd

```
1 library ieee;
2 use ieee.std_logic_1164.all;
```

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```
 3
 4 entity two_bit_equal is
 5         port ( a, b     : in std_logic_vector(1 downto 0);
 6                aeqb     : out std_logic);
 7 end two_bit_equal;
 8
 9 architecture arch of two_bit_equal is
10 signal p0, p1, p2, p3 : std_logic;
11 begin
12 aeqb <= p0 or p1 or p2 or p3;
13 p0 <= --Enter you code here;
14 p1 <= --Enter you code here;
15 p2 <= --Enter you code here;
16 p3 <= --Enter you code here;
17 end arch;
```

The only difference in this code is that inputs a and b are declared as “STD_LOGIC_VECTOR(1 downto 0)” which means it is a vector of size two.

Now to test our design we need a test file. Again the test file will be given to you but try to understand how it works.

test_two_bit_equal.vhd

```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity test_two_bit_equal is
 5 end test_two_bit_equal;
 6
 7 architecture arch_test of test_two_bit_equal is
 8 component two_bit_equal
 9 port ( a, b     : in std_logic_vector(1 downto 0);
10        aeqb     : out std_logic);
11 end component;
12
13 signal p1, p0   : std_logic_vector(1 downto 0);
14 signal pout     : std_logic;
15 signal error    : std_logic := '0';
```

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```
16 begin
17 uut: two_bit_equal port map(a => p0, b=> p1, aeqb => pout);
18 process
19 begin
20 p0 <= "00";
21 p1 <= "00";
22 wait for 1 ns;
23 if (pout = '0') then
24         error <= '1';
25 end if;
26 wait for 200 ns;
27 p0 <= "01";
28 p1 <= "00";
29 wait for 1 ns;
30 if (pout = '1') then
31         error <= '1';
32 end if;
33 wait for 200 ns;
34 p0 <= "01";
35 p1 <= "11";
36 wait for 1 ns;
37 if (pout = '1') then
38         error <= '1';
39 end if;
40 wait for 200 ns;
41 p0 <= "11";
42 p1 <= "00";
43 wait for 1 ns;
44 if (pout = '1') then
45         error <= '1';
46 end if;
47 wait for 200 ns;
48 p0 <= "11";
49 p1 <= "11";
50 wait for 1 ns;
51 if (pout = '0') then
52         error <= '1';
53 end if;
54 wait for 200 ns;
55 p0 <= "10";
56 p1 <= "11";
57 wait for 1 ns;
58 if (pout = '1') then
```

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```
59          error <= '1';
60  end if;
61  wait for 200 ns;
62  p0 <= "10";
63  p1 <= "10";
64  wait for 1 ns;
65  if (pout = '0') then
66          error <= '1';
67  end if;
68  wait for 200 ns;
69  p0 <= "11";
70  p1 <= "01";
71  wait for 1 ns;
72  if (pout = '1') then
73          error <= '1';
74  end if;
75  wait for 200 ns;
76
77  if (error = '0') then
78          report "No errors detected. Simulation successful" severity
79  failure;
80          else
81                  report "Error detected" severity failure;
82  end if;
83  end process;
84  end arch_test;
```

Using Port Maps:

As you can see writing the two-bit comparator using logical expressions could get a bit tiresome and confusing especially as we increase the number of bits. There is an easier way to do this using “PORT MAPS”. What port map does is that it uses other components that we or others have created and connects them together to make something bigger. For example to make a two-bit comparator we will connect 2 one-bit comparators making life much easier and simpler.
Below is the code for the two-bit comparator with the use of port maps:

two_bit_equal_port.vhd

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```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity two_bit_equal_port is
 5 port (
 6         a, b: in std_logic_vector(1 downto 0);
 7         aeqb : out std_logic);
 8 end two_bit_equal_port;
 9
10 architecture arch of two_bit_equal_port is
11
12         --component declaration...we are telling the compiler
13         --which components we want to use from the library.
14         component equal
15         port (
16                 I0, I1: in std_logic;
17                 Eq : out std_logic);
18         end component;
19         signal e0,e1: std_logic;
20
21         begin
22
23         --instantiates two one-bit comparators
24         H1: equal port map(i0=>a(0), i1=>b(0), eq=>e0);
25         H2: equal port map(i0=>a(1), i1=>b(1), eq=>e1);
26
27         --a and b are equal if individual bits are equal.
28         aeqb <= e0 and e1;
29
30 end arch;
```

Observe the syntax of using port maps because it is very important as we continue with more advanced projects. Port maps act as wires connecting different components or black boxes together. H1 and H2 used in the code are just names for the components; you can name them anything you want.
To test this design use the same **test_two_bit_equal** test file given above but change the name of the component to **two_bit_equal_port** since you are simulating this file instead. Simulate your code and analyze your results.

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8-BIT COMPARATOR

Using the two-bit comparator example, write the VHDL code for an eight-bit comparator. Your code should look very similar to the code from the **two_bit_equal_port** file, with the only difference that instead of using two instances of the "equal" component, you will use eight instances of the one-bit comparator. Use the following test code to verify your results.

test_eight_bit_equal_port_map.vhd

```
 1 library ieee;
 2 use ieee.std_logic_1164.all;
 3
 4 entity test_eight_bit_equal_port_map is
 5 end test_eight_bit_equal_port_map;
 6
 7 architecture arch_test of test_eight_bit_equal_port_map is
 8
 9 component eight_bit_equal_port_map
10   port ( a, b : in std_logic_vector(7 downto 0);
11          aeqb  : out std_logic);
12 end component;
13
14 signal p1, p0 : std_logic_vector(7 downto 0);
15 signal pout   : std_logic;
16 signal error  : std_logic := '0';
17 begin
18   uut: eight_bit_equal_port_map port map(a => p0, b => p1, aeqb => pout);
19   process
20     begin
21       p0 <= "00000000";
22       p1 <= "00000000";
23       wait for 1 ns;
24       if (pout = '0') then
25         error <= '1';
```

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```
26      end if;
27      wait for 200 ns;
28      p0 <= "01010101";
29      p1 <= "00010101";
30      wait for 1 ns;
31      if (pout = '1') then
32        error <= '1';
33      end if;
34      wait for 200 ns;
35      p0 <= "01100101";
36      p1 <= "11111001";
37      wait for 1 ns;
38      if (pout = '1') then
39        error <= '1';
40      end if;
41      wait for 200 ns;
42      p0 <= "11110011";
43      p1 <= "00010100";
44      wait for 1 ns;
45      if (pout = '1') then
46        error <= '1';
47      end if;
48      wait for 200 ns;
49      p0 <= "11001100";
50      p1 <= "11001100";
51      wait for 1 ns;
52      if (pout = '0') then
53        error <= '1';
54      end if;
55      wait for 200 ns;
56      p0 <= "10010001";
57      p1 <= "11100111";
58      wait for 1 ns;
59      if (pout = '1') then
60        error <= '1';
61      end if;
62      wait for 200 ns;
63      p0 <= "10111001";
64      p1 <= "10111001";
65      wait for 1 ns;
66      if (pout = '0') then
67        error <= '1';
68      end if;
```

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```
69       wait for 200 ns;
70       p0 <= "11010011";
71       p1 <= "01101001";
72       wait for 1 ns;
73       if (pout = '1') then
74         error <= '1';
75       end if;
76       wait for 200 ns;
77
78       if (error = '0') then
79         report "No errors detected. Simulation successful" severity
80         failure;
81       else
82         report "Error detected" severity failure;
83       end if;
84
85   end process;
86 end arch_test;
```

YOUR TASK

For this lab you should complete the following:

1. **One-bit comparator**
   - Add a notEq output signal:
     We gave you all the code for the one-bit comparator and its test file. We walked you through testing and simulation. Now we need you to add an extra output called **notEq** to the given equal file. Add the notEq output to the entity section and add the notEq behavior in the architecture section (remember it should output the opposite of Eq). Eq is assigned to LEDR[0]. Assign notEq to LEDR[1]. Only one of these has its light up at a time!

     You can view the pin assignments for the DE2 Board from this link.

   - Make sure you have the following files completed:

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- equal.vhd
- test_equal.vhd

- Run test in ModelSim using test file.
- Create waveform in ModelSim from equal.vhd without a test file. This is so you understand the difference versus having a test file.
- Implement circuit design in Quartus and observe behavior on DE2 board. Use switches SW[0] and SW[1] for your inputs. Eq is assigned to LEDR[0]. Assign notEq to LEDR[1].

2. Two-bit comparator

- Make sure you have the following files:
  - two_bit_equal.vhd
  - test_two_bit_equal.vhd
  - two_bit_equal_port.vhd
  - test_two_bit_equal_port.vhd
- Using the test file given, run waveform test for both cases (logic vector and port maps). Remember to change the name in the **component** part for the corresponding case in the test file.
- Implement both logic-vector and port-map-based circuit designs in Quartus and observe behavior on DE2 board. Use switches SW[0] and SW[1] for the bits of the first input (vector a), use SW[8] and SW[9] for the bits of the second input (vector b). Eq is assigned to LEDR[0]. Assign notEq to LEDR[1].

3. Eight-bit comparator

- Make sure you have the following files:
  - eight_bit_equal_port_map.vhd
  - test_eight_bit_equal_port_map.vhd
- Run test in ModelSim using test file given.
- Implement circuit design in Quartus and observe behavior on DE2 board. Use switches SW[0] to SW[7] for the bits of the first input. Use switches SW[8] to SW[15] for the bits of the second input. Eq is assigned to LEDR[0]. Assign notEq to LEDR[1].

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4. Report

Please write a lab report that addresses the following bullet points. Do not limit yourself to these; feel free to address more ideas/experiences with this lab in your summary.

Objective

- What is the goal of this assignment?

Design

- Include the VHDL code of each comparator.
- Describe the configuration of each comparator, inputs, outputs, etc, equation, etc.

Functionality

- Provide a walkthrough of the VHDL code you wrote for each comparator.
- Point out why you used logic input/outputs in one case, logic vectors and port maps in others, etc.

Simulation

- Include screenshots of your waveform results from ModelSim for each comparator.
- Analyze the waveforms obtained. Include an explanation of the waveform runs for each comparator.
- Explain the difference between using a test file and running a waveform simulation without one.

Analysis

- Were you able to use the same test file for the port map and logic vector versions of the two_bit_equal comparator? Did you have to make any changes to that file to make it work in each case? Explain.
- If you obtained any errors during simulation / compilation please explain what happened and how you solved the issue.

Laboratory Project 2
Introduction to VHDL,
ModelSim and Quartus CAD software tools
using as an example digital Comparator circuits
(Detailed version)

Instructor: Professor Izidor Gertner

February , 2017

- Can you give examples of what comparators may be useful for?

Conclusion

- Have you designed circuits using block diagrams before? Which way of circuit design do you enjoy better: block diagrams or VHDL? Why? What are the advantages/disadvantages of one versus the other?
- Do you find the structure or pieces of VHDL code similar to any other programming languages you know? Do you find it intuitive?
- Give a brief conclusion on what you learned about this assignment. What makes ModelSim different from the waveform simulation tool included in Quartus? Can you think of reasons or research why it is important to know ModelSim simulation?