Lab 1: Adders

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# Objective

# Functionality and Specification

## Half Adder

The half adder is a circuit that takes in two bits and outputs the sum and carry bits. For a visual representation, see Fig. 1 below. The x and y each take on two possible values, for a total of four input combinations. The corresponding output is shown below the line. An equivalent way of representing

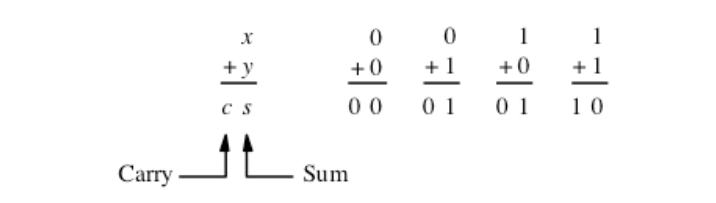


Fig. 1. Half Adder using Arithmetic

Fig. 1 is through the truth table, as shown on Table I. The carry bit is 1 when both x and y are 1, and 0 otherwise. The sum is 1 when x and y are not equal. From the truth table we can create a circuit diagram for the half adder with an AND and XOR gate for the carry and sum bits respectively.

Table I. Truth Table of Half Adder

|  |  |  |  |
| --- | --- | --- | --- |
| Input | | Output | |
| X | **Y** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Fig. 2 shows the circuit diagram for the half adder. The x and y are inputs to both the AND and XOR gate.

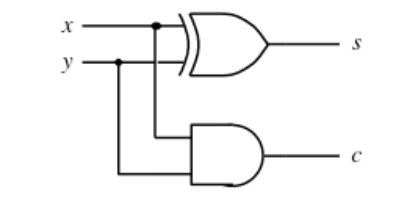


Fig. 2. Half Adder Circuit Diagram.

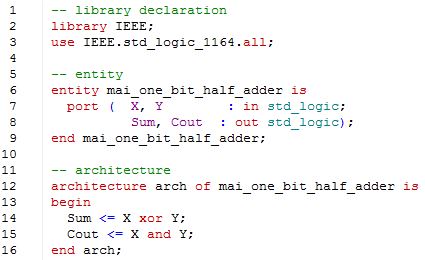


Fig. 3. VHDL Code for Half Adder.

## Full-Adder Using Gates

Table II. Truth Table for Full Adder

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | | | Output | |
| X | **Y** | **Cin** | **EQ** | **EQNOT** |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |

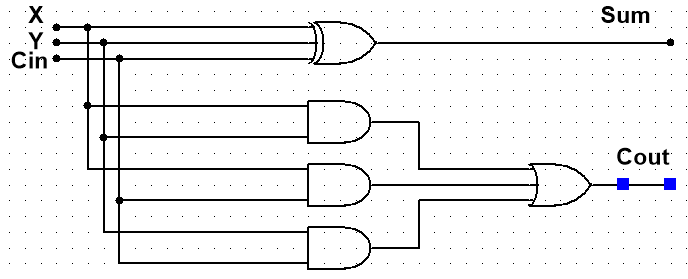


Fig. 4. Circuit Diagram for Full Adder with Gates

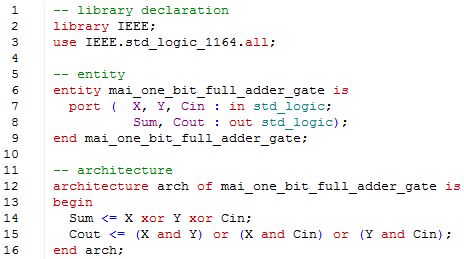


Fig. 5. VHDL Code for Full Adder with Gates.

## Full-Adder using Half Adders as Components

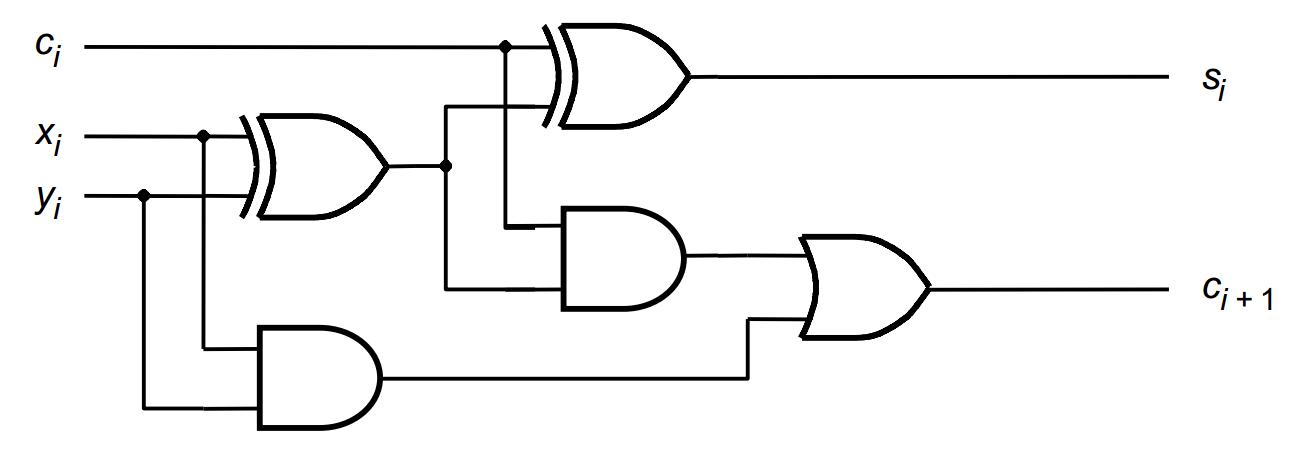


Fig. 6. Circuit Diagram of Full Adder with Half Adders as Components (gates).

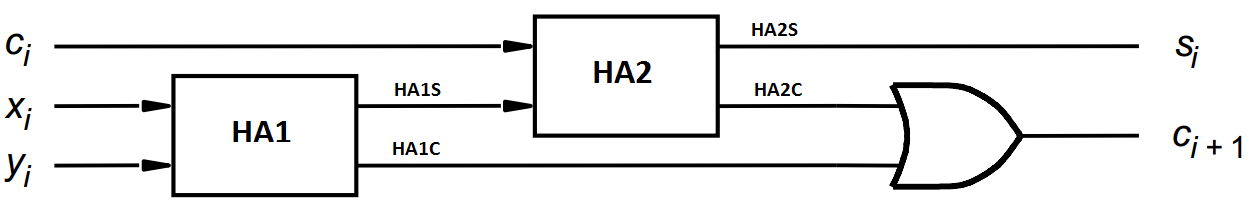


Fig. 7. Circuit Diagram of Full Adder with Half Adders as Components (Block Diagram).

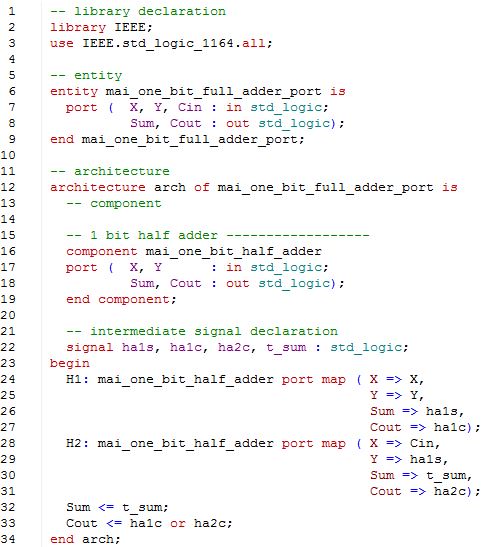


Fig. 8. VHDL Code for Full Adder using Half Adders as Components.

## Four-Bit Adder using One-Bit Full Adders as Components

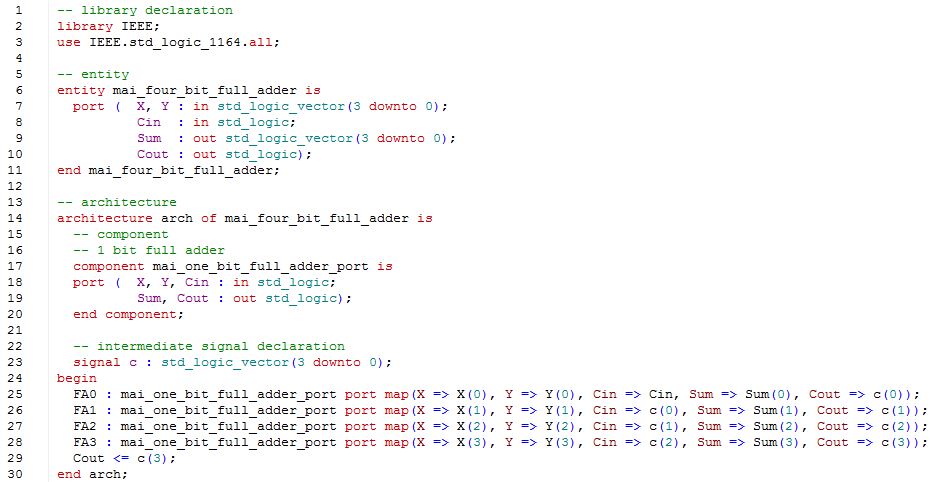


Fig. 9. VHL Code for Four-Bit Adder using One-Bit Full Adders as Components.

# Simulation

## Half Adder

## Full-Adder using Gates

## Full-Adder using Half-Adders as Components

## Four-Bit Adder using One-Bit Full Adders as Component

# Implementation

## Half Adder