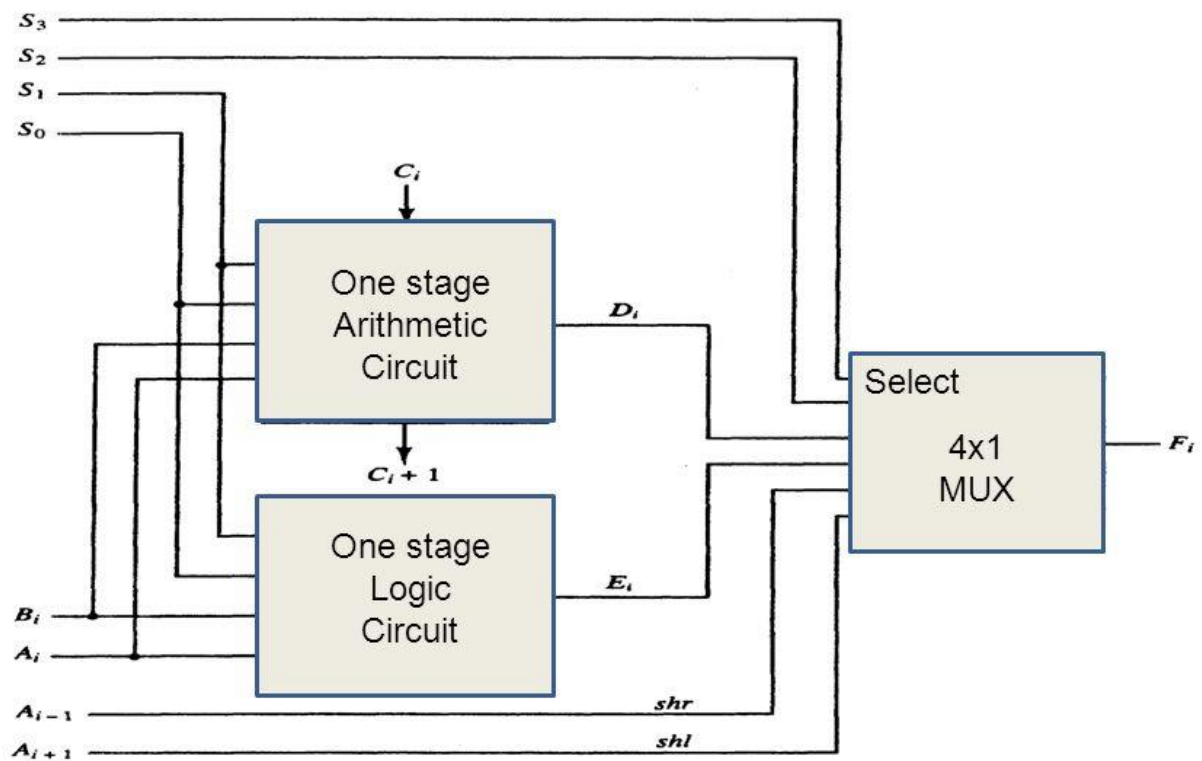


|: ARITHMETIC & LOGIC SHIFT UNIT :|

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic, logic and shift operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU).

- Block Diagram of ALS Unit

Arithmetic Logic Shift Unit

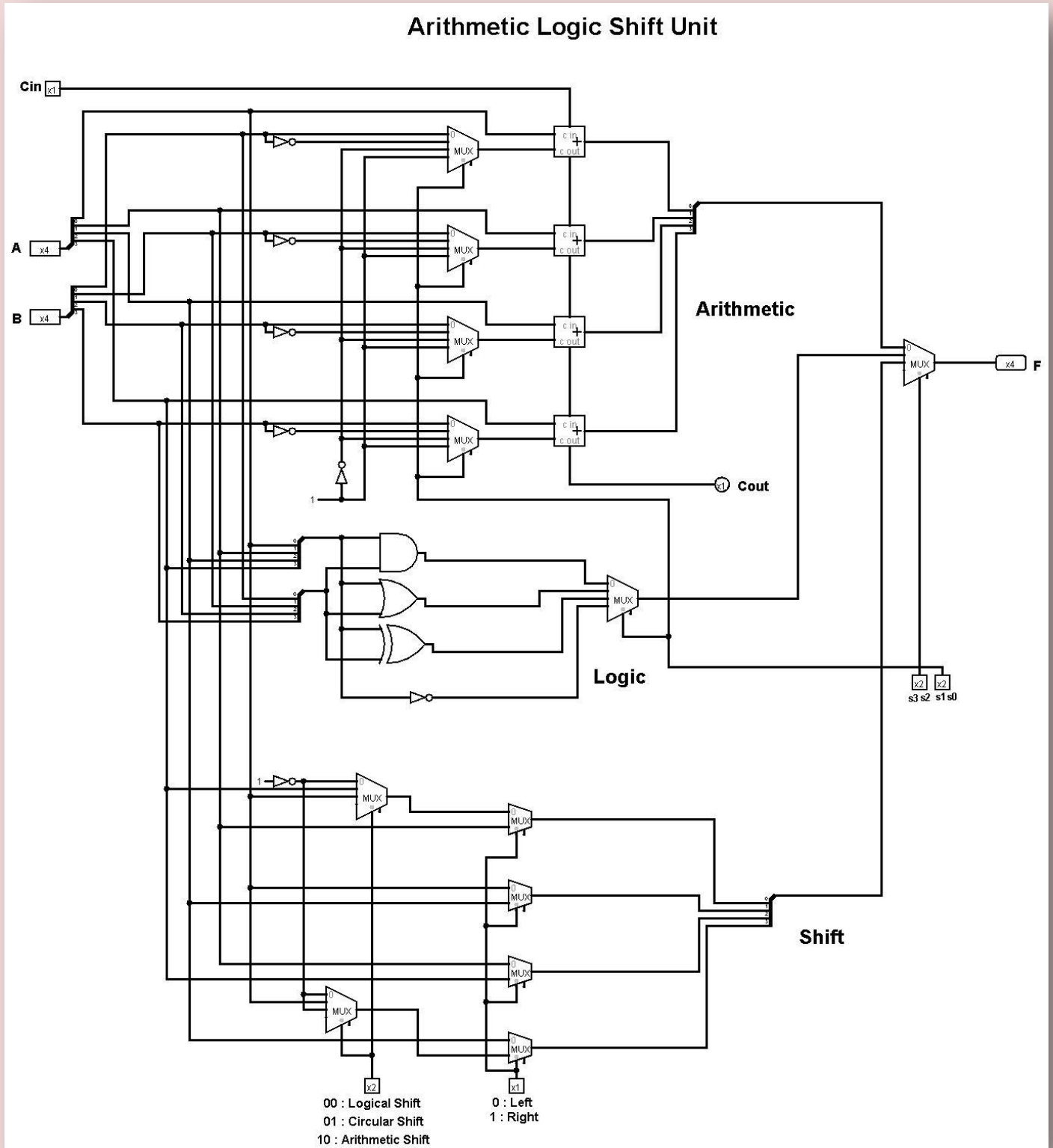


One stage of arithmetic logic shift unit

Reference Table that Shows the all the input/output of my circuit

| S3 | S2 | S1 | S0 | cin | X2 | X1 | OPERATION |
|----|----|----|----|-----|----|----|-----------|
| 0 | 0 | 0 | 0 | 0 | - | - | F=A+B |
| 0 | 0 | 0 | 0 | 1 | - | - | F=A+B+1 |
| 0 | 0 | 0 | 1 | 0 | - | - | F=A+B' |
| 0 | 0 | 0 | 1 | 1 | - | - | F=A+B'+1 |
| 0 | 0 | 1 | 0 | 0 | - | - | F=A |
| 0 | 0 | 1 | 0 | 1 | - | - | F=A+1 |
| 0 | 0 | 1 | 1 | 0 | - | - | F=A-1 |
| 0 | 0 | 1 | 1 | 1 | - | - | F=A |
| 0 | 1 | 0 | 0 | - | - | - | F=A&B |
| 0 | 1 | 0 | 1 | - | - | - | F=A B |
| 0 | 1 | 1 | 0 | - | - | - | F=A^B |
| 0 | 1 | 1 | 1 | - | - | - | F=A' |
| 1 | 0 | - | - | - | 00 | 0 | F=SHL A |
| 1 | 0 | - | - | - | 00 | 1 | F=SHR A |
| 1 | 0 | - | - | - | 01 | 0 | F=CIL A |
| 1 | 0 | - | - | - | 01 | 1 | F=CIR A |
| 1 | 0 | - | - | - | 10 | 0 | F=ASHL A |
| 1 | 0 | - | - | - | 10 | 1 | F=ASHR A |

- FULL CIRCUIT IMPLEMENTATION IN LOGISIM



Sample Test Cases

1. Test Cases For Arithmetic Operation:

A=0011 B=0011

| | | | | | |
|------|------|------|------|-------|--------------|
| S3=0 | S2=0 | S1=0 | S0=0 | Cin=1 | F=a+b+1=0111 |
|------|------|------|------|-------|--------------|



A=0011 B=0011

| | | | | | |
|------|------|------|------|-------|-------------------------|
| S3=0 | S2=0 | S1=0 | S0=1 | Cin=1 | F=a+b'+1=0000 Cout=1 |
|------|------|------|------|-------|-------------------------|



A=0011 B=0011

| | | | | | |
|------|------|------|------|-------|------------|
| S3=0 | S2=0 | S1=1 | S0=1 | Cin=0 | F=a-1=0010 |
|------|------|------|------|-------|------------|



2. Test Cases for Logical Operation

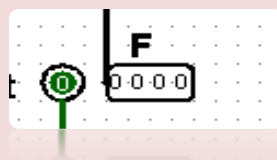
A=0011 B=0011

| | | | | |
|------|------|------|------|------------|
| S3=0 | S2=1 | S1=0 | S0=0 | F=A&B=0011 |
|------|------|------|------|------------|



A=0011 B=0011

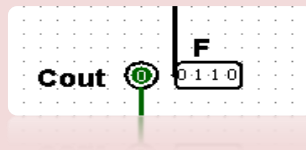
| | | | | |
|------|------|------|------|------------|
| S3=0 | S2=1 | S1=1 | S0=0 | F=A^B=0000 |
|------|------|------|------|------------|



3. Test Cases for Shift Operation

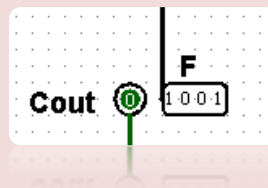
A=0011

| | | | | |
|------|------|-------|------|---------------|
| S3=1 | S2=0 | X2=00 | X1=0 | F= SHL A=0110 |
|------|------|-------|------|---------------|



A=0011

| | | | | |
|------|------|-------|------|---------------|
| S3=1 | S2=0 | X2=01 | X1=1 | F= CIR A=1001 |
|------|------|-------|------|---------------|



A=0011

| | | | | |
|------|------|-------|------|----------------|
| S3=1 | S2=0 | X2=10 | X1=1 | F= ASHR A=0001 |
|------|------|-------|------|----------------|

