1.

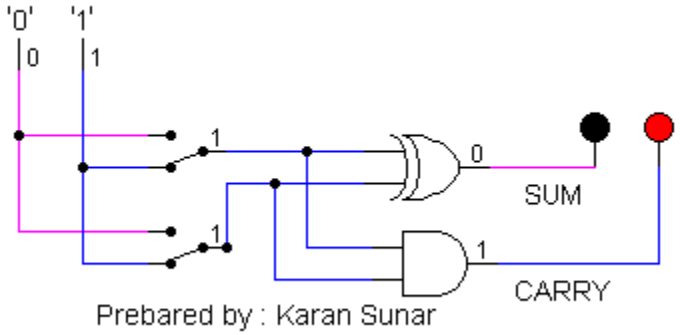
a. Define half adder.
Half adder is a circuit which is used to add two 1 bit binary digits.

b. Draw a truth table for the sum and carry of half adder.

A	B	SUM=(A XOR B)	CARRY= (A.B)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

c. Write the sop expression from the truth table.
SUM= A'.B+AB'
CARRY=A.B

d. Draw the circuit using logsim.



2.

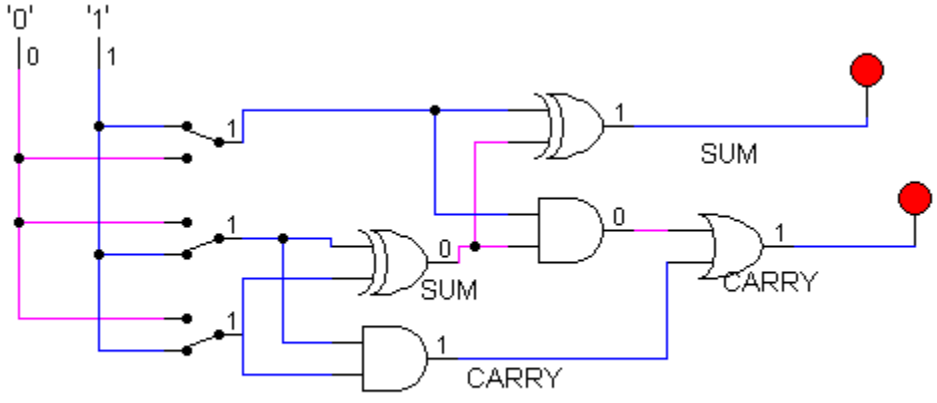
a. Draw the truth table for the outputs of the full adder.

A	B	C	X=(A.B'+A'.B)	A.B	X .C	X.C'+X'.C	(X.C)+(A.B)
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	1	0	0	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	1	0	1	0	1	1

b. Write the corresponding sop expression for sum and carry of full adder and simplify the expression

SUM=A'B'C+A'BC'+AB'C'+ABC
CARRY=A'BC+AB'C+ABC'+ABC

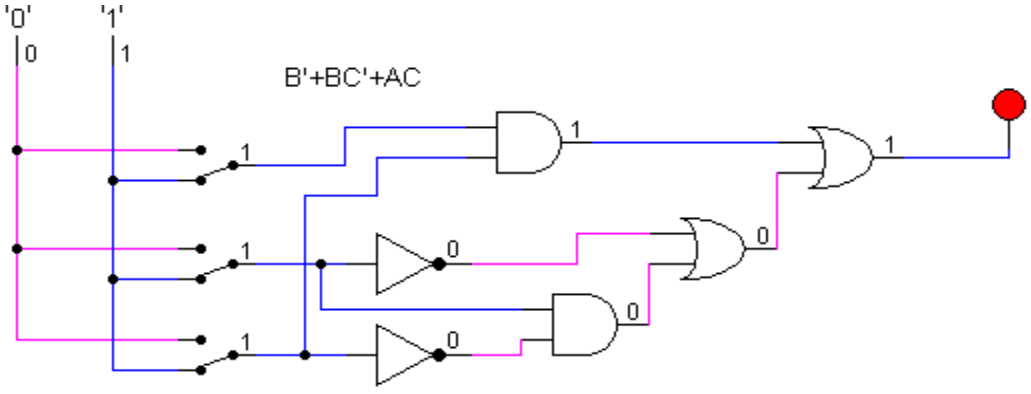
c. Draw full adder using two half adder and an OR gate.



3. Using the three stages of design, construct the circuits for the following input /output values. Here A, B and C are the inputs whereas D, E, F, G, H and I are outputs. *Note: Draw circuit diagram using logsim corresponding to the simplified expression of outputs D, E, F, G, H and I.*

A	B	C	D	E	F	G	H	I
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	1	1

D=A’B’C’+A’B’C+A’BC’+AB’C’+ABC+ABC’+AB’C=B’+BC’+AC



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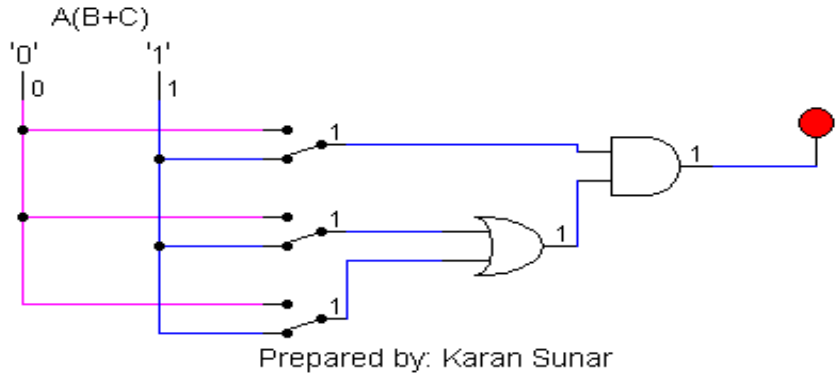
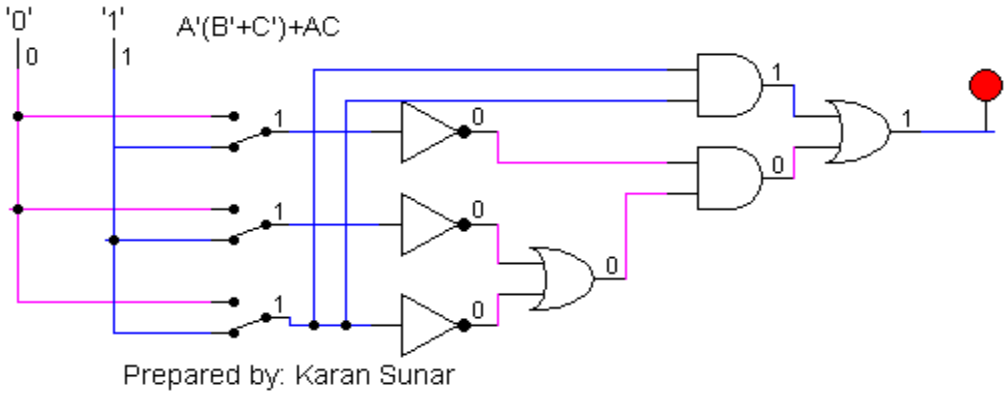
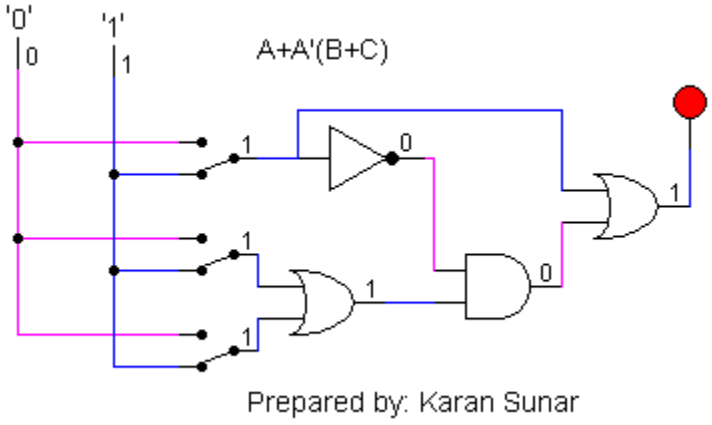
E=ABC+ABC'+AB'C =A(B+C)



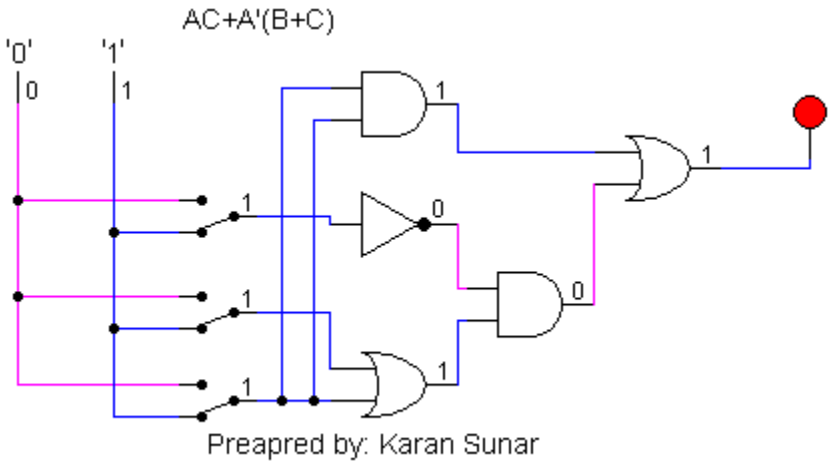
F=A'B'C'+A'B'C+A'BC'+ABC+AB'C =A'(B'+C')+AC



G=A'B'C+A'BC'+AB'C'+ABC+ABC'+AB'C+A'BC=A+A'(B+C)



H=A’B’C’+A’BC’+ABC+AB’C+A’BC=AC+A’(B+C)



I= A’B’C’ + A’B’C+A’BC’+AB’C’+ABC+ABC’ + A’BC =A’+A(B+C’)