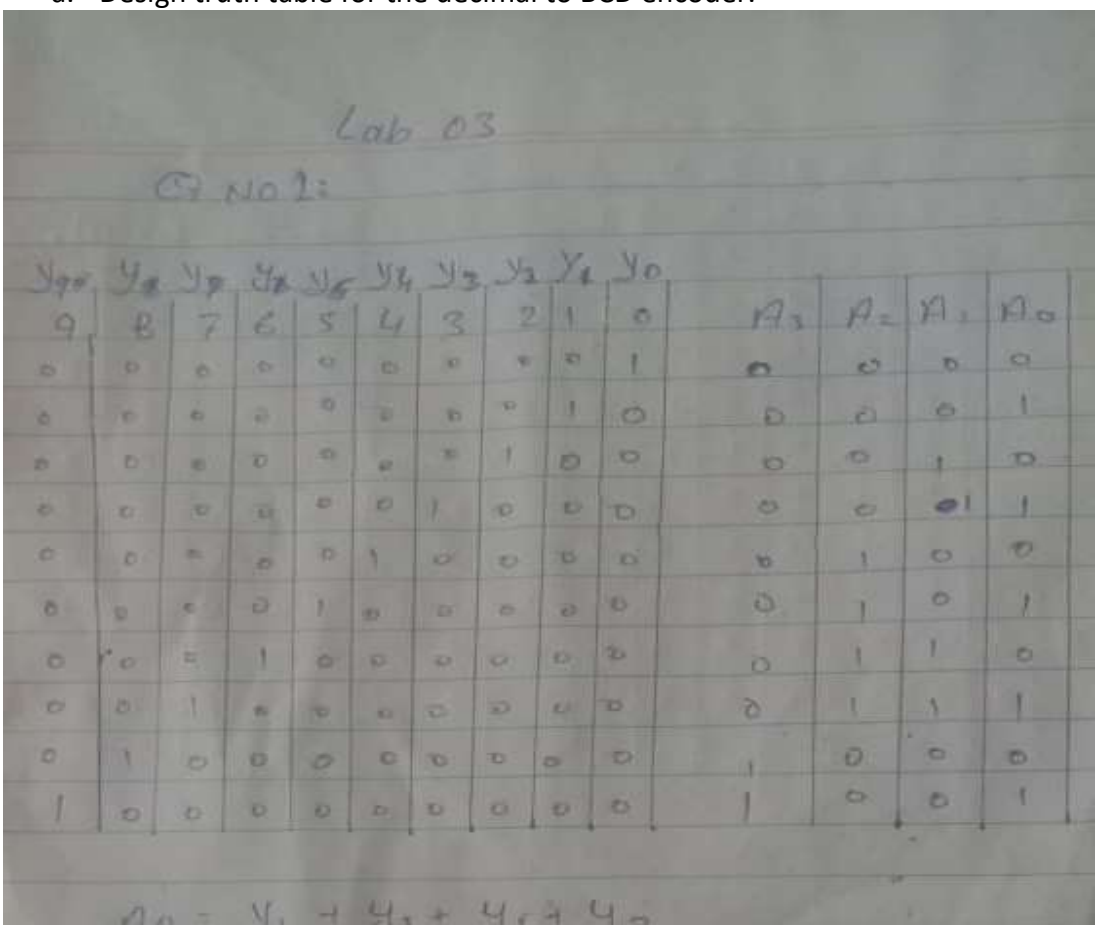
Lab 03

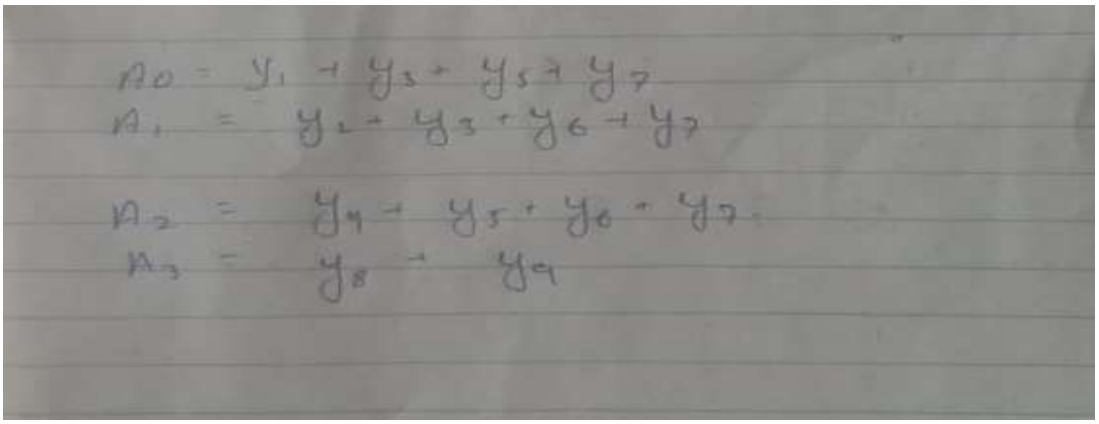
Handout#03: Behavioural Modelling for Combinational Circuits

1. Encoders are opposite to decoders, and are supposed to generate coded outputs from a single active
numeric input. A Decimal to BCD Encoder takes 10 inputs and generates corresponding 4-bit outputs.

a. Design truth table for the decimal to BCD encoder.



b. Derive the Boolean expression, and simplify if possible.



c. Implement the design using Verilog behavioural modelling, and provide code screenshot.

```
21
22  // Malak Majeed Ullah khan
23
24  module DEC_BCD(out, SW);
25  //Dimension and sizes
26  input wire [9:0] SW;
27  output reg [3:0] out;
28
29  //logic development using behavioral modelling
30  always@(*)
31  begin
32      if(SW[0] == 1)
33      out = 4'b0000;
34      else if(SW[1] == 1)
35      out = 4'b0001;
36      else if(SW[2] == 1)
37      out = 4'b0010;
38      else if(SW[3] == 1)
39      out = 4'b0011;
40      else if(SW[4] == 1)
41      out = 4'b0100;
42      else if(SW[5] == 1)
43      out = 4'b0101;
44      else if(SW[6] == 1)
45      out = 4'b0110;
46      else if(SW[7] == 1)
47      out = 4'b0111;
48      else if(SW[8] == 1)
49      out = 4'b1000;
50      else if(SW[9] == 1)
51      out = 4'b1001;
52      else
53      out = 4'bzzzz;
54  end
55
56  endmodule
57
```

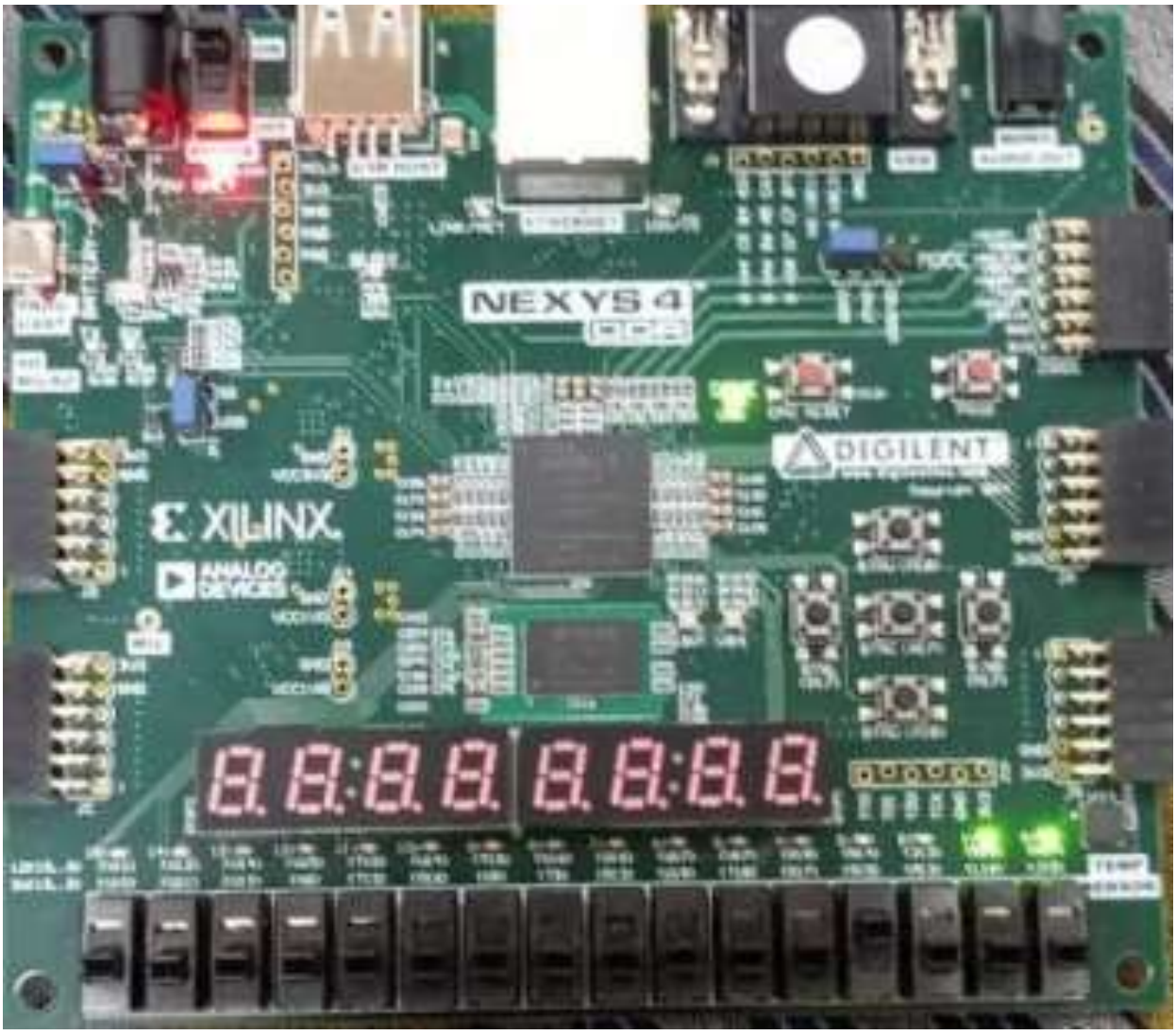
d. Investigate the design using Verilog test bench and simulations, and provide code screenshot.

```
58
59
60  module DEC_BCD_TB();
61  //Dimension and sizes
62  reg [9:0] SW;
63  wire [3:0] out;
64
65  //setting up data for simualtion
66  initial
67  begin
68       #00 SW = 10'b0000000000;
69       #10 SW = 10'b0000000001;
70       #10 SW = 10'b0000000010;
71       #10 SW = 10'b0000000100;
72       #10 SW = 10'b0000001000;
73       #10 SW = 10'b0000010000;
74       #10 SW = 10'b0000100000;
75       #10 SW = 10'b0001000000;
76       #10 SW = 10'b0010000000;
77       #10 SW = 10'b0100000000;
78       #10 SW = 10'b1000000000;
79       #10 $finish;
80  end
81
82  //displaying data on TCL console
83  initial
84  begin
85  $display("Author: Malak Majeed Ullah khan\n");
86  $monitor($time,"ns  input = %b, BCD output = %b",SW,out);
87  end
88
89  //instantiation
90  DEC_BCD DB0(out, SW);
91  endmodule
92
```

```
# run 1000ns
Author: Malak Majeed Ullah khan

                   0ns  input = 0000000000, BCD output = zzzz
                  10ns  input = 0000000001, BCD output = 0000
                  20ns  input = 0000000010, BCD output = 0001
                  30ns  input = 0000000100, BCD output = 0010
                  40ns  input = 0000001000, BCD output = 0011
                  50ns  input = 0000010000, BCD output = 0100
                  60ns  input = 0000100000, BCD output = 0101
                  70ns  input = 0001000000, BCD output = 0110
                  80ns  input = 0010000000, BCD output = 0111
                  90ns  input = 0100000000, BCD output = 1000
                 100ns  input = 1000000000, BCD output = 1001
$finish called at time : 110 ns : File "D:/FYP Slide/lab03/lab03.srcs/sources_1/new/DEC_BCD.v" Line 79
INFO: [USF-XSim-96] XSim completed. Design snapshot 'DEC_BCD_TB_behav' loaded.
```

e. Investigate the design using Nexys 4 DDR hardware. Provide the constraint file screenshot and
hardware output image.



2. **Conflict arises in encoders when more than two inputs are activated simultaneously. This issue can be resolved by prioritising the either LSB or MSB inputs. This encoder is called priority encoder.**

a. Design truth table for the decimal to BCD encoder.

b. Implement the design using Verilog behavioural modelling, and provide code screenshot.

```
22  // Malak Majeedullah khan
23
24  module DEC_priority_enc(Q, D);
25  //size and dimensions
26  input wire [9:0] D;
27  output reg [3:0] Q;
28
29  //logic for 8 bit priority encoder
30  always@(D)
31  begin
32      casex(D)
33      10'b0000000001 : Q = 4'b0000;
34      10'b000000001x : Q = 4'b0001;
35      10'b00000001xx : Q = 4'b0010;
36      10'b0000001xxx : Q = 4'b0011;
37      10'b000001xxxx : Q = 4'b0100;
38      10'b00001xxxxx : Q = 4'b0101;
39      10'b0001xxxxxx : Q = 4'b0110;
40      10'b001xxxxxxx : Q = 4'b0111;
41      10'b01xxxxxxxx : Q = 4'b1000;
42      10'b1xxxxxxxxx : Q = 4'b1001;
43      default: Q = 4'bzzzz;
44      endcase
45  end
46  endmodule
47
```

c. Investigate the design using Verilog test bench and simulations, and provide code screenshot.

```
50  module DEC_priority_enc_TB();
51  //inputs and outputs for simulations
52  reg [9:0] D;
53  wire [3:0] Q;
54
55  //setting up values for simulation
56  initial
57  begin
58      #00 D = 10'b0000000001;
59      #10 D = 10'b0000000010;
60      #10 D = 10'b0000000100;
61      #10 D = 10'b0000001000;
62      #10 D = 10'b0000010000;
63      #10 D = 10'b0000100000;
64      #10 D = 10'b0001000001;
65      #10 D = 10'b0010000001;
66      #10 D = 10'b0100000001;
67      #10 D = 10'b1000000001;
68      #10 $finish;
69  end
70
71  //displaying values on TCL console
72  initial
73  begin
74  $display("Author: Malak Majeed ullah khan\n");
75  $monitor($time,"ns  Input = %b, BCD_Output = %b", D, Q);
76  end
77
78  //instantiation
79  DEC_priority_enc DB0(Q, D);
80
81  endmodule
```

```
# }
# run 1000ns
Author: Malak Majeed ullah khan

                   0ns  Input = 0000000001, BCD_Output = 0000
                  10ns  Input = 0000000010, BCD_Output = 0001
                  20ns  Input = 0000000100, BCD_Output = 0010
                  30ns  Input = 0000001000, BCD_Output = 0011
                  40ns  Input = 0000010000, BCD_Output = 0100
                  50ns  Input = 0000100000, BCD_Output = 0101
                  60ns  Input = 0001000001, BCD_Output = 0110
                  70ns  Input = 0010000001, BCD_Output = 0111
                  80ns  Input = 0100000001, BCD_Output = 1000
                  90ns  Input = 1000000001, BCD_Output = 1001
$finish called at time : 100 ns : File "D:/FYP Slide/lab03/lab03.srcs/sources_1/new/DEC_priority_enc.v" Line 68
INFO: [USF-XSim-96] XSim completed. Design snapshot 'DEC_priority_enc_TB_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

d. Investigate the design using Nexys 4 DDR hardware. Provide the constraint file screenshot and
hardware output image.