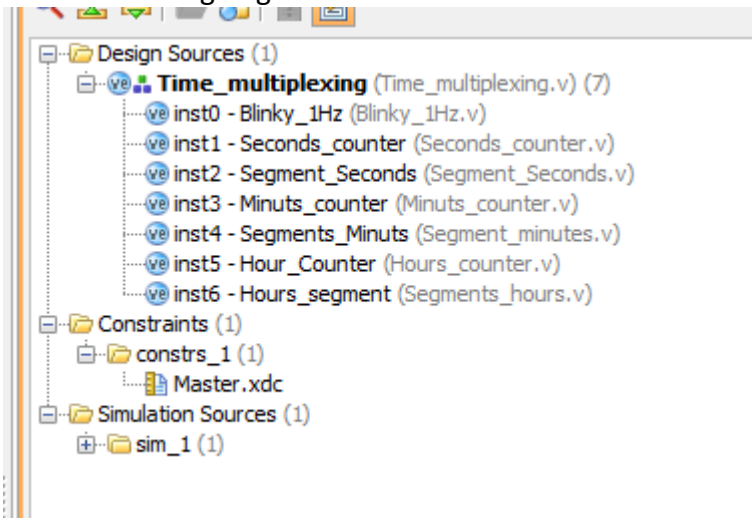
Lab 04

Handout#04: Verilog Behavioural Modelling For Sequential Circuits

1. Design a Verilog HDL based stop watch, which is able to display seconds, minutes, and hours.

a. Plan the designing and submit evidence.



b. Implement the design using Verilog HDL.

```
22  // Malak Majeedullah khan
23  module Time_multiplexing( clock_100Mhz,reset,Anode_Activate,LED_out,Start );
24  input clock_100Mhz; // 100 Mhz clock source FPGA
25  input reset; // reset
26  input Start;
27  output reg [7:0] Anode_Activate; // anode signals of the 7-segment LED display
28  output reg [6:0] LED_out;
29  wire [2:0] LED_activating_counter;
30  reg [19:0] refresh_counter;
31  wire clock_out;
32  wire [13:0] seg1;
33  wire [13:0] seg2;
34  wire [13:0] seg3;
35  wire [5:0] counter;
36  wire [5:0] min_counter;
37  wire [3:0] hours_counter;
38
39  Blinky_1Hz inst0(.clock_in(clock_100Mhz), .clock_out(clock_out));
40
41  Seconds_counter inst1(.clk(clock_out),.reset(reset),.counter(counter),.Start(Start));
42
43  Segment_Seconds inst2(.bcd(counter),.seg1(seg1));
44
45  Minuts_counter inst3(.clk(clock_out),.reset(reset),.min_counter(min_counter),.Start(Start));
```

```
22
23  //Malak Majeed Ullah khan
24  module Segment_Seconds(bcd,segl);
25
26  input [5:0] bcd;
27  output reg [13:0] segl;
28
29  always @ (bcd)
30  begin
31     case(bcd)
32            0: segl = 14'b0000001_0000001; // "0"
33            1: segl = 14'b0000001_1001111; // "1"
34            2: segl = 14'b0000001_0010010; // "2"
35            3: segl = 14'b0000001_0000110; // "3"
36            4: segl = 14'b0000001_1001100; // "4"
37            5: segl = 14'b0000001_0100100; // "5"
38            6: segl = 14'b0000001_0100000; // "6"
39            7: segl = 14'b0000001_0001111; // "7"
40            8: segl = 14'b0000001_0000000; // "8"
41            9: segl = 14'b0000001_0000100; // "9"
42
43            10: segl = 14'b1001111_0000001; // "10"
44            11: segl = 14'b1001111_1001111; // "11"
45            12: segl = 14'b1001111_0010010; // "12"
46            13: segl = 14'b1001111_0000110; // "13"
```

```
20  //////////////////////////////////////////////////////////////////////////////////
21  // Malak Majeed Ullah khan
22  module Seconds_counter(clk,reset,counter,Start);
23
24  input clk,reset,Start; //start stop buttton "Start"
25  output [5:0] counter;
26
27  reg [5:0] counter_up;
28
29  always @(posedge clk or posedge reset)
30  begin
31  if(reset)
32  counter_up<=6'd0;
33  else if(Start)
34  begin
35  counter_up<=counter_up+6'd1;
36  if(counter_up>=59)
37  begin
38  counter_up<=6'd0;
39  end
40  end
41  else
42  begin
43  counter_up<=counter_up;
44  end
```

F:/8th semster/DSD/lab 01/lab_04/lab_04.srcs/constrs_1/new/Master.xdc

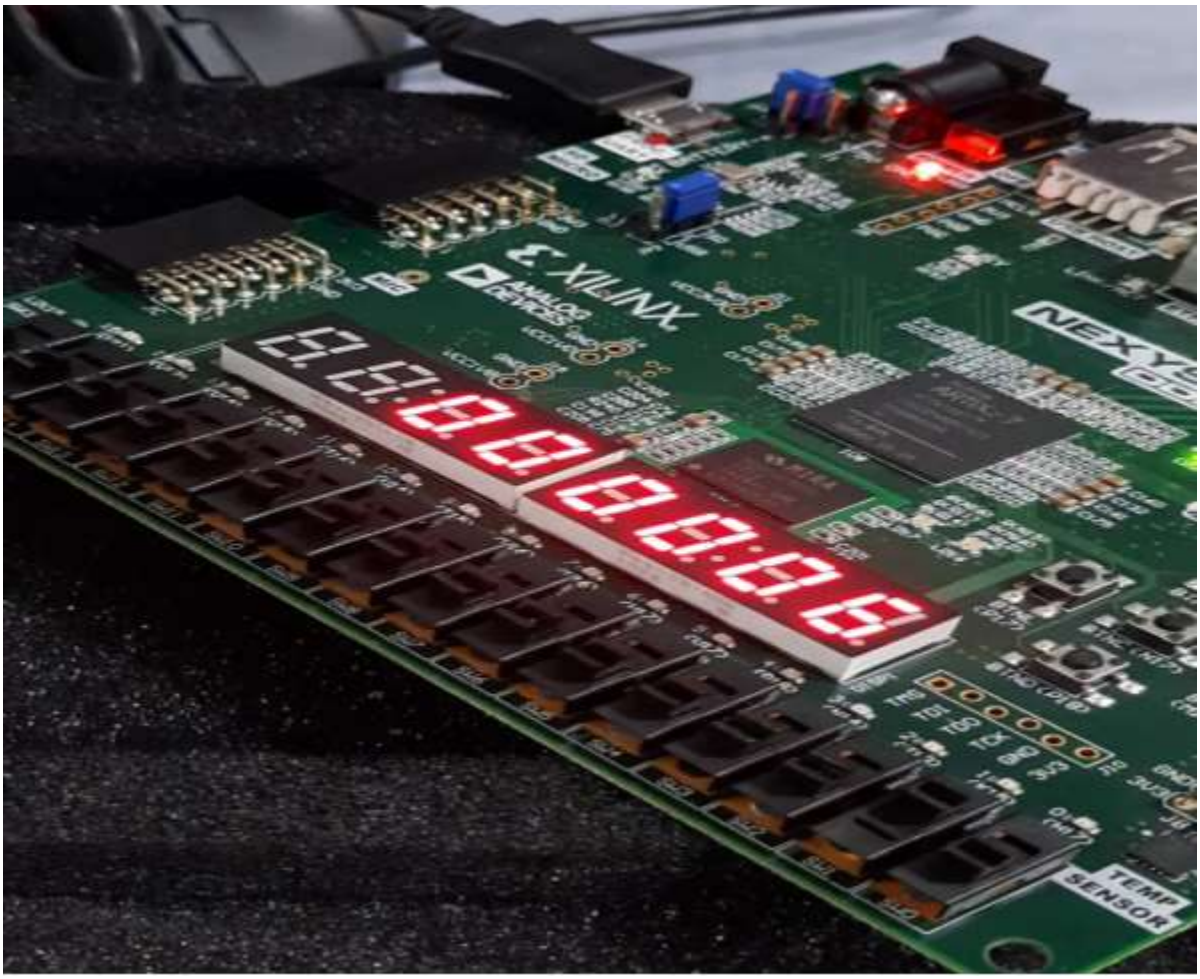
```
1  # Clock signal
2  set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clock_100Mhz}]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
3  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {clock_100Mhz}];
4
5
6  ##Switches
7
8  set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { reset }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
9  set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { Start }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
10
11 ##7 segment display
12
13 set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { LED_out[6] }]; #IO_L24N_T3_A00_D16_14 Sch=ca
14 set_property -dict { PACKAGE_PIN R10   IOSTANDARD LVCMOS33 } [get_ports { LED_out[5] }]; #IO_25_14 Sch=cb
15 set_property -dict { PACKAGE_PIN K16   IOSTANDARD LVCMOS33 } [get_ports { LED_out[4] }]; #IO_25_15 Sch=cc
16 set_property -dict { PACKAGE_PIN K13   IOSTANDARD LVCMOS33 } [get_ports { LED_out[3] }]; #IO_L17P_T2_A26_15 Sch=cd
17 set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports { LED_out[2] }]; #IO_L13P_T2_MRCC_14 Sch=ce
18 set_property -dict { PACKAGE_PIN T11   IOSTANDARD LVCMOS33 } [get_ports { LED_out[1] }]; #IO_L19P_T3_A10_D26_14 Sch=cf
19 set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports { LED_out[0] }]; #IO_L4P_T0_D04_14 Sch=cg
20
21 #set_property -dict { PACKAGE_PIN H15   IOSTANDARD LVCMOS33 } [get_ports { DP }]; #IO_L19N_T3_A21_VREF_15 Sch=dp
22
23 set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports { Anode_Activate[7] }]; #IO_L23P_T3_FOE_B_15 Sch=an[0]
24 set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports { Anode_Activate[6] }]; #IO_L23N_T3_FWE_B_15 Sch=an[1]
```

c. Write down the test bench and verify the design.

F:/8th semster/DSD/lab 01/lab_04/lab_04.srcs/sim_1/new/Stop_watch_TB.v

```
23  module Stop_watch_TB();
24  reg clock_100Mhz; // 100 Mhz clock source FPGA
25  reg reset; // reset
26  reg Start;
27
28  wire [7:0] Anode_Activate; // anode signals of the 7-segment LED display
29  wire [6:0] LED_out;
30
31  initial
32  clock_100Mhz = 0;
33
34   always
35   clock_100Mhz = ~clock_100Mhz;
36   initial
37      begin
38      #00 reset = 0;
39      #10 reset = 1;
40      @(negedge clock_100Mhz) reset = 0;
41
42      end
43      Time_multiplexing inst1 ( clock_100Mhz,reset,Anode_Activate,LED_out,Start );
44
45  endmodule
```


Name
Value
clock_100Mhz
reset
Start
Anode_Activate[7:0]
LED_out[6:0]


XILINX
TEMP SENSOR