Optimization of Parametric NTT Hardware Accelerator

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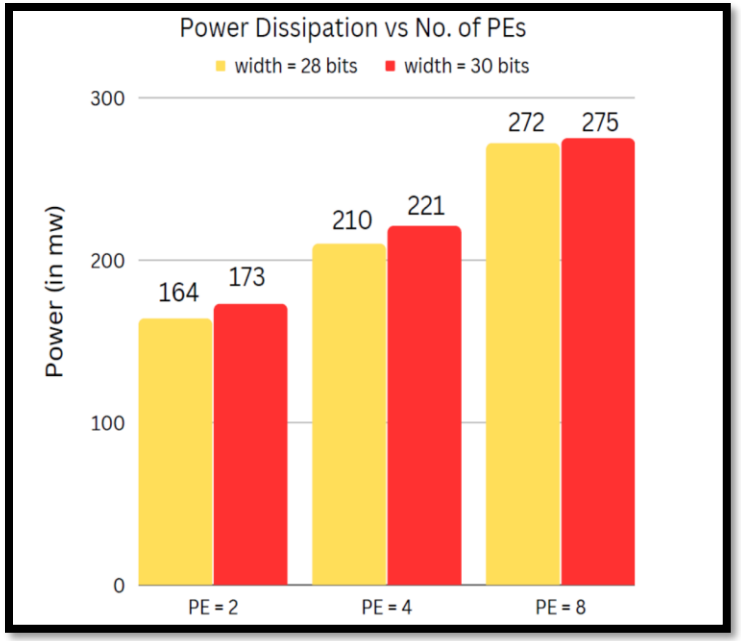
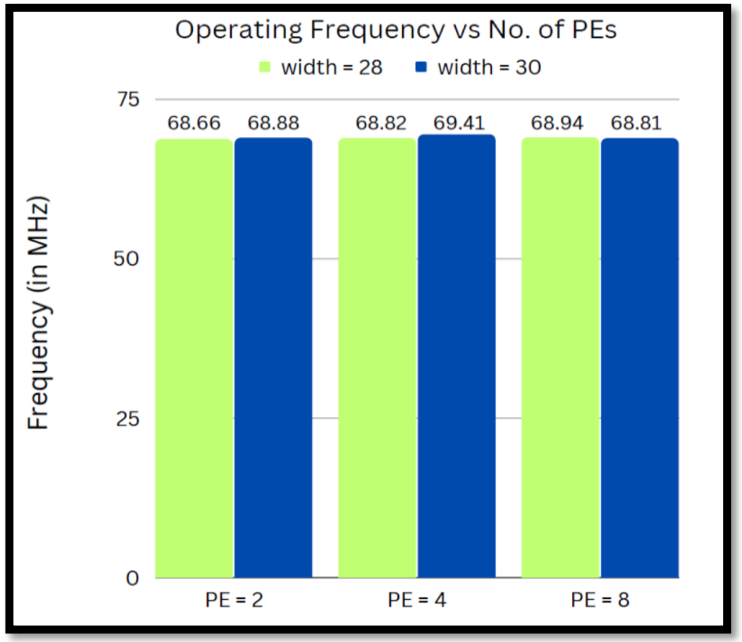
FPGA IMPLEMENTATION OF PARAMETRIC NTT HARDWARE ACCELERATOR

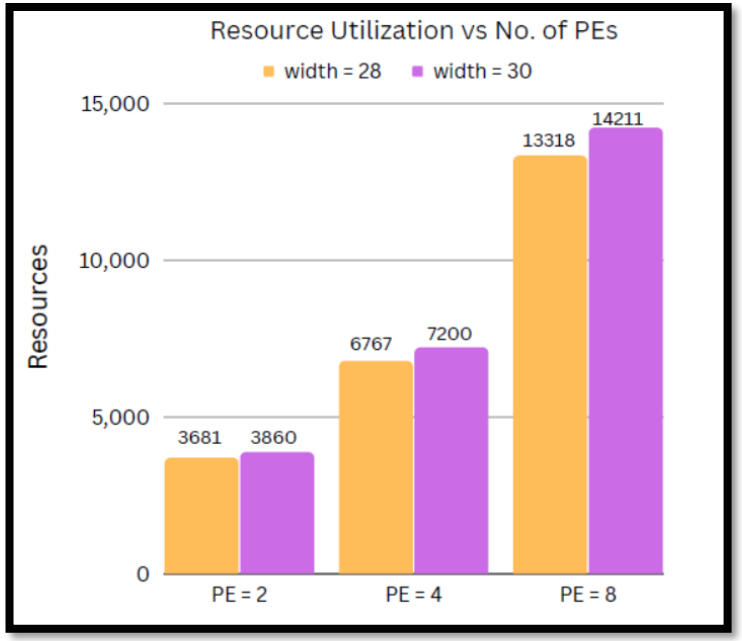
Conventional Algorithm



Power Analysis



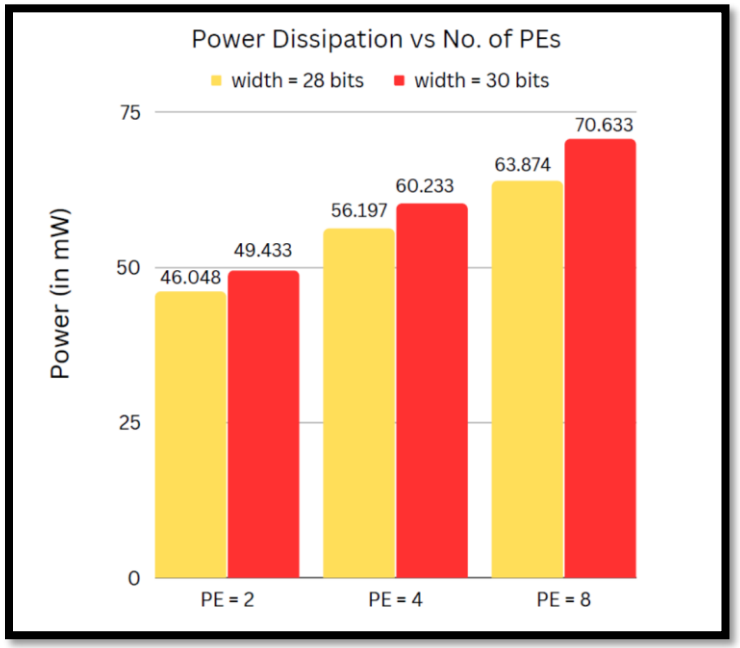
Performance Analysis



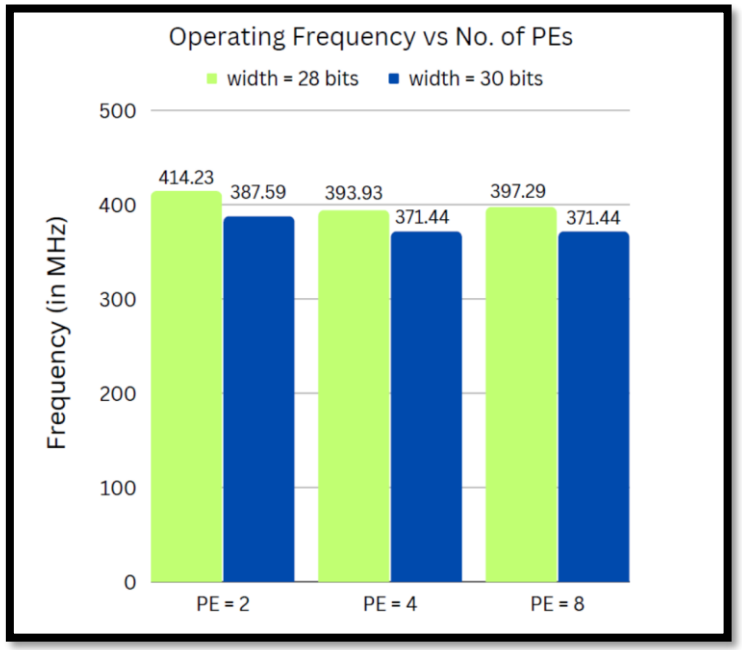
Area Analysis

ASIC IMPLEMENTATION OF PARAMETRIC NTT HARDWARE ACCELERATOR

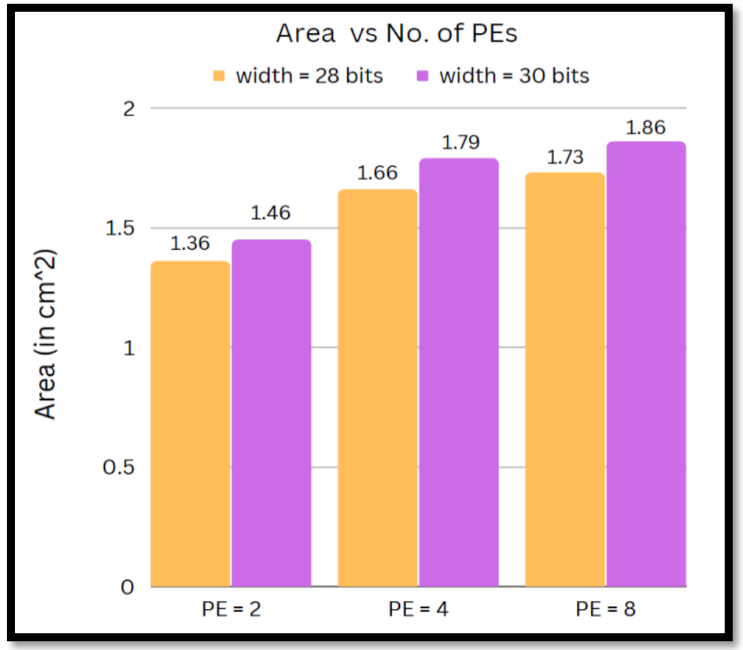
Conventional Algorithm



Power Analysis

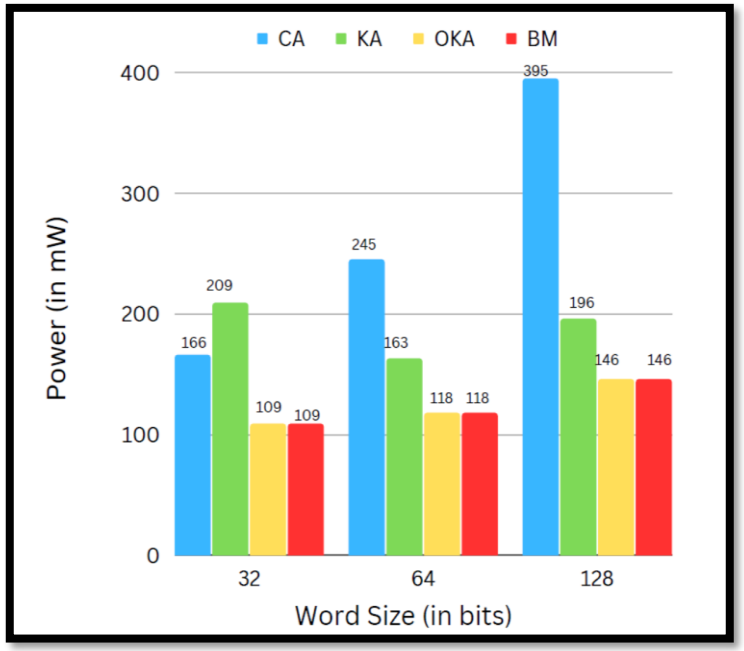


Performance Analysis

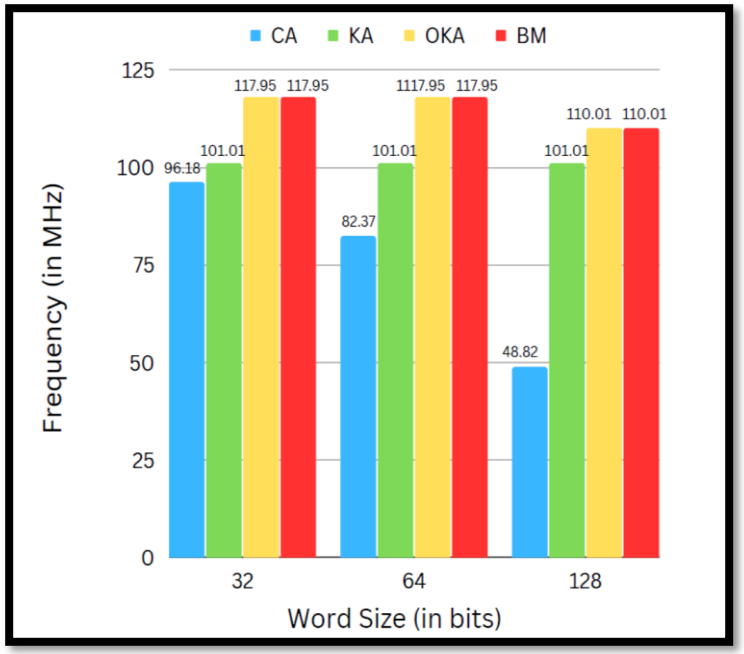


Area Analysis

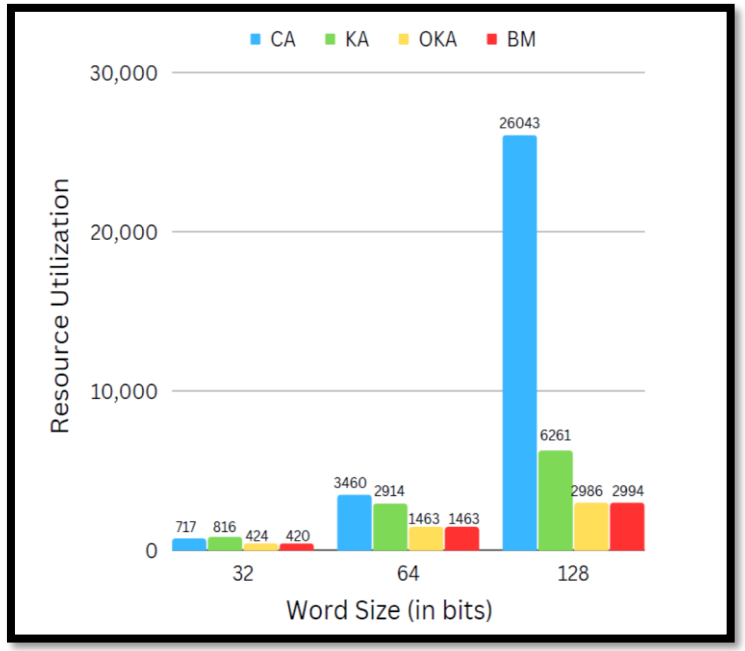
FPGA SYNTHESIS OF MODULUS MULTIPLICATION BLOCK OF PARAMETRIC NTT HARDWARE ACCELERATOR



Power Analysis

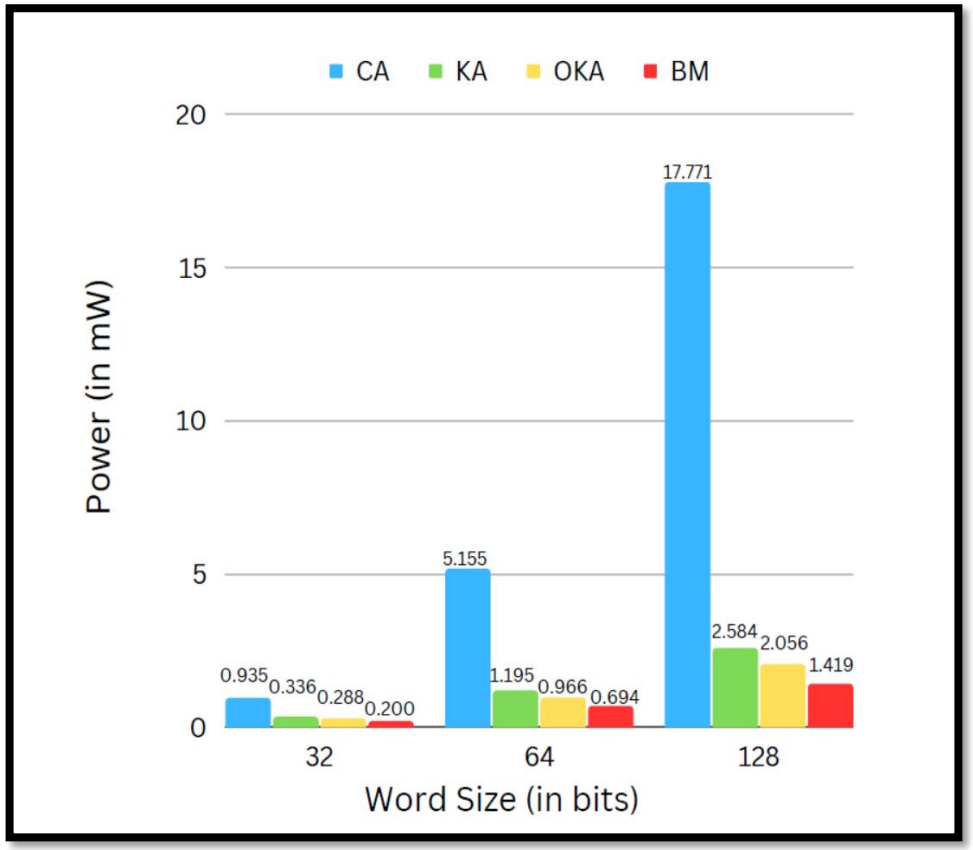


Performance Analysis

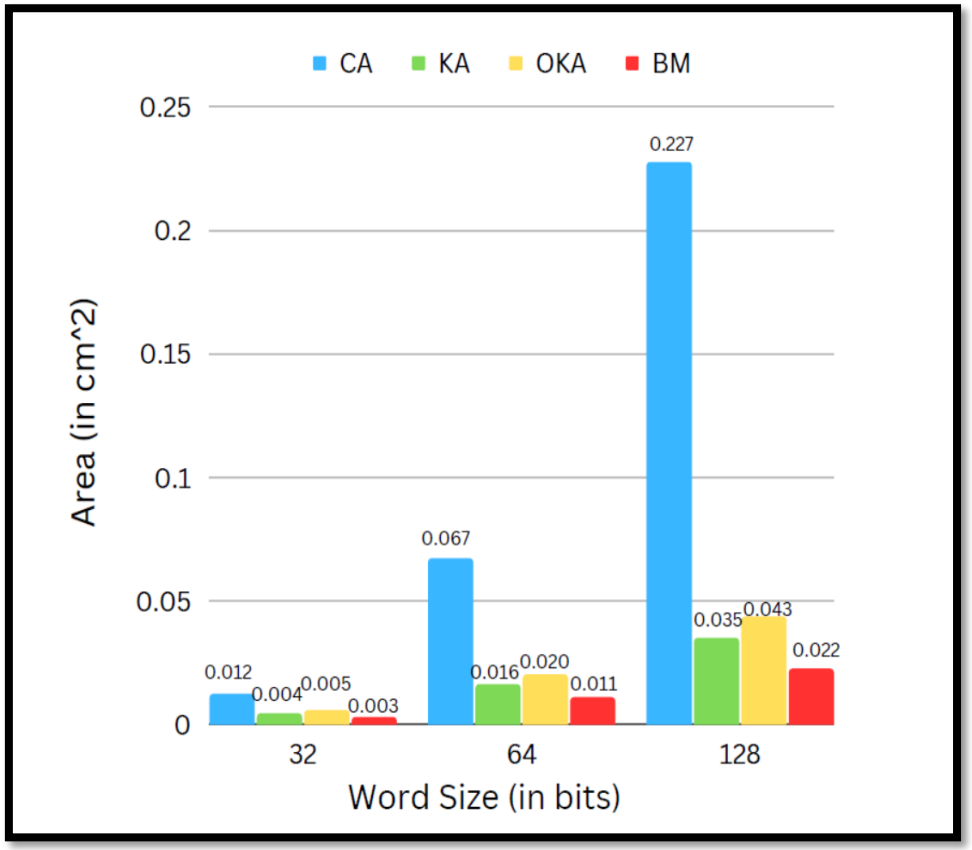


Area Analysis

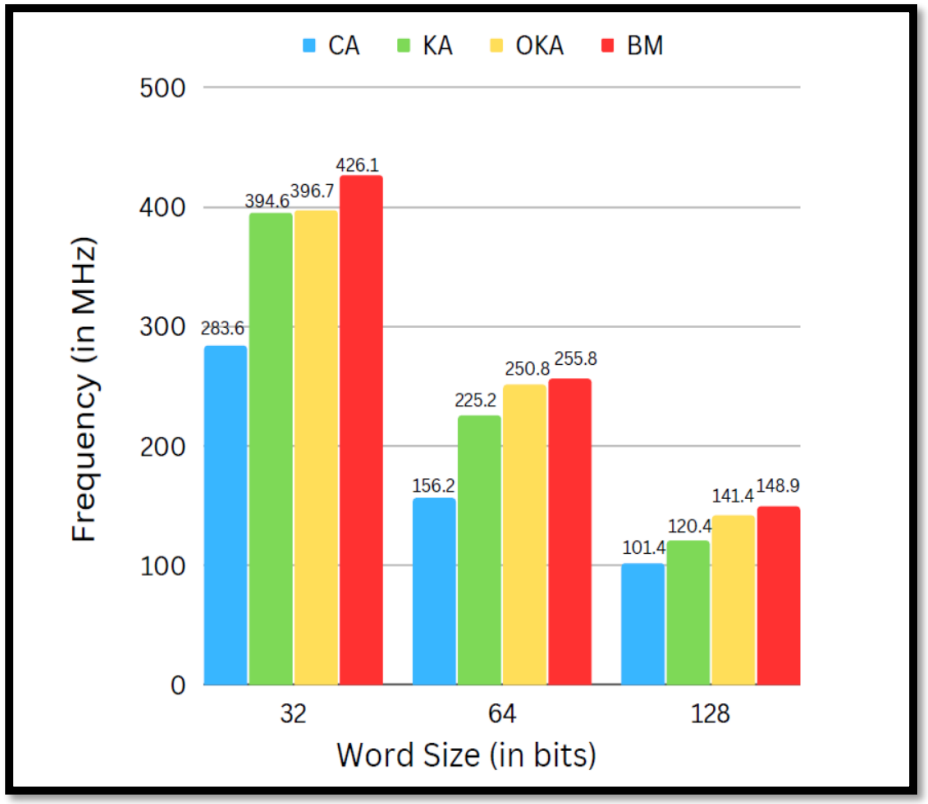
ASIC SYNTHESIS OF MODULUS MULTIPLICATION BLOCK OF PARAMETRIC NTT HARDWARE ACCELERATOR



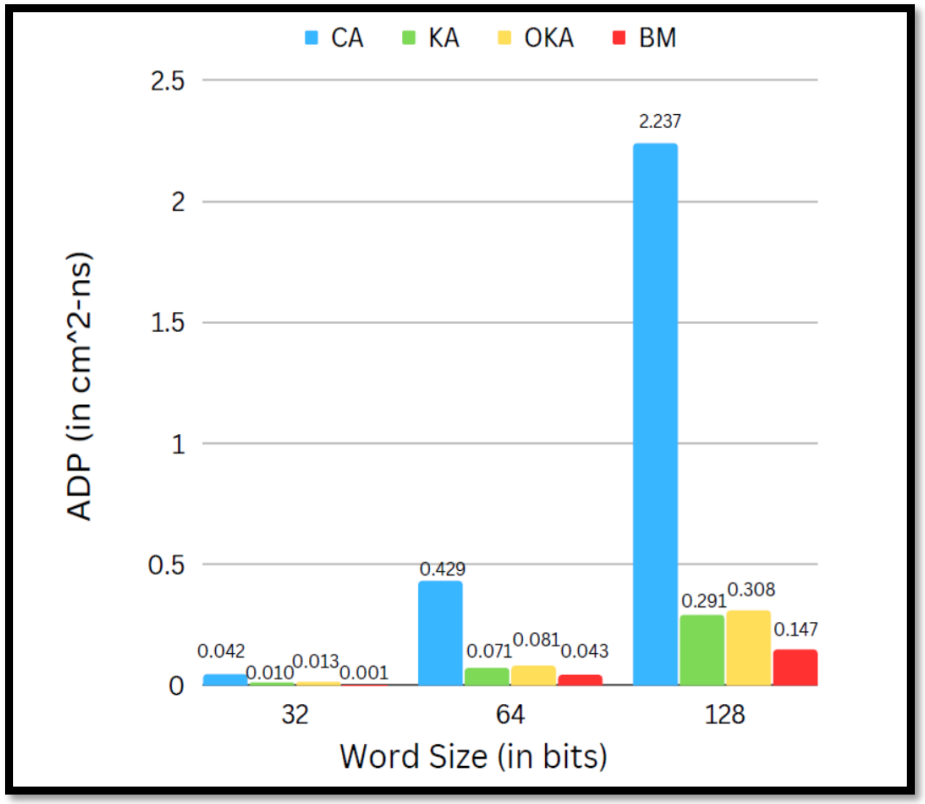
Power Analysis



Area Analysis

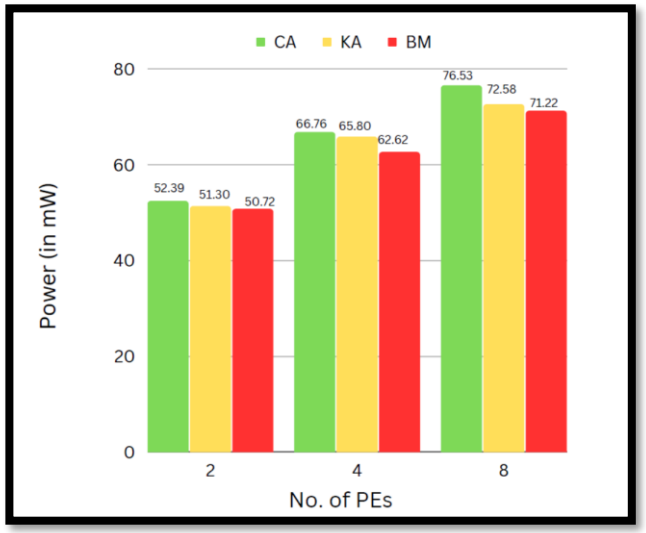


Performance Analysis

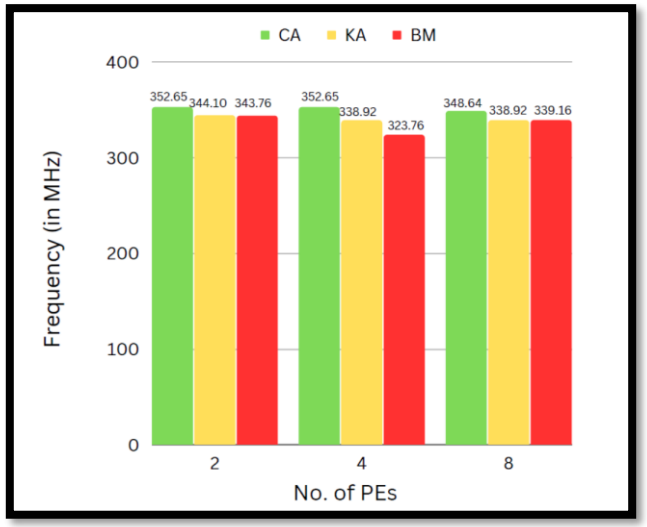


ADP Analysis

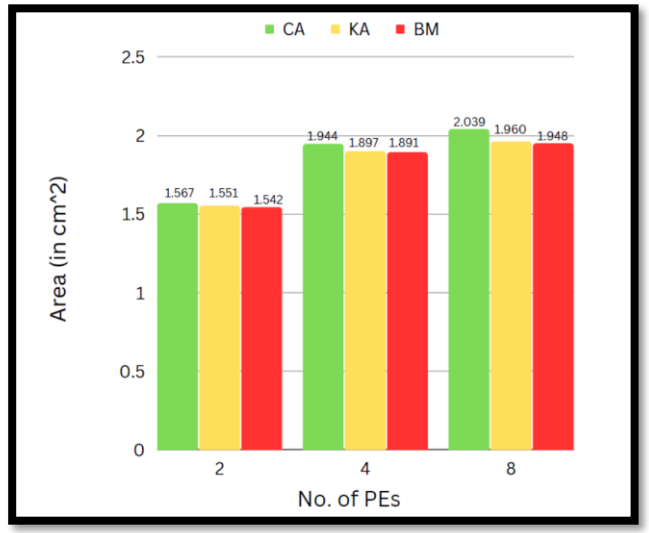
ASIC SYNTHESIS OF PARAMETRIC NTT HARDWARE ACCELERATOR USING CONVENTIONAL ALGORITHM, KARATSUBA ALGORITHM AND BOOTH MULTIPLIER RADIX-4 ALGORITHM



Power Analysis



Performance Analysis



Area Analysis