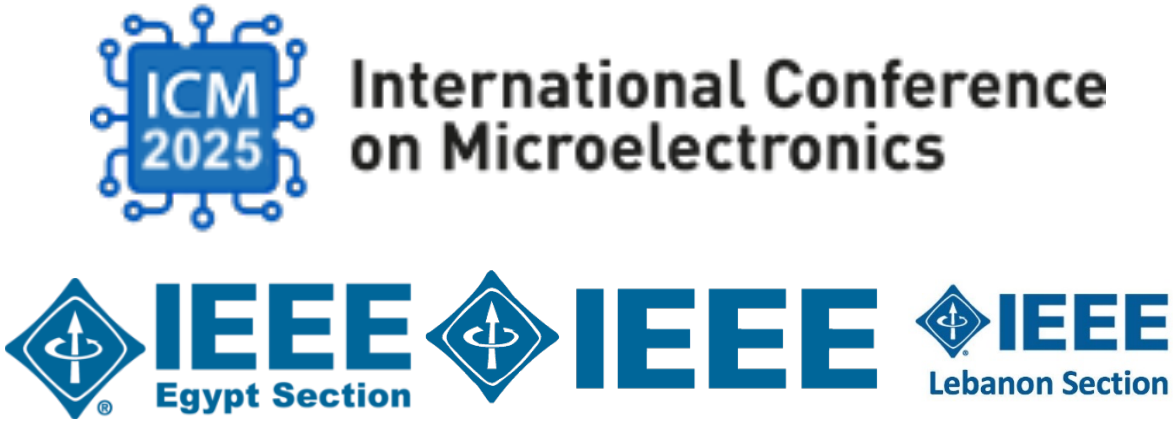

2025 International Conference on Microelectronics (ICM)
Program

2025 International Conference on Microelectronics (ICM)

Program (In Person)

Sunday, December 14	
Time (Cairo)	**Pavillon-1**
09:30 am-10:30 am	**Tutorial#1**: *From Papers to Physical Designs: Empowering LLM with Integrated Datasets* Dr. Yongfu Li, A tenured Associate Professor at Shanghai Jiao Tong University
10:30 am-11:00 am	**CB**: *Coffee Break*
11:00 am-12:00 pm	**Tutorial#2**: *Low-Power Analog Hardware Classifier Architecture for ML Applications: From A to Z* Dr. Vassilis Alimisis
12:00 pm-01:00 pm	**Tutorial#3**: *ML Accelerators on FPGAs: A Journey from Manual Design to AI-Assisted Workflows* Dr. Rashed Al Amin
01:00 pm-02:00 pm	**LB0**: *Lunch Break*
02:00 pm-03:00 pm	**Tutorial#4**: *Demystifying the Black Art: Towards a New Paradigm for Systematic Analog IC Design* Prof. Hesham Omran
03:00 pm-04:00 pm	**Tutorial#5**: *From Flexible Electronics to Universal Multimodal Sensor Chips: Concepts, Implementation and Application* Prof. Moustafa Nawito

Monday, December 15		
Time (Cairo)	**Pavillon-1**	**Pavillon-2**
09:00 am-10:00 am	*Opening Ceremony (Pavillon-1)*	
10:00 am-10:30 am	*Golden Break*	
10:30 am-11:30 am	**KeyNote#1**: *Practical Quantum Computing: The Status Quo* Prof. Ahmed El-Mahdy, Dean of the ITCS School	
11:30 am-01:00 pm	**S11(A)**: *Analog and RF Circuit Design Techniques-I*	**S11(B)**: *SS: Applying AI for and on Hardware: Cross-Layer Approaches for Security and Efficiency*
01:00 pm-02:15 pm	*Lunch Break*	
02:15 pm-04:15 pm	**S12(A)**: *Digital Systems*	**S12(B)**: *SS: Advances-in-Neuromorphic and Energy-Efficient-Analog/Digital-Computing-Architectures*
04:15 pm-05:45 pm	**S13(A)**: *Neuromorphic, In-Memory-and-Dataflow-Driven-Architectures-for-Next-Generation-AI*	**S23(B)**: *AI/ML/DL and Control Systems*
07:30 pm-09:30 pm	*Gala Dinner*	

Tuesday, December 16		
Time (Cairo)	**Pavillon-1**	**Pavillon-2**
09:00 am-10:00 am	**KeyNote#2**: *Advancing Monitoring Capabilities: The Role of Wearable Sensors in Advancing Healthcare, Environmental, and Marine Studies (Pavillon-1)* Prof. Khaled Nabil Salama, Professor, Electrical and Computer Engineering, King Abdullah University of Science and Technology	
10:00 am-10:30 am	*Coffee Break*	
10:30 am-12:00 pm	**S21(A)**: *Analog and RF Circuit Design Techniques-II*	**S21(B)**: *Bioinformatics and Biomedical Smart Applications*
12:00 pm-01:30 pm	**S22(A)**: *Smart Applications and New Trends for a Connected Industry of the Future*	**S22(B)**: *ASIC/FPGA/SoC/3D Circuits*
01:30 pm-02:30 pm	*Lunch Break*	
02:30 pm-03:00 pm	*Closing Ceremony*	
04:00 pm-07:30 pm	*Tour in Old Cairo (AZHAR, HUSSEIN and KHAN ELKHALILI)*	
Wednesday, December 17		
09:00 am-01:00 pm	*Visit to Grand Egyptian Museum*	

2025 International Conference on Microelectronics (ICM)

Program (OnLine)

Time (Cairo)	VirtualRoom-1	VirtualRoom-2	VirtualRoom-3	VirtualRoom-4
Sunday, December 14				
02:30 pm-03:00 pm 03:00 pm-04:00 pm	**Online1(A)**: *FPGA*	**Online1(B)**: *Bioinformatics and Biomedical Smart Applications*	**Online1(C)**: *FinFET/CNFET/MVL/Approximate Computing/Complexe HW*	**Online1(D)**: *ICM-General-I*
04:30 pm-06:00 pm	**Online2(A)**: *Analog and RF Circuit Design Techniques*	**Online2(B)**: *Neuromorphic, In-Memory-and-Dataflow-Driven-Architectures-for-Next-Generation-AI*	**Online2(C)**: *ICM-General-II*	**Online2(D)**: *ICM-General-III*

Sunday, December 14

Sunday, December 14 9:30 - 10:30 (Africa/Cairo)

Tutorial#1: From Papers to Physical Designs: Empowering LLM with Integrated Datasets

Dr. Yongfu Li, A tenured Associate Professor at Shanghai Jiao Tong University

Dr. Yongfu Li is a tenured Associate Professor at Shanghai Jiao Tong University (SJTU). He is also a Board of Governors (BoG), and R10 Member At Large of the IEEE Circuits and Systems (CAS) Society, an AdCom Members of the IEEE Biometrics Council, a member of the IEEE DataPort Steering Committee, Chair of the IEEE Data Competition Committee, the IEEE CASS Standard Activities Sub Division, and the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) Steering Committee. He has previously worked at the National University of Singapore and GLOBALFOUNDRIES before joining SJTU in 2019. Throughout his career, he has earned numerous academic, industrial, and IEEE awards, including the IEEE EAB Society/Council Professional Development Award (2023), IEEE MGA YP Achievement Award (2022), and IEEE YP Hall of Fame Award (2021).

Pavillon-1

In the realm of circuit logic and machine learning models (LLMs), the availability and quality of datasets play a pivotal role in advancing research and development. This talk explores the critical importance of datasets in driving circuit LLM, focusing on a diverse array of datasets ranging from academic papers to commercial device specifications and physical designs. We delve into specific techniques, such as converting images to netlists, web crawling for extracting paper content, and computer vision for extracting data from figures. By leveraging these datasets and techniques, we enhance the accuracy, efficiency, and applicability of LLM in circuit design and analysis.

Sunday, December 14 10:30 - 11:00 (Africa/Cairo)

CB: Coffee Break

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Sunday, December 14 11:00 - 12:00 (Africa/Cairo)

Tutorial#2: Low-Power Analog Hardware Classifier Architecture for ML Applications: From A to Z

Dr. Vassilis Alimisis

Dr. Vassilis Alimisis is an Analog IC Design Engineer and AI Computing Researcher. He received the B.Sc. in Physics (top 1%) and the M.Sc. degree in Electronics and Communications from the University of Patras, Greece, in July 2017 and March 2019 respectively. He received the Ph.D. degree from the National Technical University of Athens (NTUA), Greece, under the supervision of Professor Paul P. Sotiriadis in June 2024. His Ph.D. Thesis entitled "Integrated circuit architectures for classical and neural computing with applications in artificial intelligence" and research were supported and financed by the E.L.K.E. NTUA Scholarships. Currently, he is a Postdoctoral Researcher at Archimedes/Athena Research Center and Collaborating Researcher at the School of Electrical and Computer Engineering, NTUA, Athens, Greece and Adjunct Lecturer at the Department of Digital Industry Technologies, National and Kapodistrian University of Athens (NKUA). Since September 2025, Dr. Alimisis, has been awarded a postdoctoral research fellowship by the Bodossaki Foundation. During his PhD, he was a Teaching Assistant in undergraduate and graduate courses and supervised several Diploma Thesis (more than 20). He has authored and co-authored several journal articles and conference papers (more than 80 publications). His main research interests include analog microelectronic circuits, low power electronics, analog computing, neuromorphic computing, edge AI computing, circuit modeling, hardware accelarators and integrated circuit architectures with applications in artificial intelligence and machine learning. Also, in 2025, he received the PhD Thesis Award from the National Technical University of Athens, Greece (IAKOVOS GIOUROULIAN 2024 Award). He has received the Best Paper Award in the IEEE Int. Conf. on Microelectronics 2020, the Best Paper Award in the IEEE Int. Conf. on Microelectronics 2021, the Best Paper Award (3rd Place) in the IEEE Int. Conf. on Microelectronics 2023, the Best Paper Award in IEEE Symposium on Integrated Circuits and Systems Design (SBCCI) 2021, the Best Runner-Up PhD Symposium Paper Award in the 1st International Conference on Frontiers of Artificial Intelligence, Ethics, and Multidisciplinary Applications in 2023, the Best PhD Symposium Paper Award in the 2nd International Conference on Frontiers of Artificial Intelligence, Ethics, and Multidisciplinary Applications in 2024, the Best Student Paper Award in MOCAST 2025. He regularly reviews many IEEE transactions and conferences and serves on proposal review panels.

Pavillon-1

Abstract This tutorial provides a comprehensive introduction to the design and implementation of low-power analog hardware classifiers tailored for machine learning (ML) applications, with a focus on energy-constrained environments such as edge devices and biomedical wearables. With the growing need for fast, efficient, and real-time data processing, analog computing has re-emerged as a promising solution that enables in-memory computation and significantly reduces power consumption compared to conventional digital processors.

The tutorial is designed to guide participants from fundamentals to practical deployment, starting with an overview of analog signal processing principles, followed by an in-depth discussion of circuit-level implementations operating in the sub-threshold region and architectural design of classifiers such as Bayesian classifier, Voting classifier, Gaussian mixture model and Support vector machines. Emphasis is placed on understanding the power-performance trade-offs, the impact of non-idealities, noise resilience, and techniques for enhancing linearity and dynamic range in analog circuits.

Hands-on case studies based on real-life classification tasks (e.g., thyroid disease detection, ECG signal analysis, image edge detection) will be presented using Python, Cadence Virtuoso simulation tools and software-hardware codesign architectures. In addition, the tutorial provide an analysis related to hybrid analog- digital systems, training-aware hardware co-design, and prospects for reconfigurable analog machine learning chips.

This tutorial targets researchers, graduate students, and engineers interested in analog/mixed-signal IC design, edge ML systems, and energy-efficient hardware. Attendees will gain both theoretical insights and practical know-how to design analog classifier architectures that meet the demands of next-generation AI applications.

Sunday, December 14 12:00 - 1:00 (Africa/Cairo)

Tutorial#3: ML Accelerators on FPGAs: A Journey from Manual Design to AI-Assisted Workflows

Dr. Rashed Al Amin

Rashed Al Amin received his B.Sc. degree in Electrical and Electronics Engineering from the University of Dhaka, Bangladesh, and an M.Sc. degree (With Deans Award) in mechatronics from the University of Siegen, Germany. He obtained his PhD degree in Computer Science from the University of Siegen, Germany. Currently, He is working as a Post Doctoral Researcher and Lecturer at the Chair of Embedded Systems at the University of Siegen. His research interests include hardware for artificial intelligence, reconfigurable computing, and FPGA architecture. He aims to design the next-generation FPGA architecture to optimize deep learning workloads.

Room: Pavillon-1

The growing computational demands of machine learning (ML) have driven the development of specialized hardware accelerators. Among these, Field-Programmable Gate Arrays (FPGAs) have emerged as an ideal platform due to their reconfigurability, energy efficiency, and ability to achieve low-latency processing. FPGAs enable the customization of ML accelerator architectures to match specific application requirements, making them a preferred choice in domains such as autonomous systems, healthcare, and data analytics.

Despite their advantages, designing and verifying ML accelerators on FPGAs is inherently challenging. Engineers must navigate complex hardware-software co-design, optimize for limited resources, and rigorously verify functionality to ensure reliable operation. These challenges are compounded by the increasing demand for shorter development cycles and the need for more efficient workflows. Traditional manual design and verification approaches, while effective, are time-consuming and prone to human error.

This tutorial explores the transformative potential of AI-assisted workflows, specifically those leveraging Large Language Models (LLMs), to address these challenges. LLMs can assist in Hardware Description Language (HDL) generation, error detection, and verification, enabling designers to streamline development and reduce debugging time. This integration of manual expertise with AI-driven assistance represents a paradigm shift in FPGA-based ML accelerator design and verification.

The tutorial will begin by establishing the relevance of FPGAs in ML acceleration and the associated challenges of manual workflows. Participants will gain foundational knowledge in designing ML accelerators using manual methods, including optimization techniques and verification strategies. The session will then transition to an in-depth exploration of AI-assisted workflows, highlighting how LLMs can enhance HDL generation, optimize designs, and improve verification accuracy. Practical demonstrations and real-world case studies will illustrate the benefits and limitations of integrating LLMs into FPGA development.

By the end of the tutorial, participants will understand how to combine traditional and AI- assisted techniques to address the complexities of FPGA-based ML accelerator design. They will gain actionable insights into implementing efficient, reliable, and scalable hardware solutions that meet the demands of modern ML workloads. This tutorial is particularly valuable for hardware designers, researchers, and industry practitioners seeking innovative approaches to accelerate their workflows and improve design outcomes.

Sunday, December 14 1:00 - 2:00 (Africa/Cairo)

LB0: Lunch Break

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Sunday, December 14 2:00 - 3:00 (Africa/Cairo)

Tutorial#4: Demystifying the Black Art: Towards a New Paradigm for Systematic Analog IC Design

Prof. Hesham Omran

Dr. Hesham Omran received the B.Sc. (with honors) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2007 and 2010, respectively, and the Ph.D. degree from King Abdullah University of Science and Technology (KAUST), Saudi Arabia, in 2015, all in Electrical Engineering. From 2008 to 2011, he was a Design Engineer with Si-Ware Systems (SWS), Cairo, Egypt, where he worked on the circuit and system design of the first miniaturized FT-IR MEMS spectrometer (NeoSpectra), and a Research and Teaching Assistant with the Integrated Circuits Lab (ICL), Ain Shams University. From 2011 to 2016 he was a Researcher with the Sensors Lab, KAUST. He held internships with Bosch Research and Technology Center, CA, USA, and with Mentor Graphics, Cairo, Egypt. In 2016, he rejoined the ICL, Ain Shams University, where he is currently an Associate Professor. He created the Mastering Microelectronics YouTube channel, which specializes in microelectronics education for the Arab world and has over 18,000 subscribers. He co-founded Master Micro in 2020 to develop The Analog Designer's Toolbox (ADT), a novel EDA tool that is defining a new paradigm for analog IC design. Dr. Hesham has received several awards, including the Egyptian State Encouragement Award for Engineering (2019), the Ain Shams University Encouragement Award for Technology (2021), the Design Automation Conference (DAC) Innovator's Award (2022), and the UNESCO AlFozan Award for Young Scientists in STEM (2023). He has published over 50 papers in international journals and conferences. His research interests are in the design of analog and mixed-signal integrated circuits, with a special focus on analog and mixed-signal CAD tools and design automation.

Room: Pavillon-1

As the demand for more powerful and efficient custom chips continues to rise, there is an increasing need for experienced and knowledgeable chip designers. However, analog design remains a "black art" that requires years of practice to master. The increased complexity of transistor models has aggravated the problem and widened the gap between simple analytical models and (post-layout) simulation results. Consequently, the design process is tending towards a trial-and-error process on simulation tools, which calls for a new paradigm for analog IC design that restores the designer's intuition, boosts productivity, and makes analog IC design a systematic and optimized process. The use of precomputed look-up tables (LUTs) to enable intuitive and visualized design scenarios is a promising candidate for this new design paradigm. This tutorial will provide insights in using precomputed LUTs to redefine sizing at the device and circuit level. We will explain how LUTs can capture the effective parameters of an arbitrary device using black box characterization. Next, we will see how the LUTs can be used to enable sizing the devices using their electrical parameters instead of using the geometry. Finally, we will see practical design examples for design space exploration, interactive sensitivity analysis, feasibility studies, and what-if scenarios for several analog building blocks.

Sunday, December 14 3:00 - 4:00 (Africa/Cairo)

Tutorial#5: From Flexible Electronics to Universal Multimodal Sensor Chips: Concepts, Implementation and Application

Prof. Moustafa Nawito

Moustafa Nawito was born in 1979 in Cairo Egypt. He attained his B.Sc. in Electronics and Electrical Communication Engineering from the faculty of engineering at Cairo University in 2002 and his M.Sc. in RF Electronics from the German university in Cairo in 2007. In 2017 he attained his Dr.-Ing. (Magna cum laude) in Microelectronics from Stuttgart University in Germany. In 2008 he was appointed as technical manager of the research center for digital broadcasting at GUC in cooperation with Fraunhofer Institute IIS in Erlangen Germany. During this time, he conducted several seminars and workshops on advanced ASIC design for industrial and academic partners. He also cofounded the "Center for Artificial Intelligence" and led a research team to win the international RoboCup scientific competition in 2009. He was also a co-founder of the Egyptian IEEE chapter for computational intelligence which received the best chapter award in 2009.

In addition, he was the scientific project director of various German and international research projects. In 2017 he founded the startup company Polymath Analog where he works in close cooperation with customers to provide innovative and reliable ASIC solutions for Internet of Things, Industry 4.0 and automotive applications, with special emphasis on advanced analog design. He served as lead consultant for the development of a new generation of implantable image sensors for the company Retina Implant AG. In 2020 he joined the IU International University of Applied Sciences as a professor and founding chair of the electrical engineering program. He successfully led the development of the curriculum and the academic accreditation of the newly established department. He also serves as scientific reviewer on several committees for the appointment of new Professors. Prof. Nawito is the author of several publications, including the textbook "CMOS Readout Chips for Implantable Multimodal Smart Biosensors (Springer)". His research interests include the design of low power data converters, high precision sensors and organic and implantable electronics. He is a senior member of IEEE, VDE, OE-A and other technical societies and associations. In addition, he is an expert reviewer for the accreditation of engineering university programs for the EU and has conducted on-site reviews in 4 continents.

Room: Pavillon-1

Flexible and multimodal sensors are transforming modern electronics, driving advances in smart healthcare, wearable monitoring, Industry 4.0, and the Internet of Things. Yet, current approaches to sensor chip development remain fragmented. Application-Specific Integrated Circuits (ASICs) provide high accuracy and efficiency but are costly and limited to niche applications, while general-purpose solutions such as FPGAs and microcontrollers offer adaptability at the expense of miniaturization, power efficiency, and multifunctionality.

This tutorial introduces a new design paradigm: Universal Multimodal Actuator Sensor Chips (UMASCs). These platforms combine the precision of ASICs with the versatility of programmable solutions, enabling circuits that operate across multiple sensing and actuation modalities. UMASCs achieve universality along two dimensions: circuit functionality and form factor adaptability. On the circuit level, UMASCs leverage reconfigurable building blocks-such as amplifiers, OTAs, ADCs, DACs, filters, and waveform generators-that can be reused across electrophysiological, electrochemical, optical, and mechanical measurements. On the physical level, they can be implemented in bulk CMOS, ultra-thin chips, hybrid systems-in-foil, or through integration with organic and printed non-organic transistors.

In the beginning a review of flexible and organic electronics is presented, establishing the foundations of materials, fabrication techniques, and circuit design challenges. The UMASC framework is then discussed, including its design requirements, building blocks, and technical feasibility in mature CMOS technologies. Case studies will highlight applications in biomedical implants (electrophysiology, neurostimulation, impedance spectroscopy), biosensors (glucose, oxygen, pH), wearable optical monitoring (PPG, NIRS), and IoT/industrial sensing (flexible smart labels, multimodal monitoring). Participants will gain both a conceptual understanding and a practical methodology for designing universal multimodal sensor platforms that are future-ready, adaptable, and scalable. The tutorial is intended for engineers, researchers, and graduate students working in circuit

Sunday, December 14 2:30 - 4:00 (Africa/Cairo)

Online1(A): FPGA

VirtualRoom-1

Chair: Abdallah Kassem (Notre Dame University, Lebanon)

Inside GateMate: Analysis and Benchmarking of a New FPGA Architecture
Tarik Ibrahimović (University of Sarajevo & Faculty of Electrical Engineering, Bosnia and Herzegovina); Nedim Osmic (University of Sarajevo, Bosnia and Herzegovina & Faculty of Electrical Engineering, Bosnia and Herzegovina)

Prompt Engineering for FPGA Design: LLM-Driven Workflows Beyond HLS
Richard Yarnell, Paul Amoruso and Ronald F DeMara (University of Central Florida, USA)

TinyCNet: Turning Pretrained-CNNs to Edge-Ready FPGA Logic
Mukesh Narayana Gadde, Vipin Kizheppatt and A. Amalin Prince (Birla Institute of Technology and Science Pilani, India)

Routability-Aware FPGA Design Automation with Graph Transformer Models
Challa Murali Krishna Yadav and B Naresh Kumar Reddy (NIT Tiruchirappalli, India); Y Charan Krishna (Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Che, India); Sarangam K (NIT Warangal, India)

Hybrid FSR-Based Pseudo-Random Number Generator on FPGA for Encrypting Biometrics
Keerthana Menon (IIIT Kottayam, India); Goutam Mali (Indian Institute of Information Technology Kottayam, India); Nalesh S (Cochin University of Science & Technology, Kochi, Kerala, India); Babita Jajodia (Indian Institute of Information Technology Guwahati, India); Kala S (Indian Institute of Information Technology Kottayam, India)

Secure and Optimized IP Design Using Key-Driven Cipher-Based Multi-Layer Encrypted HLS Watermarking Integrated with FA Based Exploration
Anirban Sengupta, Vishal Chourasia and Nabendu Bhui (Indian Institute of Technology Indore, India)

Sunday, December 14 2:30 - 4:00 (Africa/Cairo)

Online1(B): Bioinformatics and Biomedical Smart Applications

Room: VirtualRoom-2

A Unified Deep Learning and Retrieval-Augmented System for Chest X-Ray Decision Support

Mennatallah Habiba, Ahmed Abozeid and Adham Moussa (Egypt-Japan University of Science and Technology (EJUST), Egypt); Hanin Eltabakh (Egypt-Japan University of Science and Technology (E-JUST), Egypt); Mariem Abdelbaki (Egypt-Japan University of Science and Technology, Egypt); Sameh Sherif (Egypt-Japan University of Science and Technology (E-JUST), Egypt)

Leveraging AI for Precision Muscle Analysis and Performance Optimization

Shereen Afifi (German University in Cairo, Egypt); Daniel Ashraf Ekdawi (Media Engineering and Technology, German University in Cairo, Egypt); Duaa Zuhair Al-hamid (Auckland University of Technology, New Zealand); Radwa E Taha (German University in Cairo, Egypt); Mohammed A.-Megeed Salem (German University in Cairo & Ain Shams University, Egypt); Ibrahim Y Noshokaty (Enosh Science Center, Egypt)

A Comparative Study of Convolutional Layer Depths and Activation Functions in the Detection and Classification of Diabetic Retinopathy

Saxon Vandenwollenberg, Sneha Chitte, Sudipta Modak and Esam Abdel-Raheem (University of Windsor, Canada)

Lung Cancer Detection Using Deep Learning Models: A Comparative Study of Preprocessing Techniques with Explainable AI Integration

Hawraa Hotiet (University of Genova, Italy); Marwan AlHawat (LIU, Lebanon); Abdallah Kassem (Notre Dame University, Lebanon); Mohamad Abou Ali (University of the Basque Country, Spain & Lebanese International University, Lebanon)

Enhanced Performance High-Accuracy Wearable Non-EEG Seizure Detection Signal System

Michael H Zakhari (Cairo University, Egypt); Hassan Mostafa (University of Toronto, Canada)

SkyAid: A Low-Cost Autonomous Hexacopter for Resilient Medical Supply Delivery in GPS-Denied Environments

Mohamad Abou Ali (University of the Basque Country, Spain & Lebanese International University, Lebanon); Khallad Mustafa and Reem Kisanieh (Lebanese International University (LIU), Lebanon); Mohamad Hajj-Hassan (Lebanese International University, Lebanon); Ali H Cherry (International University of Beirut, Lebanon); Abdallah Kassem (Notre Dame University, Lebanon)

Sunday, December 14 2:30 - 4:00 (Africa/Cairo)

Online1(C): FinFET/CNFET/MVL/Approximate Computing/Complexe HW

VirtualRoom-3

Chair: Mohamad Kassab (MAJKassab NET, Lebanon)

On the Extension of Boundary Scan Testing for Approximate Computing
Mahmoud Saleh Masadeh (Hijjawi Faculty for Engineering, Yarmouk University, Irbid, Jordan); Houssam Massalkhi (Concordia University, Montrea, Jordan); Doa'a Mohammad Aloqoul (Yarmouk University, Jordan); Omar AlShorman (Alshrouk Trading Company, Saudi Arabia)

Energy-Efficient Approximate Prewitt Filter Design
Mahmoud Saleh Masadeh (Hijjawi Faculty for Engineering, Yarmouk University, Irbid, Jordan); Abdelrahman Idries (Concordia University, Canada); Omar AlShorman (Alshrouk Trading Company, Saudi Arabia)

Analysis of the ZTC Bias Points in the FinFET Gate Capacitance and Transition Frequency
Miguel F Coelho (Ciências, Universidade de Lisboa, Portugal); Pedro Toledo (Synopsys, Portugal); Alexandra Matos (NOVA SoS and Technology, France); Rafael Martins and Rafael Ferreira (NOVA SoS and Technology, Portugal); Boyapati Subrahmanyam (Synopsys, Ireland); Luis Oliveira (DEE, FCT NOVA & Monte da Caparica, Portugal); Jose Soares Augusto (Universidade de Lisboa, Faculdade de Ciências, Portugal); João Oliveira (FCT-UNL & Uninova, Portugal)

Comparative Robustness Analysis of Different Adder Topologies Using ASAP7 FinFET Technology
Umayia Mushtaq (Jamia Millia Islamia New Delhi India, India); Mohammad Akram (Jamia Millia Islamia, New Delhi, India); Dinesh Prasad (Jamia Millia Islamia, India)

Proposed a Ternary Adder Using CNTFET
Ramzi A. Jaber (Notre Dame University, Lebanon)

Utility of Non-Aligned Double Gate FET in the Design of Multi-Logic Digital Gate
Sri Lakshmi Sangam (VIT-AP University, India); Arun Kumar Sinha (Vellore Institute of Technology, Andhrapradesh, India)

Sunday, December 14 2:30 - 4:00 (Africa/Cairo)

Online1(D): ICM-General-I

VirtualRoom-4

Chair: Ahmed Madian (Nile University, Egypt)

A Frequency Automated Spurless Large Bandwidth EOPLL for a High Resolution LiDAR
Aya Ghobashy (Cairo University, Egypt)

SLM-Arch: Trade-Off Analysis and Optimized Hardware Design for Small Language Models
Lantian Li (Nanyang Technological University, Singapore & NTU, Singapore); Mohamed Sabry (NTU, Egypt)

Optimized Regression Modeling for Predicting Electrical Resistance in 3D Structures
Nashaat El Halabi (City St George's, University of London, United Kingdom (Great Britain) & American University of Science and Technology, Lebanon); Enayet Rahman (City University London, United Kingdom (Great Britain)); Mohamad Rahal (American University of Science and Technology, Lebanon); Michael Powner (City St Georges, University of London, United Kingdom (Great Britain)); Iasonas Triantis (City University London, United Kingdom (Great Britain))

Design of Low-Cost Hardware Chaos-Based Image Cryptosystem
Marwan Ahmed Fetteha (Nile University, Egypt); Wafaa Sayed (Assistant Lecture, Egypt); Lobna Said (Nile University, Egypt)

A Hybrid Classical-Quantum Reinforcement Learning Agent for Real-Time Noise Suppression in Quantum Processors
Abdel Mehsen Ahmad (Lebanese International University, Lebanon); Awad Wehbe (LIU, Lebanon)

Explainable Machine Learning for Trip-Level Battery Stress Prediction in Electric Vehicles
Joe Farah (American University of Science & Technology, Lebanon); Mohamad Rahal (American University of Science and Technology, Lebanon)

Sunday, December 14 4:30 - 6:00 (Africa/Cairo)

Online2(A): Analog and RF Circuit Design Techniques

VirtualRoom-1

Chair: Abdallah Kassem (Notre Dame University, Lebanon)

A Power-Efficient, Fully-Adjustable, Bulk-Controlled, Linearized, Analog Integrated Gaussian Function Circuit for Kernel Functions

Daniela Papa, Emilios Georgiou, Theodoros Kantianis, Vasileios Moustakas and Vassilis Alimisis (National Technical University of Athens, Greece); Paul P Sotiriadis (National Technical University of Athens, Greece & Archimedes, Athena Research Center, Greece)

Low-Energy Real-Time Self-Organizing Classifier Architecture for Edge SNN Applications

Ugur Eroglu, Necati Teoman Bahar and Hasan Uluşan (Middle East Technical University, Turkey); Ali Muhtaroglu (Oslo Metropolitan University, Norway)

Digital SNN in 5 nm FinFET CMOS with Latency-Reducing Hybrid Spiking Scheme Operated at 2.6 GHz

Marcel Kossel (IBM, Switzerland); Giovanni Cherubini (IBM Zurich Research Laboratory, Switzerland); Matthias Braendli (IBM Research - Zurich, Switzerland); Victoria Miguel Gullón Alfonso, Stanisław Woźniak and Pier Andrea Francese (IBM Zurich, Switzerland); Jaewon Lee (Company, Switzerland); Thomas Morf (IBM Research - Zurich, Switzerland); Angeliki Pantazi (IBM Zurich Research Lab, Switzerland)

Analog Voltage-Shifter for 8-Bit Flash-SAR Hybrid Feed-Forward Architecture-Based ADC

Mohamed Amine Bensenouci (Polytechnique Montréal, Canada); Naim Ben-Hamida (Ciena, Canada); Ahmad Hassan (Polytechnique Montreal, Canada); Mohamad Sawan (Westlake University, China & Polytechnique Montréal, Canada); Yvon Savaria (École Polytechnique de Montréal, Canada)

A Six-Channel Dual-Mode Switched-Capacitor Capacitance-to-Voltage Converter for MEMS Gyroscopes

Omar Zabalawy, Sameh Ibrahim and Hesham Omran (Ain Shams University, Egypt)

An X Band GaN MMIC Power Amplifier Harnessing the Effect of Nonlinear Output Capacitance in CCE Mode

Yericharla Mary Asha Latha (IIT (ISM) Dhanbad, India)

Sunday, December 14 4:30 - 6:00 (Africa/Cairo)

Online2(B): Neuromorphic, In-Memory-and-Dataflow-Driven-Architectures-for-Next-Generation-AI

Room: VirtualRomm-2

Chair: Vassilis Alimisis (National Technical University of Athens, Greece)

Research on Key Technologies of EDA Software Based on RTL Code and AI Guidance

Dan Liu, Zhe Zhang, Junhao Wang and Junhao Li (Beijing Tango Software Technology Company, China)

End-to-End Transformer Acceleration Through Processing-in-Memory Architectures

Xiaoxuan Yang and Peilin Chen (University of Virginia, USA); Tergel Molom-Ochir and Yiran Chen (Duke University, USA)

Dataflow-Driven Neuromorphic Architectures for Edge AI: Theory, Design, and Applications

Bokyung Kim and Parshva Mehta (Rutgers University, USA); Yiran Chen (Duke University, USA)

FERMI-ML: A Flexible and Resource-Efficient Memory-in-Situ SRAM Macro for TinyML Acceleration

Mukul Lokhande, Akash Sankhe, S. V. Jaya Chand and Shivangi Mishra (Indian Institute of Technology Indore, India); Santosh Kumar Vishvakarma (IIT, Indore, India)

3D Memristive in-Memory GAN for Automated Design of on-Glass Patch Antenna for Ku Band

Shilpa Pavithran (Kerala University of Digital Sciences Innovation and Technology, India); Sruthi P and Alex James (Digital University Kerala, India)

Low-Power CMOS Design of ReLU Activation Module for Neural Networks

Mohamed Ghoneim (Department of Electrical and Computer Engineering, University of Louisiana at Lafayette, LA, USA); Kasem Khalil (University of Mississippi, USA); Magdy A Bayoumi (University of Louisiana Lafayette, USA)

Sunday, December 14 4:30 - 6:00 (Africa/Cairo)

Online2(C): ICM-General-II

VirtualRoom-3

Chair: Mohamad Kassab (MAJKassab NET, Lebanon)

Circuit Order Reduction of Closed Loop DC/DC Battery Converter via Padé Approximants

Asmae Chakir (EMSI Casablanca, Morocco); Yassine Chakir (EMSI, Morocco); Mohamed Tabaa (EMSI Casablanca, Morocco); Hassan Safouhi (Campus Saint-Jean, University of Alberta, Canada)

Urban-Hybrid-CDQNet: A Unified Deep Learning Framework for Semantic Change Detection and Quantification in Urban Monitoring and Disaster Response

Israa El Rifahi, Hussein Nasrallah, Hadi Noureddine and Ahmad Kobeissi (Lebanese International University, Lebanon)

Lightweight Dual-Branch CRNN for Interference Classification in SATCOM

Abdallah Agamy (Military Technical College, Egypt); Mohamed Naguib (The Ohio State University, USA); Essam Abd Elwanees (Communications Engineering Military Technical College, USA); Alaa Eldin Rohiem (MTC, Egypt)

Mechanistic Optimization of RF-MEMS Capacitive Switches: Low-Roughness Material Stacks for Superior mm-Wave Reliability

Farid Khamoueitouli (Iran University of Science and Technology, Iran; Sabanci University, Istanbul, Türkiye); Parisa Enshaee (Iran University of Science and Technology, Tehran, Iran); Farid Sayar Irani and Mostafa Vafaei (Sabanci University, Istanbul, Türkiye); Zehra Çobandede (Sabanci University (SUNUM) Nanotechnology Research and Application Center, Istanbul, Türkiye); Javad Yavandhasani (Iran University of Science and Technology Tehran, Iran); Murat Kaya Yapici (Sabanci University, Istanbul, Türkiye; University of Washington-Seattle, WA, USA)

Embedded Characterization of MOS Gate-to-Substrate Capacitances Using Ring Oscillators

Paul Devoge (ST-Microelectronics, France); Noémie Couzi (Aix-Marseille University, France & STMicroelectronics, France); Hassen Aziza (Universite of Aix-Marseille, France); Franck Julien, Abderrezar Marzaki, Alexandre Malherbe, Arnaud Regnier and Stephan Niel (STMicroelectronics, France)

An Automated Smart Contract-Based Architecture for IoT Device Recruitment and Service Provisioning

Hussein Othman (Islamic University of Lebanon, Lebanon); Fatima Abdallah (Al-Maaref University, Lebanon); Mubarak Mohammad (Al Maaref University, Lebanon)

A Novel Transformerless AC-DC Power Supply for Integrated Circuits in Telecom Applications

Isaac Ogunmola, Sufiaan Riaz, Isabel Smith, Lucas Chan and Abir Ihsan (Ontario Tech U, Canada); Mohamed Youssef (Ontario Tech University, Canada)

Sunday, December 14 4:30 - 6:00 (Africa/Cairo)

Online2(D): ICM-General-III

VirtualRoom-4

Chair: Ahmed Madian (Nile University, Egypt)

A Reactive VNF Orchestrator with Explainable AI-Based Intrusion Detection in 5G Networks
Abdel Mehsen Ahmad (Lebanese International University, Lebanon); Ola Zein and Zeina Allaw (LIU, Lebanon); Asmaa Amer (ETIS, CY Cergy Paris Université, ENSEA, CNRS, France)

AI-Driven Real-Time Security for 5G/6G Network Slices Using Adaptive SDN
Abdel Mehsen Ahmad (Lebanese International University, Lebanon); Zeina Allaw and Ola Zein (LIU, Lebanon); Asmaa Amer (ETIS, CY Cergy Paris Université, ENSEA, CNRS, France)

Integrating One-Class Anomaly Detection and Ensemble Learning for Robust and Efficient IDS Design
Bashar S. Khassawneh and Faisal Alanazi (Amman Arab University, Jordan); Ayoub Alsarhan (Hashemite University, Jordan); Ghaith Jaradat (Amman Arab University, Jordan); Mahmoud Aljamal (Irbid National University, Jordan); Sami Aziz Alshammari (Northern Border University, Saudi Arabia)

LOEA: Leading One-Based Exact Adder for Resource-Efficient High-Performance Computing
Prateek Goyal (Indian Institute of Technology, Goa (IIT Goa) India, India); Sujit Kumar Sahoo (Indian Institute of Technology Goa, India)

Analog PI Synchronization Circuit Design for a Memristive Chua's Chaotic Oscillator
Ali Mazak (Yildiz Technical University, Turkey); Dorukhan Astekin (Işık University, Turkey); Fatih Adiguzel (Yildiz Technical University, Istanbul, Turkey)

Reliability Challenges and Aging Behavior in a TSV-Based 3D-Stacked DRAM I/O Interface
Raoul Saber (American University of Beirut & Silicon Cedars, Lebanon); Maria Mansour (IPACK Solutions, Lebanon); Jad G. Atallah (American University of Beirut, Lebanon)

Monday, December 15

Monday, December 15 9:00 - 10:00 (Africa/Cairo)

OC: Opening Ceremony (Pavillon-1)

Pavillon-1

Monday, December 15 10:00 - 10:30 (Africa/Cairo)

CF1: Golden Break

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Monday, December 15 10:30 - 11:30 (Africa/Cairo)

KeyNote#1: Practical Quantum Computing: The Status Quo

Prof. Ahmed El-Mahdy

Chairs: Prof. Ahmed Madian (NU)

Prof. Ahmed El-Mahdy is the dean of the ITCS school. He joined NU in February 2023. He got his BSc and MSc from Alexandria University and PhD from Manchester University, UK. Coming from a computing systems background, Prof El-Mahdy is now exploring making quantum computing usable in practice. His group is exploring Quantum-AI, dealing with quantum noise, developing 'self-healing' quantum memories, and doing practical quantum communications. He collaborates strongly with Waseda University Japan, UAEU, Emirates, and E-JUST, Egypt. Upon his undergraduate graduation, he achieved the best student award from the Faculty of Engineering, Alexandria University. He was also awarded the prestigious IBM faculty award for his work on the Cell processor. He has also won first prize in the Middle East in the MIT Arab Start-up Competition; he had a distinguished promotion to full professor from the Supreme Council of Universities. He was awarded the Tariq Abd El-Wareth Award for Outstanding Contribution to Innovation Pillar from Nile University. He has many issued US patents and publications. He is currently a member of the organization committee of the IEEE International Conference on Quantum Computing and Engineering, responsible for publicity for the Middle East and Africa.

Pavillon-1

While quantum computing is showing strong promise, there is dismay about its current practical capabilities. After giving a quick introduction to quantum computing, this talk aims to highlight existing promising approaches in quantum computing that are starting to demonstrate a quantum advantage. We start with the quantum principle and variational circuits. We will discuss their utility in solving the ground-level energy that is used in many applications in computational chemistry, as well as their use in quantum neural networks. We then move into quantum optimisation using adiabatic quantum annealing, and the newly more promising counterdiabatic quantum computing. We then move into provably secure quantum communication. We conclude with quantum ghost imaging, showing how picturing an object without seeing it results in better quality!

Monday, December 15 11:30 - 1:00 (Africa/Cairo)

S11(A): Analog and RF Circuit Design Techniques-I

Room: Pavillon-1

Chairs: Anwar Hasan Jarndal (United Arab Emirates, United Arab Emirates & University of Sharjah, United Arab Emirates), Raafat Lababidi (ENSTA Bretagne, Lebanon)

Linear Modeling of GaN Transistors Using Black Hole Optimization

Anwar Hasan Jarndal (United Arab Emirates, United Arab Emirates & University of Sharjah, United Arab Emirates)

AlPN/GaN HEMT with Enhanced Sensitivity for Biosensor Applications: A Materials and Simulation Driven Analysis

Husna Hamza (University of Sharjah, United Arab Emirates); Anwar Hasan Jarndal (United Arab Emirates, United Arab Emirates & University of Sharjah, United Arab Emirates); Eqab Almajali, Sohaib Majzoub, Soliman Mahmoud and Talal Bonny (University of Sharjah, United Arab Emirates)

A High Isolation on-off Keying CMOS Modulator for mm-Wave Applications

Mohamed Ahmed Taha (Egypt-Japan University of Science and Technology, Egypt); Marwa Mansour (Electronics Research Institute (ERI), Egypt); Haruichi Kanaya (Kyushu University, Japan); Adel Bedair (Egypt-Japan University of Science and Technology, Egypt); Ahmed Sayed Ahmed Abdelhamid Allam (Egypt-Japan University of Science and Technology (E-JUST), Egypt)

Self-Regulating Load Voltage in a CMOS Cross-Coupled Rectifier

Takahiro Fujita, Takahide Sato and Satomi Ogawa (University of Yamanashi, Japan)

A CMOS Image Sensor Low-Power Counter for Single-Slope ADC at 500MHz Clock Frequency and 14pJ/Conversion-Step Figure-of-Merit

Tonny Do (University of Oslo, Norway); Robert Johansson (Sony Europe Limited, Norway); Philipp Häfliger (University of Oslo, Norway)

DC-DC Converter Optimization Strategies for Improved Performance with Resistive Loads in Low-Power Applications

Salma Elakkad and Sameh Osama (The British University in Egypt, Egypt); Ayman Hassan Ismail (Ain Shams University, Egypt); Hani A. Ghali (British University in Egypt (BUE), Egypt)

Monday, December 15 11:30 - 1:00 (Africa/Cairo)

S11(B): SS: Applying AI for and on Hardware: Cross-Layer Approaches for Security and Efficiency

Room: Pavillon-2

Chairs: Falah Awwad (UAE University, United Arab Emirates), Hassan Nassar (Karlsruhe Institute of Technology, Germany)

A Polymorphic Encryption Framework for Cross-Silo and Cross-Device Distributed Learning

Rawan Amr Hagag (German University in Cairo, Egypt & Karlsruhe Institute of Technology, Germany); Hassan Nassar (Karlsruhe Institute of Technology, Germany); Joerg Henkel (KIT, Germany); Mohamed A. Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

FPGA-Based Artificial Intelligence Accelerator for on-Board Processing of Aerial Scenes

Omnia AbdElkarim Saad, Os (Egypt-Japan University of Science and Technology (E-JUST), Egypt); Rami Zewail (EJUST, Egypt); Koji Inoue (Kyushu University Japan, Japan); Sameh Sherif (Egypt-Japan University of Science and Technology (E-JUST), Egypt); Mohammed Sayed (Egypt-Japan University of Science and Technology, Egypt)

Applying AI for and on Hardware: Cross-Layer Approaches for Security and Efficiency

Hassan Nassar and Mohammed Bakr Sikal (Karlsruhe Institute of Technology, Germany); Daniel Biebert and Christian Hakert (TU Dortmund, Germany); Heba Khdr (Karlsruhe Institute of Technology, Germany); Michel Lang (LAMARR, Germany); Lena Schmid and Markus Pauly (TU Dortmund, Germany); Jeferson Gonzalez-Gomez (TEC, Costa Rica); Kuan-Hsun Chen (University of Tewente, The Netherlands); Jian-Jia Chen (TU Dortmund University, Germany); Joerg Henkel (Karlsruhe Institute of Technology, Germany)

Prototype Replay: Memory-Efficient Continual Learning via Class-Conditioned Centroids

Elham Serria (United Arab Emirates University); Mishal Fatima Minhas (United Arab Emirates University, United Arab Emirates); Falah Awwad (UAE University, United Arab Emirates)

A Tampering Attack on ASCON with Hardware Trojans

Islam Elsadek and Eslam Tawfik (The Ohio State University, USA)

AI-Based Parking Lot Management System Using Computer Vision

Abdallah Ahmed Hassan (The German University in Cairo, Egypt); Eman Azab (German University in Cairo, Egypt)

Monday, December 15 1:00 - 2:15 (Africa/Cairo)

LB1: Lunch Break

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Monday, December 15 2:15 - 4:15 (Africa/Cairo)

S12(A): Digital Systems

Room: Pavillon-1

Chair: Mohamed A. Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

Effective Partitioning Approaches for High Performance FPGA Routing

Timothy Martin, Ka Chuen Cheng, Gary Grewal and Shawki Areibi (University of Guelph, Canada)

GrammLLM: Grammar-Guided LLM Test Generation for Compiler Validation

Mostafa Hassan, Islam Ahmed, Mohamed Gamal Talaat, Mohanad Mohamed and Mohamed Sayed (Siemens DISW, Egypt)

Mitigation of Single Event Effects (SEEs) Through TMR Implementation in Multi-Core Processors with LLM-Assisted Assembly Code Generation

Aya Khaled Galal Mohammed, Zoya Ahmed, Otmane Ait Mohamed and Abdelwahab Hamou Lhadj (Concordia University, Canada)

Open-Source Hyperdimensional RISC-V Vector Processor with Radix-8 CORDIC-Based Nonlinear Encoding for Memory-Efficient Edge-AI

Marawan T Abdelhady (N-a, Egypt & Egypt-Japan University of Science and Technology, Egypt); Mohamed Abdelsalam (Cairo University, Egypt); Mahmoud Magdi Mansi (Si-Vision LLC, Egypt); Mohamed A. Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

Formal That "Floats" High: Formal Verification of Floating Point Arithmetic

Hansa Mohanty (Infineon Technologies India Private Limited, India); Vaisakh Naduvodi Viswambharan (Infineon Technologies Dresden GmbH & Co. KG, Germany); Deepak Narayan Gadde (Infineon Technologies Dresden GmbH Co. KG, Germany)

Efficient Pruning and Acceleration of Encoder-Based LLM Transformers on eFPGA

Omar Elayat, Vincent Gaudet and Mohammed Elmasry (University of Waterloo, Canada)

Quantization-Aware CNN for Channel Estimation in 5G on FPGA

Wegdan Mohammed (The German University in Cairo, Egypt); Mohamed A. Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

Hybrid Integration of RRAM and CMOS Circuits Using Open-Source 130-nm PDK

Maryam Mostafa Ebrahim Atia, Mohammad Alhawari and Mohammed Ismail (Wayne State University, USA)

Monday, December 15 2:15 - 4:15 (Africa/Cairo)

S12(B): SS: Advances-in-Neuromorphic and Energy-Efficient-Analog/Digital-Computing-Architectures

Room: Pavillon-2

Chairs: Vassilis Alimisis (National Technical University of Athens, Greece), Moustafa Nawito (IU Internationale Hochschule, Germany)

Resource-Efficient Convolutional Tsetlin Machine Accelerator for Real-Time Image Classification on FPGAs

Rashed Al Amin (University of Siegen, Germany); Viplav Vijay Patil (Institute for Embedded Systems, University of Siegen, Germany); Roman Obermaisser (University of Siegen, Germany)

A ΔT-Triggered Spiking Temperature Sensor for Neuromorphic and Edge Applications

Moustafa Nawito (IU Internationale Hochschule, Germany)

An Analog-Implemented Burst-Dependent Synaptic Plasticity Model for Hierarchical Neuromorphic Architectures

Vasileios Moustakas, Vassilis Alimisis, Anna Mylona and Francky Francky Catthoor (National Technical University of Athens, Greece); Paul P Sotiriadis (National Technical University of Athens, Greece & Archimedes, Athena Research Center, Greece)

Temporal Drift-Regularization and Hyperparameter Optimization for Phase-Change Memory-Based Neural Network Applications

Adnan Haidar, Ahmed M Abdelsamad and Hongliu Yang (Technische Universität Dresden, Germany); Vasileios Ntinas (Aalborg University, Denmark); Ronald Tetzlaff (Technische Universität Dresden, Germany)

Hardware Trojan Insertion and Detection in Chiplet-Based Architectures

Zeyd Rashed, Peter Abdelmalk, Omar Mohamed and Mark Waheeb (GUC, Egypt); Hassan Nassar (Karlsruhe Institute of Technology, Germany); Joerg Henkel (KIT, Germany); Mohamed A. Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

HORUS: Hash-Oriented Resilient Unforgeable Sensing - Tamper-Evident Sensor Telemetry on Edge Microclusters

Mohamed El-Hadedy (California State Polytechnic University Pomona, USA & University of Illinois at Urbana-Champaign, USA)

Design of a Low Power Leaky Integrate-and-Fire Neuron Circuit Using a Memristor Emulator

Amel Neifar (University of Sfax & ENIS, Tunisia); Imen Barraj (Prince Sattam Bin Abdulaziz University, Al-Kharj, Saudi Arabia)

A Neuromorphic FPGA-Based Architecture for Energy-Efficient Visual Recognition

Tianyang Li (Westlake Institute for Optoelectronics, China); Zhipeng Liao (Westlake University, China); Chengjun Zhang (Westlake Institute for Optoelectronics, China); Jie Yang and Mohamad Sawan (Westlake University, China)

Monday, December 15 4:15 - 5:45 (Africa/Cairo)

S13(A): Neuromorphic, In-Memory-and-Dataflow-Driven-Architectures-for-Next-Generation-AI

Room: Pavillon-1

Chair: Shady Agwa (The University of Edinburgh, United Kingdom (Great Britain))

DISCA: A Digital in-Memory Stochastic Computing Architecture Using a Compressed Bent-Pyramid Format

Shady Agwa (The University of Edinburgh, United Kingdom (Great Britain)); Yikang Shen (Queens University Belfast, United Kingdom (Great Britain)); Shiwei Wang (The University of Edinburgh, United Kingdom (Great Britain)); Themistoklis Prodromakis (University of Edinburgh, United Kingdom (Great Britain))

Hybrid Quantum Generative Adversarial Networks: A Technical Review of Implicit Quantum Models and Hybrid Optimization

Wael Badawy (Egyptain Russian University, Egypt)

A Streaming SNN Accelerator Exploiting Temporal-Spatial Sparsity for Automatic Modulation Classification

Kuilian Yang (King Abdullah University of Science and Technology, Saudi Arabia & KAUST, Saudi Arabia); Ahmed M. Eltawil and Khaled Nabil Salama (King Abdullah University of Science and Technology, Saudi Arabia)

Design of a 160-μW OOK Transmitter Utilizing the Quenching Principle for Super-Regenerative Transceivers

Sherif Saleh (Institute for Microsystem and Technology, Germany); Haytham Azmi (Electronics Research Institute, Egypt); Hattan F. Abutarboush (Taibah University & Communications and Electronics Engineering, Saudi Arabia)

A Framework of Hexadecimal Locking Mechanism Using 65nm CMOS Process

Bhaskar Lal Das and Alak Majumder (NIT Arunachal Pradesh, India)

Monday, December 15 4:15 - 5:45 (Africa/Cairo)

S23(B): AI/ML/DL and Control Systems

Room: Pavillon-2

Chairs: Vassilis Alimisis (National Technical University of Athens, Greece), Rayane El Sibai (Al Maaref University, Lebanon)

An Energy-Efficient Analog Hardware Artificial Neural Network Architecture for Obesity Classification

Andreas Papathanasiou, Anna Mylona and Vassilis Alimisis (National Technical University of Athens, Greece); Paul P Sotiriadis (National Technical University of Athens, Greece & Archimedes, Athena Research Center, Greece)

LiDAR Vs Camera in Robotic Disassembly: A Comparative Study of Safety and Perception in Human-Robot Collaboration

Soufiane Ameur (CCPS Laboratory, ENSAM, University of Hassan II Casablanca Morocco, Morocco); Kaouter Karboub (EMSI, Morocco); Mohamed Tabaa (EMSI Casablanca, Morocco); Mohamed Hamlich (Hassan II University, Morocco)

A Novel AI-Enabled Decision Support Framework for Smart Agrivoltaic Management

Rayane El Sibai and El Abed El Safadi (Al Maaref University, Lebanon)

Intelligent Control of a 7-Level Multilevel Inverter Using ANN and PI Controllers Implemented on DSP TMS320F28379D

Youness Hakam (Moroccan School of Engineering Sciences, Morocco); Sofia Lemssadak and Mohamed Tabaa (EMSI Casablanca, Morocco); Mourad Zegrari and Ait elmahjoub Abdelhafid (Université Hassan II Casablanca, Morocco)

Maximum Power Point Tracking for PV Systems Under Partial Shading Conditions Using Kalman Filter and DSP Control

Youness Hakam (Moroccan School of Engineering Sciences, Morocco); Mohamed Tabaa (EMSI Casablanca, Morocco); Abdellah Ailane (EMSI, Morocco)

Comparative Study of Deep Learning Models for Multi-Task Breast Cancer Detection in Ultrasound Imaging

Afaf Ridaoui and Aboubaker Abouelkacim (DELTA Laboratory, Morocco); Leila Bouchoua (Ensam Casablanca, Morocco); Loubna El Faquih (ENSAM Casablanca, University Hassan II, Morocco); Ghita Zaz (The National School of Arts and Crafts, Hassan II University, Morocco)

Monday, December 15 7:30 - 9:30 (Africa/Cairo)

GD: Gala Dinner

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Tuesday, December 16

Tuesday, December 16 9:00 - 10:00 (Africa/Cairo)

KeyNote#2: Advancing Monitoring Capabilities: The Role of Wearable Sensors in Advancing Healthcare, Environmental, and Marine Studies (Pavillon-1)

Prof. Khaled Nabil Salama, Professor, Electrical and Computer Engineering, King Abdullah University of Science and Technology

Professor Khaled Nabil Salama serves as a professor of Electrical and Computer engineering. He earned his bachelor's degree with honors from Cairo University in 1997 and later completed his master's and doctoral degrees at Stanford University in 2000 and 2005, respectively. His early academic career included a position as an assistant professor at Rensselaer Polytechnic Institute before joining KAUST in 2009, where he was the founding program chair for Electrical Engineering until 2011. He was the director of KAUST sensors initiative between 2016-2021. Professor Salama's research is highly interdisciplinary, focusing on the development of devices, circuits, systems, and algorithms to facilitate inexpensive analytical platforms for industrial, environmental, and biomedical applications. He has made significant contributions to the field of low-power mixed-signal circuits for intelligent sensors and integrated biosensors. His work also extends into VLSI architectures for bio-imaging and instrumentation. More recently, he has been involved in pioneering neuromorphic circuits aimed at emulating brain functions. His scholarly output includes over 400 papers and 48 patents.

Pavillon-1

Chair: Fouad El Haj Hassan (Al Maaref University, Lebanon)

This seminar examines the transformative impact of wearable sensor technologies across healthcare, environmental monitoring, and marine biology. In healthcare, these sensors enable continuous monitoring for enhanced patient care and disease management. Environmental applications range from real-time pollution monitoring to ecosystem management, while in marine biology, wearable sensors facilitate non-invasive studies of aquatic life. The discussion will highlight technological advancements in sensor miniaturization and energy efficiency, emphasizing the critical role of interdisciplinary collaboration in optimizing wearable technologies for diverse applications.

Tuesday, December 16 10:00 - 10:30 (Africa/Cairo)

CB2: Coffee Break

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Tuesday, December 16 10:30 - 12:00 (Africa/Cairo)

S21(A): Analog and RF Circuit Design Techniques-II

Room: Pavillon-1

Chairs: Vassilis Alimisis (National Technical University of Athens, Greece), Waleed Madany (Institute of Science Tokyo, Egypt & Aswan University, Egypt)

A Fetal Monitoring IoT-Edge Cardiotocography System Based on Low-Power Analog Hardware Neural Network

Vassilis Alimisis, Anna Mylona, Andreas Papathanasiou and Vasileios Moustakas (National Technical University of Athens, Greece); Paul P Sotiriadis (National Technical University of Athens, Greece & Archimedes, Athena Research Center, Greece)

A Low-Power, Tunable Analog CMOS Implementation of the Swish Activation Function

Anna Mylona, Andreas Papathanasiou and Vassilis Alimisis (National Technical University of Athens, Greece); Paul P Sotiriadis (National Technical University of Athens, Greece & Archimedes, Athena Research Center, Greece)

FMCW Radar Chirp Linearity Requirements and Benchmarking Approach

Johan Holmstedt (Eindhoven University of Technology, The Netherlands); Paul T.m. Van Zeijl (Zelectronix BV, The Netherlands)

A Synthesizable Frequency Modulator Based on Digital PLL for Spread Spectrum Clock Generation

Waleed Madany (Institute of Science Tokyo, Egypt & Aswan University, Egypt)

Cracks Detection in Concrete Blocks Using Microwave Multi-Channel CSRR Sensors

Mohammed Bait-Suwailam (Communication and Information Research Center, Sultan Qaboos University, Oman & Dept. of ECE, Sultan Qaboos University, Oman); Awad Al-Shanfari (Communication and Information Research Center, Sultan Qaboos University, Oman); Abdullah Al-Saidy (Sultan Qaboos University, Oman)

A VSWR-Resilient X-Band CMOS Doherty Power Amplifier Using a Dual-Use Quadrature Hybrid in 22-nm FD-SOI

Mohamed K Hussein, Mohammed El-Nozahi, Hani Ragai and Mostafa Gamal Ahmed (Ain Shams University, Egypt)

Tuesday, December 16 10:30 - 12:00 (Africa/Cairo)

S21(B): Bioinformatics and Biomedical Smart Applications

Room: Pavillon-2

Chair: Khaled Nabil Salama (King Abdullah University of Science and Technology, Saudi Arabia)

Enhancing Skin Lesion Segmentation and Classification via Feature Fusion of Convolutional Neural Network Backbones

Nariman Khalil (Suez University, Egypt); Ahmed Madian (Nile University, Egypt); Ahmed Madian (NCRRT & Egyptian Atomic Energy Authority, Egypt)

Novel Integrated CMOS Capacitive Sensor for Nano-Microfluidics Systems

Abdulrahman Alghamdi (King Saud University, Saudi Arabia)

ATC-WAFNet: An Enhanced ATCNet with Window Attention Fusion for EEG Motor Imagery Classification

Youssef Abdelrahman Ahmed Abdelrazek (The German University in Cairo (GUC), Egypt); Shereen Afifi (German University in Cairo, Egypt); Mohammed A.-Megeed Salem (German University in Cairo & Ain Shams University, Egypt); Mohamed A. Abd El Ghany (German University in Cairo & TU Darmstadt, Egypt)

A Compact Potentiostat Architecture for Amperometric Biosensors

Ibrahim Alkhalifa and Lavita Rizalputri (King Abdullah University of Science and Technology (KAUST), Saudi Arabia); Saptami Suresh Shetty (King Abdulla University of Science and Technology, Saudi Arabia); Mario Soto Martinez (King Abdullah University of Science and Technology, Saudi Arabia); Mohamad Sawan (Westlake University, China); Khaled Nabil Salama (King Abdullah University of Science and Technology, Saudi Arabia)

DistillSort: Distilling Autoencoders for Efficient Spike Sorting in Intracortical Brain-Computer Interfaces

Mohammad Mansour and Ameer Abdelhadi (McMaster University, Canada)

Ultrasound in Early Breast Cancer Detection: A Review of Conventional Methods and Emerging Innovations

Leila Bouchoua (Ensam Casablanca, Morocco); Ghita Zaz (The National School of Arts and Crafts, Hassan II University, Morocco); Loubna El Faquih (ENSAM Casablanca, University Hassan II, Morocco); Afaf Ridaoui and Aboubaker Abouelkacim (DELTA Laboratory, Morocco)

Tuesday, December 16 12:00 - 1:30 (Africa/Cairo)

S22(A): Smart Applications and New Trends for a Connected Industry of the Future

Room: Pavillon-1

Chair: El Abed El Safadi (Al Maaref University, Lebanon)

An Integrated AI-Driven System for Real-Time PPE Compliance and Safety Monitoring in Smart Laboratories

Mubarak Mohammad, Mohammad Rhayem, Ali Rhayem, Mohammad Jawad El Sayed and El Abed El Safadi (Al Maaref University, Lebanon)

Cost-Effective IoT Smart Metering Architecture with STM32 Microcontrollers for Sustainable Energy Management

Youness Hakam (Moroccan School of Engineering Sciences, Morocco); Mohamed Lamane (EMSI LPRI, Morocco); Mohamed Tabaa (EMSI Casablanca, Morocco)

Enhancing Microgrid Efficiency: Integrating MPPT with Droop Control for Optimal Power Sharing

Youness Hakam (Moroccan School of Engineering Sciences, Morocco); Mohamed Tabaa (EMSI Casablanca, Morocco)

Negative Group Delay Predictor Application for CO2 Gas Concentration in Real Environment Condition

Jonas Pellegrino (Aix Marseille University, France); Hassen Aziza (Universite of Aix-Marseille, France); Mathieu Guerin and Pascal Taranto (Aix Marseille University, France)

Brownian Feature Trajectories with Geometric Decision Boundaries for Edge Anomaly Detection

Redwane Ait-Ouammi (University of Technology of Troyes, France & Artifeel Company, France); Hichem Snoussi and Ahmad Bitar (University of Technology of Troyes, France); Alain Staron (Artifeel Company, Paris, France)

Large Language Model-Based Hierarchical Framework for Emerging Trends in Extreme Ultraviolet Research

Sung Tae Yoo and Seonho Kim (Korea Institute of Science and Technology Information, Korea (South)); Jae-Min Lee (Korea Institute of Science and Technology Information)

Tuesday, December 16 12:00 - 1:30 (Africa/Cairo)

S22(B): ASIC/FPGA/SoC/3D Circuits

Room: Pavillon-2

Chair: Mohamed Tabaa (EMSI Casablanca, Morocco)

Digital Baseband Architecture and Control Logic for Sub-GHz Mixed-Signal TR-PPM Transmitter ASIC

Syed Usman U Amin (University of Milano-Bicocca, Italy & University of Pavia, Italy); Andrea Baschirotto (University of Milano Bicocca, Italy)

Fast and Resource-Aware Implementation of Recurrent Neural Network Accelerators on FPGAs

Tom Xaviour and Xiaofang Wang (Villanova University, USA)

AI/ML Based Prediction of FPGA Synthesis Features from RTLs

Ahmed Gasser (German University in Cairo, Egypt); Amr Hegazy (German University in Cairo, Egypt & Technical University of Munich, Germany); Adam Adham, Mohamed Wael, Omar ElHarridy and Seif Tarek (German University in Cairo, Egypt); Hala Ibrahim and Reem Sameh (Siemens, Egypt); Milad Ghantous (The German University in Cairo, Egypt)

TCAD Evaluation of Spacer Length in SoC I/O FinFETs

Zih Fei Chen (National Cheng Kung University, Taiwan); Yu Sheng Lai (Taiwan Semiconductor Research Institute, Taiwan); Meng-Hsueh Chiang (National Cheng Kung University, Taiwan)

FPGA-Optimized CNN Architecture for Automatic Modulation Classification

Kamal A. Mohamed, Michael B. Abdullah, Sara S. Kolta and Seif Eldin A. Hassan (Engineering, Egypt); Ratshih Sayed (Electronics Research Institute); H. H. Draz (ERI, Egypt); Haytham Azmi (Electronics Research Institute, Egypt)

Causal-Bayesian Modeling for Risk-Aware Resilience in Industrial Cyber-Physical Systems

Youness Ghazi (Université Hassan II de Casablanca, Morocco & EMSI, Morocco); Ghita Zaz (The National School of Arts and Crafts, Hassan II University, Morocco); Mohamed Tabaa (EMSI Casablanca, Morocco); Mohamed Ennaji (he National School of Arts and Crafts, Hassan II University, Morocco)

Tuesday, December 16 1:30 - 2:30 (Africa/Cairo)

LB2: Lunch Break

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Tuesday, December 16 2:30 - 3:00 (Africa/Cairo)

CC: Closing Ceremony

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Tuesday, December 16 4:00 - 7:30 (Africa/Cairo)

TR: Tour in Old Cairo (AZHAR, HUSSEIN and KHAN ELKHALILI)

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

Wednesday, December 17

Wednesday, December 17 9:00 - 1:00 (Africa/Cairo)

MS: Visit to Grand Egyptian Museum

Pavillon-1, Pavillon-2, VirtualRomm-2, VirtualRoom-1, VirtualRoom-4, VirtualRoom-3

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