IN1020 - oblig 1

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1 Report

I solved this assignment pragmatically, almost blindly. First by adding inputs and outputs in logisim, needing to know which gates to use between them I made a truth table which was then used to create k-maps for each output, then implemented the simplified terms from the k-maps into logic gates, wire everything nicely and, done before you know.

Most of the logic was quite easy to implement, except for the 'd' output. Adding to the complexity was a lot of typos in the groupings (the group labels outside the k-map, I mixed them up). I started the assignment in the middle of the night while on the phone with a long distance friend so typos was pretty much inevitable. Had to redo all the simplified terms multiple times because of mix up in k-map groups, the inputs are x3, x2, x1,and x0, and I mixed up where x3 and x2 were in the k-map, same with x1 and x0. (turned out i had it correct the first time and early morning me was just an idiot). Anyway, I thought the 'd' k-map was maybe just an xnor with inverted corners, but that was an incorrect approach. It was much easier to group the two middle lines as a group and separately group the two corners. For the specific logic on each output see figure description below.

For viewability the multiplier has been made into a sub-circuit along with the 'a', 'b', 'c', and 'd' logic; while the 'e', 'f', 'g', and 'h' logic are so trivial that they need no abstraction.

My implementation was made by calculating the correlating input and output values beforehand. But it is also possible to implement a general 4 by 4 bit multiplier and hard-wire one of the numbers to be 1010 (10 decimal). But since we've had truth tables and k-maps in lectures, it feels like this implementation is as valid. Also I could probably optimize further by reusing some gates, but I'm content by the way it is now.

In short it was a good assignment. It was fun toying around with logisim.

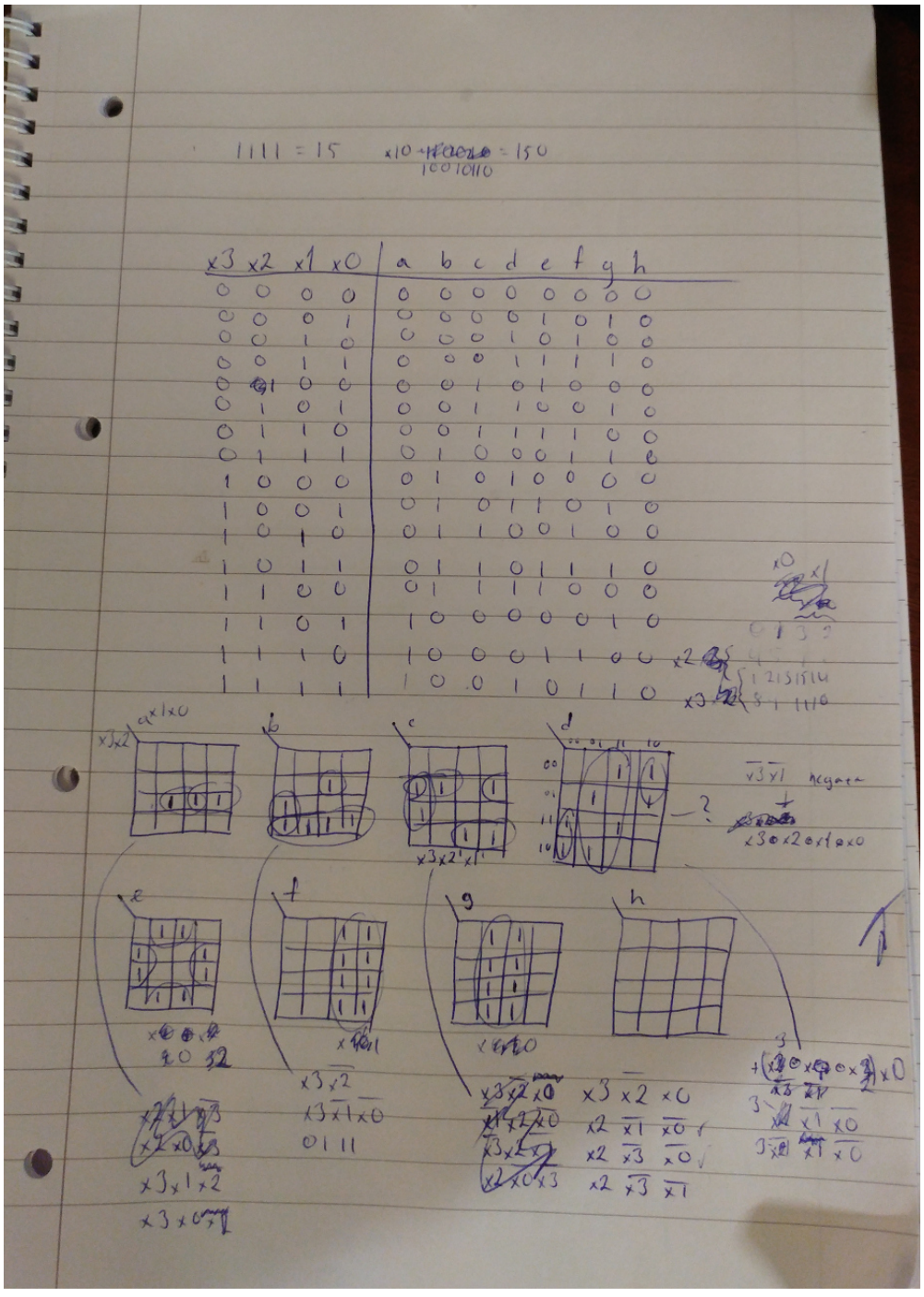

Figure 1: Sketch of the truth table and k-maps. Mislabels everywhere.

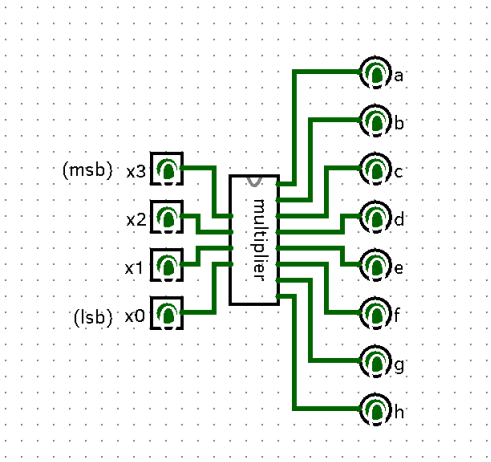

Figure 2: Main circuit

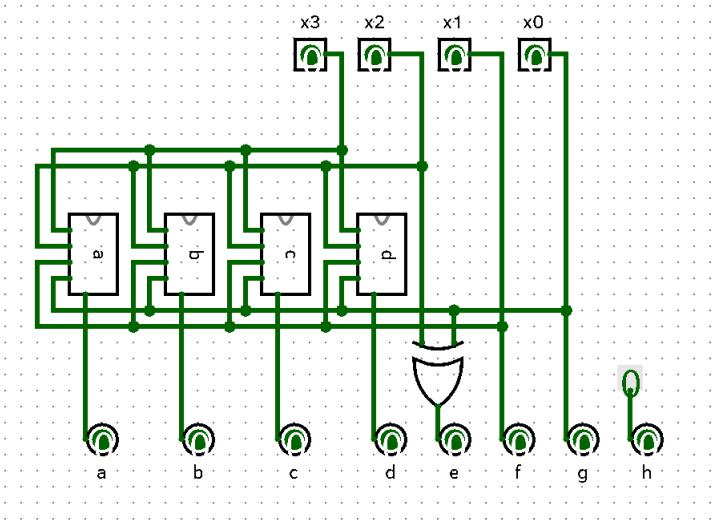

Figure 3: Multiplier circuit

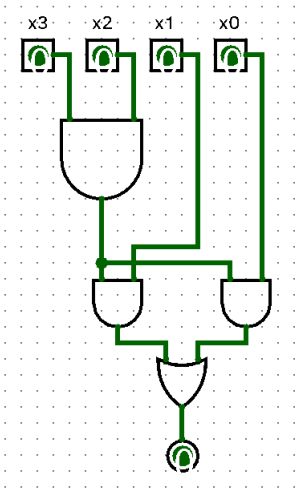

Figure 4: a circuit
`x3x2x1 + x3x2x0`

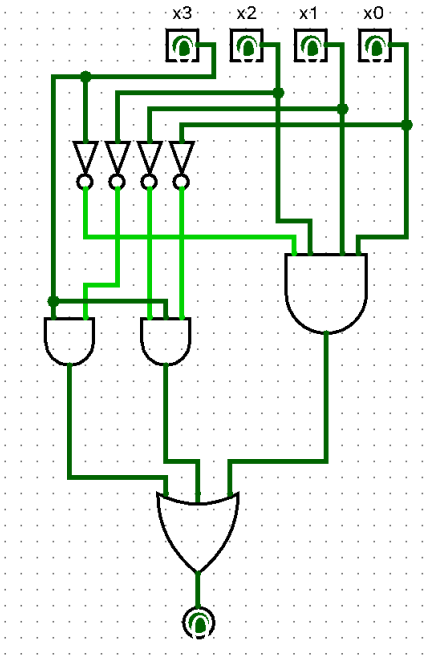

Figure 5: b circuit
`x3x2' + x3x1'x0' + x3'x2x1x0`

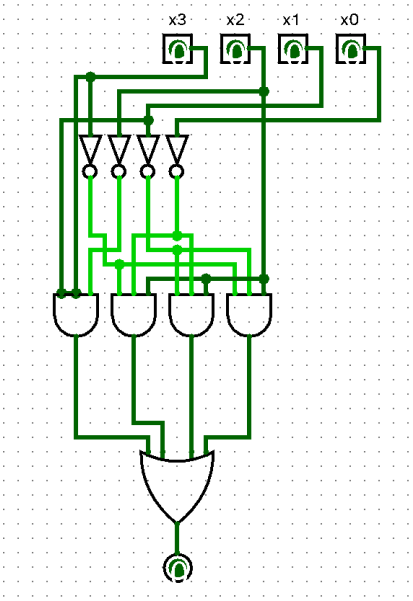

Figure 6: c circuit
`x3x2'x1' + x2x1'x0' + x3'x2x0 + x3'x2x1'`

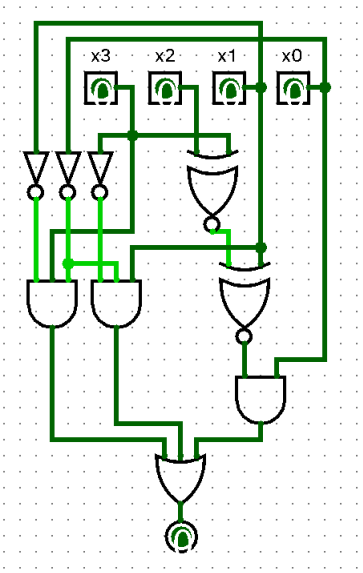

Figure 7: d circuit
`((x3⊕x2)'⊕x1)'x0 + x3x1'x0' + x3'x1x0'`