# Green SoCs for a Sustainable Internet-of-Things

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***Abstract*— The vision of the Internet-of-Things (IoT) calls for the deployment of trillions of wireless sensor nodes (WSNs) in our environment. A sustainable deployment of such a large number of electronic systems needs to be addressed with a Design-for-the-Environment approach. This requires minimizing 1) the embodied energy and carbon footprint of the WSN production, 2) the ecotoxicity of the WSN e-waste, and 3) the Internet traffic associated to the generated data. In this paper, we study how ultra-low-power yet high-performance systems-on-a-chip (SoCs) in nanometer CMOS technologies can contribute to these objectives by allowing compact batteryless WSNs with on-node data processing. We then review latest results achieved at the Université catholique de Louvain in the field of green SoC design for a massive yet sustainable deployment of the IoT.**

## I. Introduction

The Internet-of-Things (IoT) targets the development of ambient intelligence with wireless sensor nodes (WSNs) attached to every objects [1]. Such WSNs require unique identification as well as sensing and computing capabilities with memories, energy management and wireless communication to allow interactions with the cloud. The IoT will enable new exciting applications in fields such as energy savings, home automation, transportation, industrial production, logistics, healthcare, entertainment and security [1]. Regarding the climate change that the world is facing and the necessity to reduce carbon dioxide emissions, the IoT could significantly contribute by improving the energy and resource efficiency in several key applications: smart grid, smart buildings, smart cities and smart supply chains. However, the IoT vision calls for the deployment of up to trillions of connected WSNs [2] with millions of terabytes of traffic generated annually by machine-to-machine (M2M) communications. This may also trigger sustainability concerns: an increase of the electricity consumption of the ICT infrastructure (datacenters and network equipment) to handle the generated data, a significant carbon footprint for the high-volume production of WSNs and an increased level of electronic waste.

In this paper, we study how IC design can contribute to mitigate these effects in a Design-for-the-Environment (DfE) approach. In Section II, we give a preliminary look at the IoT impact on the environment, and derive design targets for *green systems-on-a-chip (SoCs)* targeting a sustainable development of the IoT. We then review an example of such a green SoC in Section III: the SleepWalker SoC [3]. Finally, further performance improvements of green SoCs are reviewed in Section IV based on circuit design and technology scaling.

## II. Environmental impact of the IoT

The environmental impact of a system can generally be evaluated bottom-up by carrying out a life-cycle assessment (LCA) of all its components. The idea is to systematically assess every phase of their life cycle from cradle to grave: material extraction, fabrication and assembly processes, transportation, use and end-of-life (disposal or recycling). For complex systems such as large-scale communication networks, this can be a very difficult task [4] and alternative top-down approaches are sometimes preferred [5]. The IoT is no exception: performing a full LCA would require addressing the wide variety of heterogeneous components (datacenters, wired network infrastructure, cellular base stations, local gateways and WSNs), communication protocols and usage scenarios. As most of these components are already in use for the Internet as we know it today, existing environmental studies can be re-used for the IoT as a first approximation, albeit with an update of the numbers for the data traffic. Let us focus on the new components that will enable the rise of the IoT: the WSNs of the connected things.

Several studies exist on the LCA of generic semiconductor products [6], [7]. They report that the electrical power consumption during the use phase usually dominates their environmental impact. However, we recently showed that the life-cycle energy demand of baseline WSN chips is dominated by IC production [8], as illustrated in Fig. 1. This is due on one hand to their very low power consumption thanks to low computation and memory requirements coupled with a low activity duty cycle [8], and on the other hand to the high embodied energy in modern CMOS chips required by high-precision process steps and high-purity chemicals [7].

To evaluate the carbon footprint of the WSN deployment for the IoT, we look at the individual footprint of the components we may find in baseline commercial WSNs such as [9]: off-the-shelf ICs typically in $0.18/0.13\mu m$ CMOS technologies (microcontroller, radio, sensors) for a total silicon area around $\sim 20mm^2$, a small printed circuit board ($\sim 25cm^2$), two AA batteries and some off-chip components (passives and connectors). Let us focus on the carbon foot-

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TABLE I

PROPOSED ROADMAP FOR REDUCING THE CARBON FOOTPRINT OF WSN PRODUCTION.

| WSN improvement | IC design challenges | Estimated GWP $[CO_2e]$ (1000 units) |
|---|---|---|
| Baseline | — (off-the-shelf ICs with PCB assembly, running on AA batteries) | $\sim$ 800 kg |
| No battery | Ultra-low-power ICs with energy harvesting supply | $\sim$ 705 kg |
| No PCB | Cubic-millimeter 3-D SiP assembly | $\sim$ 500 kg |
| Low die area | Heterogeneous SoC integration in nanometer CMOS technology | $\sim$ 200 kg |

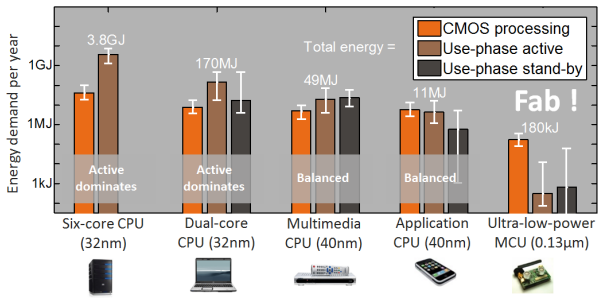


Fig. 1. Life-cycle energy demand of microprocessors for various application domains [8]. In high-performance applications, the energy demand is totally dominated by the electrical power consumption in active mode. In ultra-low-power applications the production of the CMOS IC dominates.

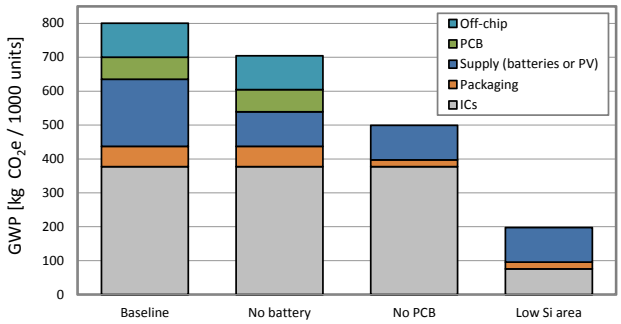


Fig. 2. Carbon footprint breakdown of WSN production for the roadmap proposed in Table I. The estimated footprint is expressed in the conventional unit $CO_2e$ of global-warming potential (GWP).

print for WSN production[1]. We carried out a review of the scientific LCA literature for these components to generate a preliminary carbon footprint model for WSN production. The model gives 800 kg $CO_2e$ for 1000 units, with the breakdown represented in Fig. 2. This represents $\sim$8% of the average annual footprint of a European citizen[2]. Such a high footprint would not be acceptable as the world is now facing the critical challenge to limit its carbon emissions.

For a massive yet sustainable deployment of WSNs, this footprint needs to be reduced. A possible roadmap is proposed in Table I. We first need to get rid of the batteries by operating the node on an energy-harvesting basis for example with a tiny photovoltaic (PV) cell ($\sim 1cm^2$) and a small energy storage device (thin-film battery or supercapacitor). The absence of AA batteries only saves $\sim$15% of the production carbon footprint but will limit the ecotoxicity of the e-waste. This requires significantly reducing the average power consumption of the ICs below 10 $\mu W$ [10]. We may further save by getting rid of the off-chip components and by using a 3-D system-in-package (SiP) with a PCB-less cubic-millimeter form factor [11]. As shown in Fig. 2, the footprint at this stage is largely dominated by the IC production. The last step would thus be to port all functions (microcontroller, radio, sensors) into a single SoC using a nanometer CMOS technology (65/40nm) to significantly reduce the silicon area. With an estimated area of $\sim 4mm^2$, the total expected savings in carbon footprint compared to the baseline WSN is a factor 4$\times$. Two DfE targets thus appear: low silicon area and low average power as it will affect proportionally PV cell sizing.

In addition to WSN production and e-waste, another impact of the IoT comes from the data that will be generated by the WSNs. Indeed, this data will be sent to the cloud for processing and/or archiving and this will consume electrical power for the supporting ICT infrastructure (datacenters, wired and cellular network equipment, local gateways). The worldwide carbon footprint for this was estimated to represent about 2% (830 MT $CO_2$e) of the total emissions from human activity in 2007 and this number is predicted to reach 6% (1430 MT $CO_2$e) by 2020 [12]. The ICT footprint is largely dominated by the use-phase electrical power with half of it coming from the datacenters and the network equipment. This needs to be put into perspective with the fast increase of the Internet data traffic, particularly in mobile wireless communications [13]. The IoT will contribute to this traffic increase as the volume of M2M communications is predicted to rise by a factor 24$\times$ between 2012 and 2017 to reach up to 6.7 millions of terabytes per year in 2017, corresponding to 5% of the total mobile traffic [13].

In order to limit their contribution to this traffic increase, the IoT WSNs need to be capable of locally processing their data for limiting the generated traffic to only relevant information. This can be done through several schemes such as compressive sensing, compression/entropy coding, feature extraction and classification [14]. Eventually, the goal is to provide sufficient (distributed) intelligence to WSNs to allow them to take their own decisions locally. This requires embedding sufficient processing capabilities and memory capacity to the nodes in opposition to baseline WSN designs, which leads to a clear trade-off in green SoC design between ultra-low area and power on one hand and high computing performances on the other.

## III. GREEN SOCS AND THE SLEEPWALKER EXAMPLE

Based on the observations from previous section, we define green SoCs for the IoT as:

*Batteryless/ultra-low-power single-chip solutions enabling high computing performance at low die area.*

[1]The energy consumed during the use phase of battery-powered devices is accounted for by the production footprint of the batteries.

[2]Estimated at 9.8 T $CO_2$e per capita in 2010 (Emission Database for Global Atmospheric Research, *http://edgar.jrc.ec.europa.eu*, v4.2, 2011).

TABLE II

COMPARISON OF MSP430 MICROCONTROLLER SOCS

| Reference | TI, ISSCC, 2011 | MIT, JSSC, 2009 | UCL, JSSC, 2013 |
|---|---|---|---|
| Technology | 0.13$\mu$m CMOS LP + FeRAM | 65nm CMOS LP | 65nm CMOS LP/GP |
| Die area [mm$^2$] | 4.4 (total) | 1.62 (core) / 4.26 (total) | 0.42 (core) / 0.66 (total) |
| External supply | 2.0-3.6V | 1.2V | 1-1.2V |
| Internal $V_{dd}$ | N/C | 0.5V | 0.32-0.48V (AVS) |
| Speed performance | 24 MHz | 0.3 MHz | 25 MHz |
| SoC active power | 164-130 $\mu$W/MHz | 27.3 $\mu$W/MHz | 7.0 $\mu$W/MHz |
| SoC stand-by power | <6 $\mu$W @85°C | <1 $\mu$W @25°C | 1.7 $\mu$W @25°C |
| GWP for IC production **(1000 units)** | 83 kg $CO_2$e | 47 kg $CO_2$e | 14 kg $CO_2$e |

To build such green SoCs, we may exploit the high density of nanometer technologies with the versatility of modern CMOS processes to operate logic at ultra-low-voltage (ULV) (0.3-0.5V) for ultra-low average power while keeping reasonable speed performance in the near-threshold regime. Designing robust and energy-efficient ULV SoCs in 65/45nm CMOS at MHz-range clock frequencies requires overcoming the following challenges [15]: high stand-by power due to leakage currents, large cycle time guardband to accommodate low-temperature operation, poor yield due to degraded logic noise margins and variability-induced clock skew. Moreover, ULV supply needs to be generated on-chip with an embedded DC/DC converter [16], [17].

A microcontroller SoC codenamed SleepWalker [3] was designed to address these pitfalls while being compatible with the MSP430 instruction set and operating at the 25-MHz speed of its off-the-shelf counterpart. It fully exploits a dual-core-oxide 65nm CMOS process with both Low-Power (LP) and General-Purpose (GP) MOSFETs co-integrated to 1) operate the CPU and most of the logic at ULV in GP while meeting the 25-MHz timing constraint and 2) minimize stand-by power and die area with a dense 1-V SRAM array. It also uses an on-chip adaptive voltage scaling (AVS) system to compensate for speed degradation at low temperature with power gating of the GP CPU in stand-by mode embedded into the AVS DC/DC converter. Standard-cell libraries with upsized gate length allows recovering the noise margins and a low variability clock tree avoids hold-time violations. Finally, a miniature ULV cache synthesized from standard cells with glitch-masking logic reduces the power overhead of the 1-V SRAM by limiting the number of accesses.

Measurement results summarized in Table II demonstrate 20× energy savings compared to best nominal-voltage industrial results at the same speed, and 4× savings compared to best ULV research results with a 50× speedup. The net die area reduction also saves on the carbon footprint and the cost of IC production. Let us now explore how to further improve this speed/area/energy performance trade-off of green SoCs.

## IV. IMPROVING GREEN-SOC PERFORMANCE

### A. ULV synthesis flow

Optimum ULV logic synthesis for area/energy efficiency under green-SoC timing constraints is a challenging design task as the supply voltage is not locked in opposition to nominal-voltage synthesis. Moreover, the selection of the standard-cell library in versatile 65/40nm CMOS menus was shown to be critical for energy efficiency [18]. Designers thus face the complex problem of finding the optimum solution that minimizes the energy while ensuring robust timing closure in a wide *(V,L,N)* design space [19] corresponding to supply voltage *(V)* and library *(L)* selection, as well as netlist *(N)* optimization produced by the synthesis tool. As shown in Fig. 3, a synthesis flow that jointly explores this *(V,L,N)* design space brings significant energy savings when the target frequency is above 1 MHz for high computing performances in green SoCs. This is due to the fact that at these target frequencies, the optimum lies in the near-threshold rather than in subthreshold region where critical path optimizations enable significant voltage scaling under timing constraints [19]. To find this *(V,L,N)* optimum, we proposed a fast synthesis flow ensuring robust timing closure [19]. It is based on a three-step synthesis and only requires a single library re-characterization at the ULV design point.

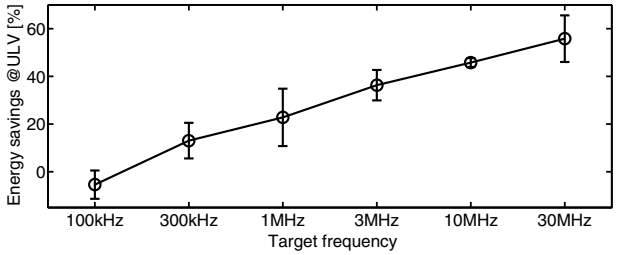


Fig. 3. A ULV synthesis flow that jointly optimizes the supply voltage, library and netlist [19] is capable of large energy savings when reaching the near-threshold regime with target frequencies above 1 MHz, compared to a baseline ULV flow with nominal voltage/library synthesis followed by a post-silicon voltage scaling down to the speed limit [19] (mean data and standard deviation over 10 *ITC*99 benchmarks in 65nm LP/GP CMOS).

### B. Hardware acceleration

Software execution of tasks on microcontrollers suffer from an energy penalty compared to hardware execution on ASICs. However, green SoCs for the IoT need software capability for control tasks, and the possibility of updating the firmware to avoid early technical obsolescence. In this context, the energy efficiency of specific tasks including data processing with arithmetic operations can be significantly improved by embedding hardware accelerators into the SoC [20]. At nominal voltage, the savings can be up to a factor 200× for individual operations and 10× for full data processing tasks, at the expense of larger die area.

When implemented at ULV, the accelerators for complex operations can suffer from long critical paths. In order to avoid limiting the system clock frequency of the whole SoC,

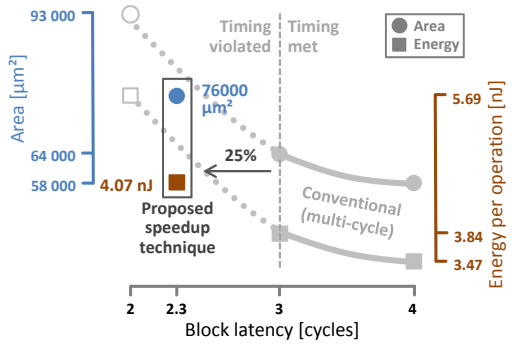


Fig. 4. The speed of multi-cycled hardware accelerators can be boosted by exploiting the data-dependent propagation delay at low area and energy costs [21] (synthesis results on a 32-bit multiply-and-divide unit at 0.35V with a cycle time of 20ns in 65nm GP CMOS).

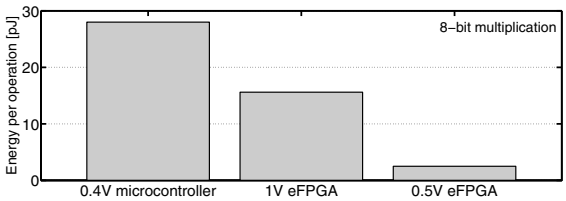


Fig. 5. Hardware acceleration on a ULV embedded FPGA can bring high energy savings for arithmetic operations compared to microcontroller execution [22] (measurements of the SleepWalker SoC and pre-layout simulations with a 4×4-tile eFPGA macro in 65nm LP/GP CMOS).

system architects can decide to operate them on a multi-cycle basis or to pipeline them at the cost of area and energy. We recently proposed another technique to exploit the data-dependent propagation delays in complex combinatorial blocks [21]. The idea is to monitor the propagation of data inside the block through the insertion of transition detectors at regular intervals along the paths. When input data does not activate the critical paths, the multi-cycled operation can be terminated in advance to decrease the average latency in the block. Results show in Fig. 4 that an average speedup of 25% can be achieved while relaxing the pressure on the critical path and thereby saving energy and area.

An alternative to dedicated hardware for the accelerators is to embedded an FPGA macro within the SoC (eFPGA) to preserve flexibility/reconfigurability for specific tasks [22]. By fully exploiting the versatility of LP/GP CMOS process for high-speed acceleration at low leakage, a ULV eFPGA is capable of energy savings up to 10× for specific operations as shown in Fig. 5 [22].

### C. CMOS technology scaling

The minimum energy $E_{min}$ level of ULV logic in 65/40nm bulk technologies is above the level of 90nm due to a degradation of subthreshold swing, drain-induced barrier lowering (DIBL) effect, gate leakage and within-die $V_t$ variability [23]. Fig. 6 shows a how small gate length ($L_g$) upsize contributes to keep this the $E_{min}$ under control, thereby making 65/40nm nodes a good choice for green SoCs [23], with a GP CMOS process for speed concern [18]. The $E_{min}$ level can further be improved by using an FD SOI technology [24]. In 28nm FDSOI with an LP CMOS process, LVT MOSFETs needs to be used instead of RVT with forward back biasing (FBB) to recover speed at ULV [25]. Moreover, adaptive control of this

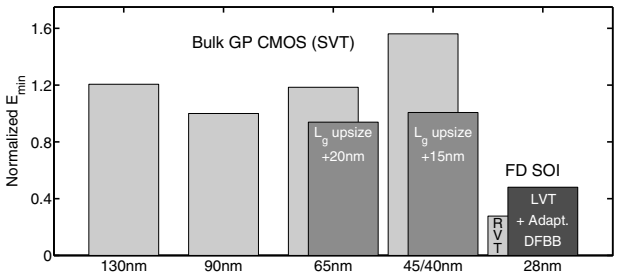


Fig. 6. The energy of ULV logic can be significantly improved at 28nm with FD SOI technology [24] and adaptive delta forward back biasing (DFBB) [25] (Monte-Carlo SPICE simulation results of an 8-bit multiplier at the minimum-energy point).

FBB must be applied to NMOS and PMOS independently for limiting noise margin degradations and thus maximizing the functional yield [25]. This is predicted to enable 200-MHz ULV SoC operation for demanding IoT applications.

## V. Conclusion

A sustainable development of the IoT requires addressing challenges related to the number of WSNs to be deployed and the high amount of data to be generated. In this paper, we gave a preliminary sight at the environmental impact of the IoT and explored how IC design can contribute to its sustainable development by minimizing the carbon footprint of WSN production and the ecotoxicity of the associated e-waste while enabling on-node data processing for limiting the Internet traffic. We proposed the green SoC definition in that sense i.e. *batteryless/ultra-low-power single-chip solutions enabling high computing performance at low die area.*

We showed through the recent SleepWalker example how ultra-low-voltage SoCs in 65/40nm CMOS can contribute to reach the green SoC targets and studied potential improvements based on efficient ULV logic synthesis, hardware acceleration and technology scaling to 28nm CMOS.

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