صاعق الناموس

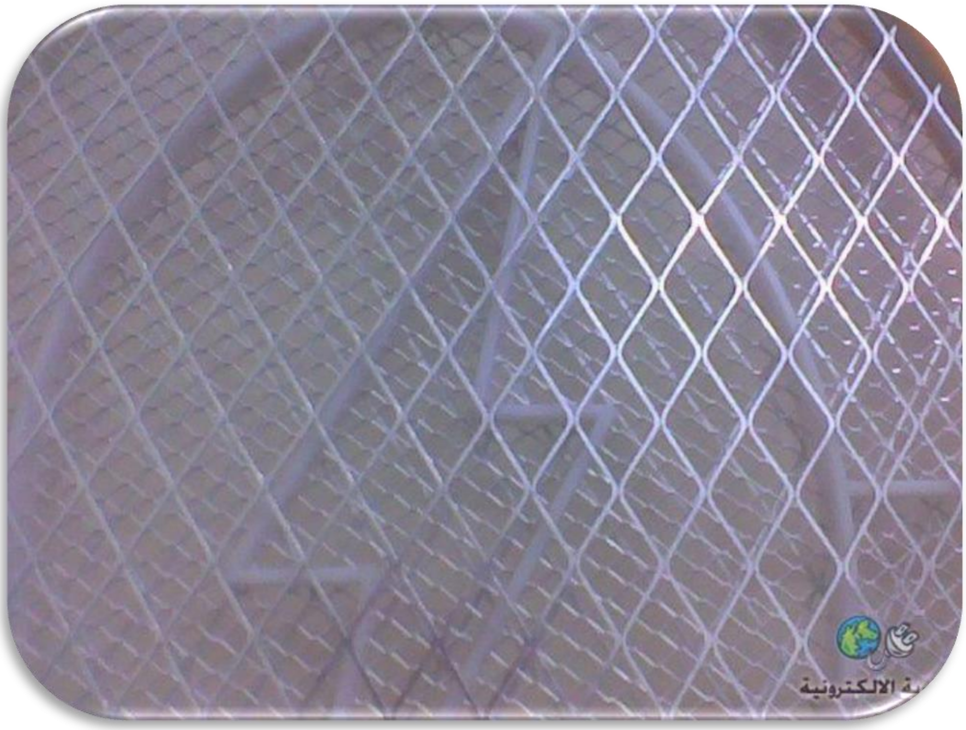
Outline

1- نظرة عامه.
2- الفكره الأساسيه والتطبيق.
3- الشرح المبسط.

1-التعريف

عبارة عن دائره تنتج جهد عالي بين 2000 الى 2500 فولت بشدة تيار ضعيفه جدا ودا كفيل انه يقتل أي حشره تلمس الشبكه.

الشبكة عباره عن شبكتين بينهم عازل يمنع تلامسهم كما بالصورة وكل شبكه عباره عن قطب من اقطاب الخرج



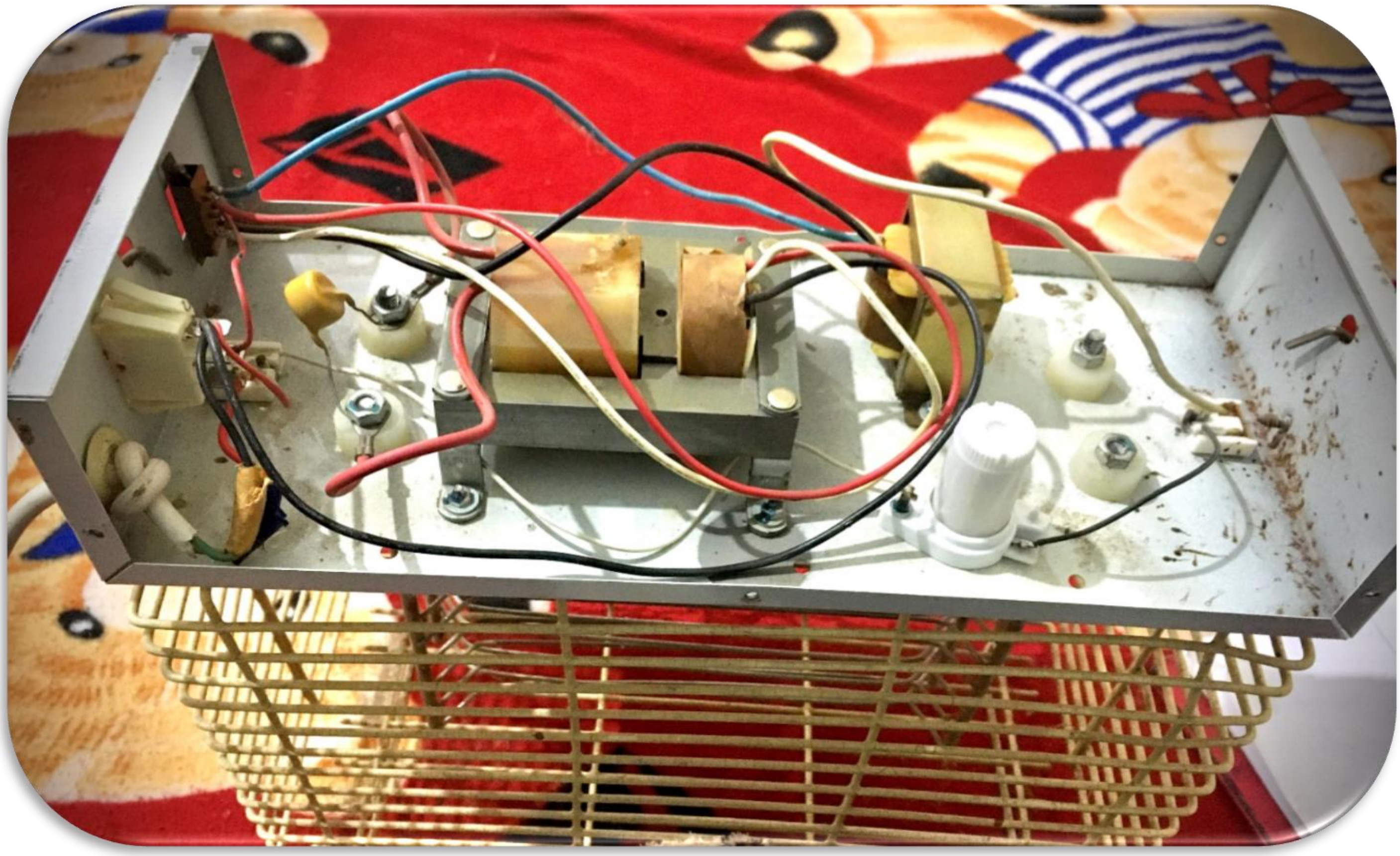
2- الفكرة الأساسية:

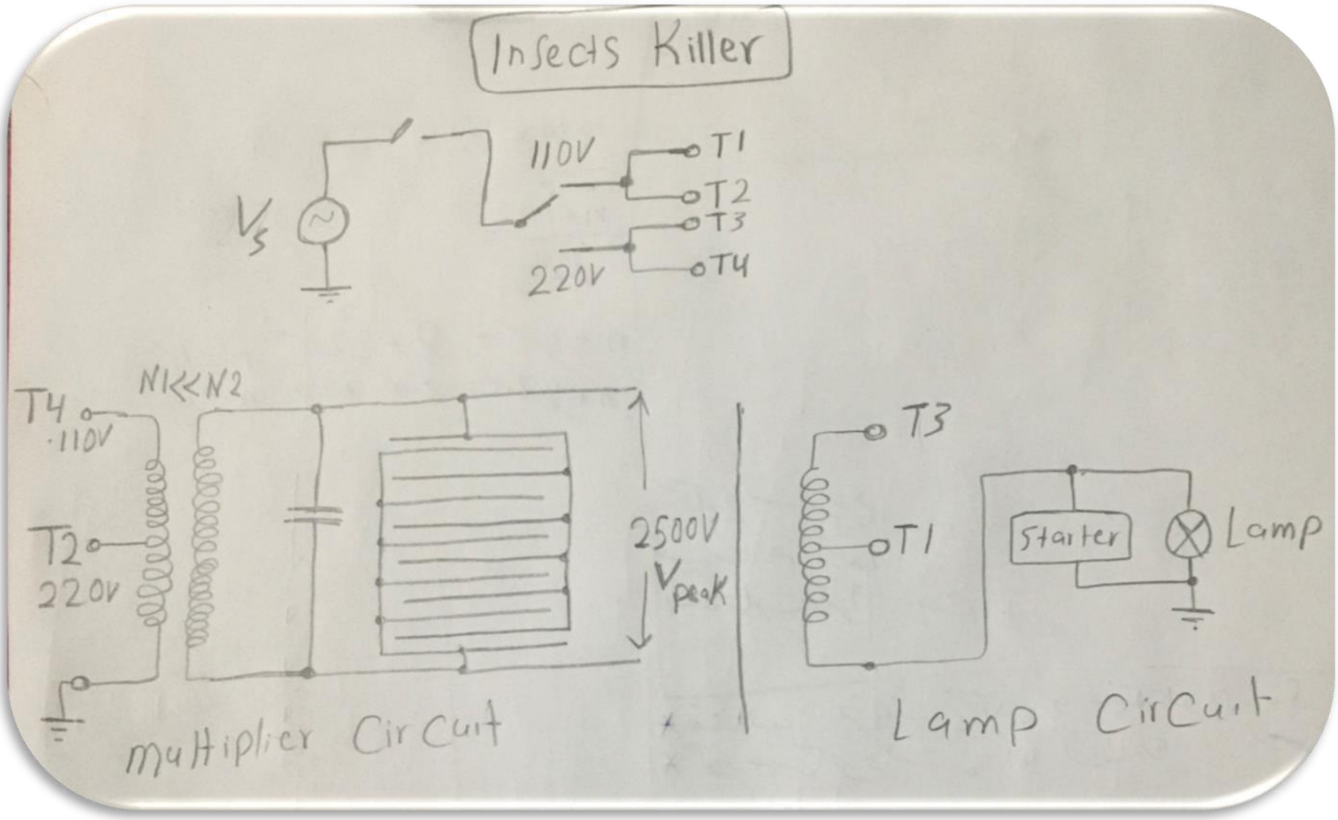
تضخيم الجهد من 220V إلى 2000 أو2500 فولت وطبعا تكبير الفولت بيجي على التيار فبيكون التيار ضعيف جدا ودي بتحمينا احنا لو اتكهربنا منه.

مبدأ التضخيم بطريقتين:

الطريقة القديمه: استخدام Transformer

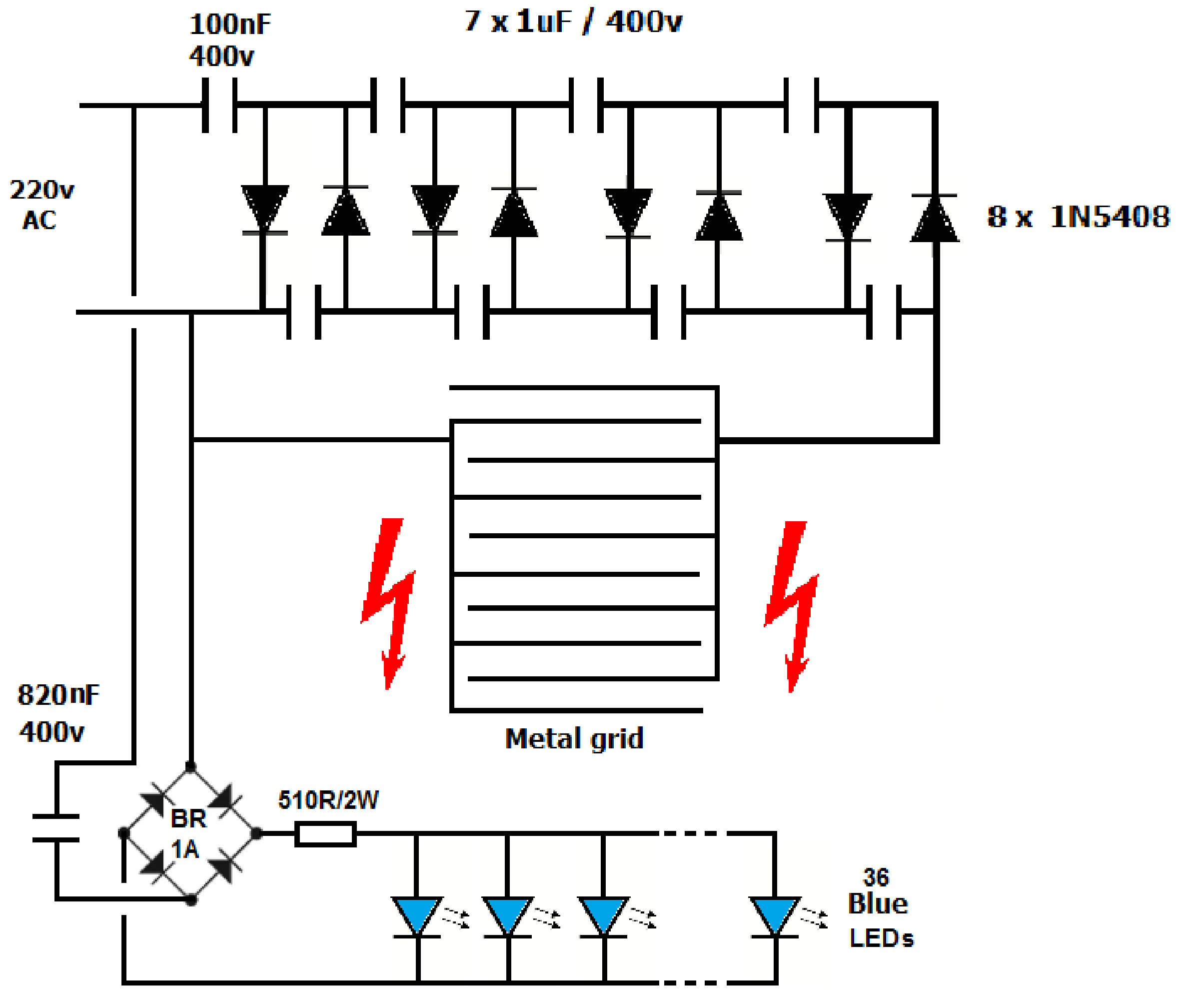
ودي مشكلته انه غالي جدا في السعر




Insects Killer
Vs
110V
T1
T2
T3
220V
T4
N1<<N2
T4
110V
T2
220V
2500V
Vpeak
multiplier Circuit
T3
T1
Starter
Lamp
Lamp Circuit

الطريقه الحاليه: استخدام دايرة Voltage Multiplier

ودي كويسه جدا من حيث التكلفه رخيصه جدا لاعتمادها على دايودات ومكثفات فقط



تعديل بسيط: المكثفات نختارها تستحمل 600 فولت لان كل مكثف بيشحن $2* V_{peak}$ فـ400 فولت ممكن هيتحرق.

الجهد الكلي = جهد المصدر(V_{peak}) * عدد مراحل

في الدائره السابقه 8 مراحل

الجهد الكلي = $220\sqrt{2}$ * 8 = 1760 فولت

Diode Clampers

A clamper adds a dc level to an ac voltage. **Clampers** are sometimes known as *dc restorers*. Figure 2–63 shows a diode clamper that inserts a positive dc level in the output waveform. The operation of this circuit can be seen by considering the first negative half-cycle of the input voltage. When the input voltage initially goes negative, the diode is forward-biased, allowing the capacitor to charge to near the peak of the input ($V_{p(in)} - 0.7$ V), as shown in Figure 2–63(a). Just after the negative peak, the diode is reverse-biased. This is because the cathode is held near $V_{p(in)} - 0.7$ V by the charge on the capacitor. The capacitor can only discharge through the high resistance of R_L. So, from the peak of one negative half-cycle to the next, the capacitor discharges very little. The amount that is discharged, of course, depends on the value of R_L.

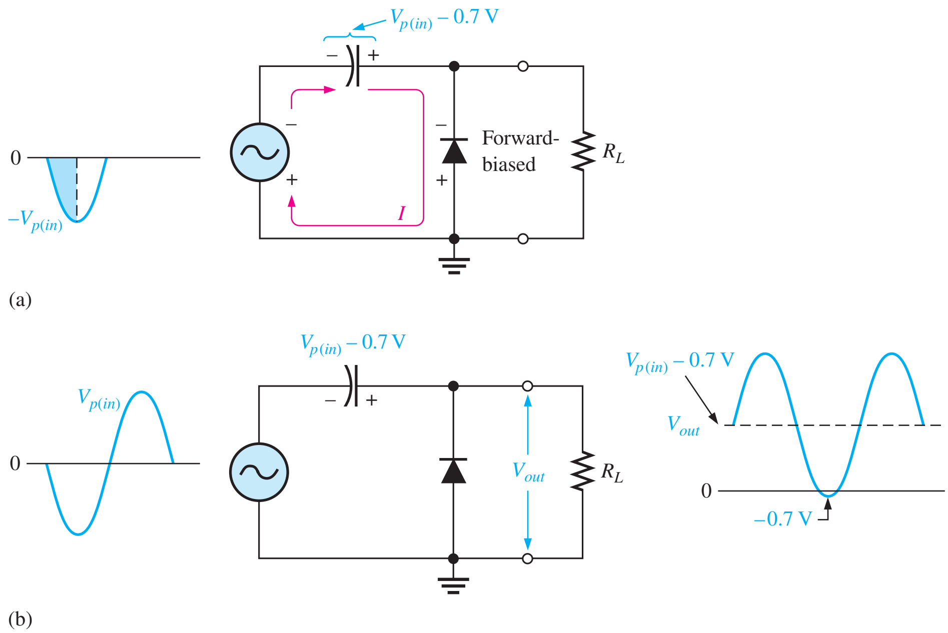


FIGURE 2–63

Positive clamper operation.

If the capacitor discharges during the period of the input wave, clamping action is affected. If the *RC* time constant is 100 times the period, the clamping action is excellent. An *RC* time constant of ten times the period will have a small amount of distortion at the ground level due to the charging current.

The net effect of the clamping action is that the capacitor retains a charge approximately equal to the peak value of the input less the diode drop. The capacitor voltage acts essentially as a battery in series with the input voltage. The dc voltage of the capacitor adds to the input voltage by superposition, as in Figure 2–63(b).

If the diode is turned around, a negative dc voltage is added to the input voltage to produce the output voltage as shown in Figure 2–64.

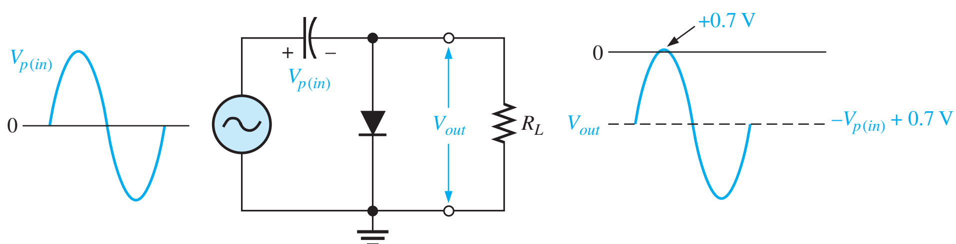


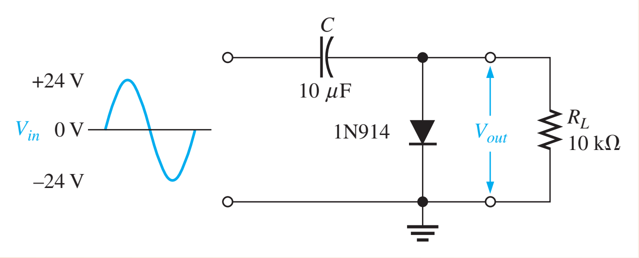
FIGURE 2–64

Negative clamper.

EXAMPLE 2–13

What is the output voltage that you would expect to observe across R_L in the clamping circuit of Figure 2–65? Assume that RC is large enough to prevent significant capacitor discharge.

▶ **FIGURE 2–65**



Solution

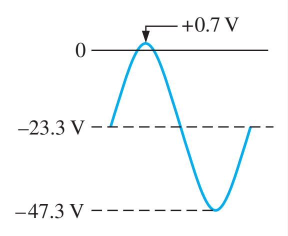
Ideally, a negative dc value equal to the input peak less the diode drop is inserted by the clamping circuit.

$$V_{DC} \cong -(V_{p(in)} - 0.7\text{ V}) = -(24\text{ V} - 0.7\text{ V}) = \mathbf{-23.3\text{ V}}$$

Actually, the capacitor will discharge slightly between peaks, and, as a result, the output voltage will have an average value of slightly less than that calculated above. The output waveform goes to approximately +0.7 V, as shown in Figure 2–66.

▶ **FIGURE 2–66**

Output waveform across R_L for Figure 2–65.



Related Problem

What is the output voltage that you would observe across R_L in Figure 2–65 for $C = 22\ \mu\text{F}$ and $R_L = 18\text{ k}\Omega$?

Open the Multisim file E02-13 in the Examples folder on the companion website. For the specified input, measure the output waveform. Compare with the waveform shown in the example.

SECTION 2–7 CHECKUP

1. Discuss how diode limiters and diode clampers differ in terms of their function.
2. What is the difference between a positive limiter and a negative limiter?
3. What is the maximum voltage across an unbiased positive silicon diode limiter during the positive alternation of the input voltage?
4. To limit the output voltage of a positive limiter to 5 V when a 10 V peak input is applied, what value must the bias voltage be?
5. What component in a clamping circuit effectively acts as a battery?

2–8 VOLTAGE MULTIPLIERS

Voltage multipliers use clamping action to increase peak rectified voltages without the necessity of increasing the transformer's voltage rating. Multiplication factors of two, three, and four are common. Voltage multipliers are used in high-voltage, low-current applications such as cathode-ray tubes (CRTs) and particle accelerators.

After completing this section, you should be able to

- **Explain and analyze the operation of diode voltage multipliers**
- Discuss voltage doublers
  - Explain the half-wave voltage doubler
  - Explain the full-wave voltage doubler
- Discuss voltage triplers
- Discuss voltage quadruplers

Voltage Doubler

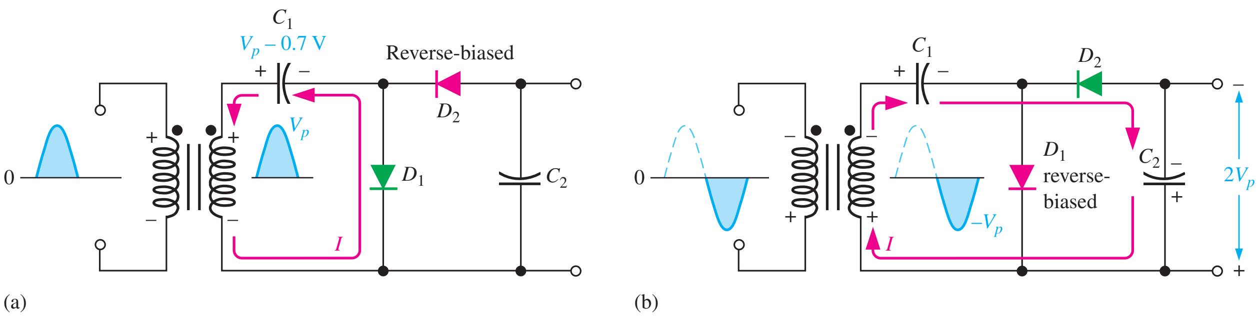
Half-Wave Voltage Doubler A voltage doubler is a **voltage multiplier** with a multiplication factor of two. A half-wave voltage doubler is shown in Figure 2–67. During the positive half-cycle of the secondary voltage, diode D_1 is forward-biased and D_2 is reverse-biased. Capacitor C_1 is charged to the peak of the secondary voltage (V_p) less the diode drop with the polarity shown in part (a). During the negative half-cycle, diode D_2 is forward-biased and D_1 is reverse-biased, as shown in part (b). Since C_1 can't discharge, the peak voltage on C_1 adds to the secondary voltage to charge C_2 to approximately $2V_p$. Applying Kirchhoff's law around the loop as shown in part (b), the voltage across C_2 is

$$V_{C1} - V_{C2} + V_p = 0$$

$$V_{C2} = V_p + V_{C1}$$

Neglecting the diode drop of D_2, $V_{C1} = V_p$. Therefore,

$$V_{C2} = V_p + V_p = 2V_p$$

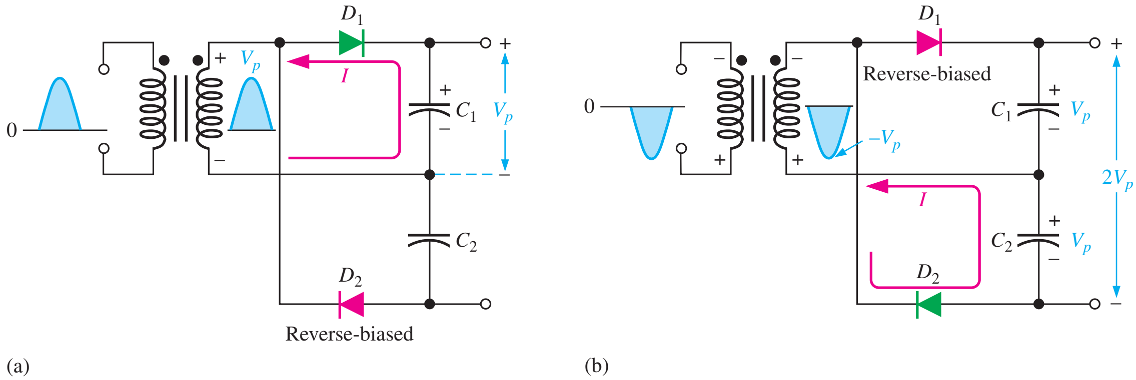


▲ FIGURE 2–67

Half-wave voltage doubler operation. V_p is the peak secondary voltage.

Under a no-load condition, C_2 remains charged to approximately $2V_p$. If a load resistance is connected across the output, C_2 discharges slightly through the load on the next positive half-cycle and is again recharged to $2V_p$ on the following negative half-cycle. The resulting output is a half-wave, capacitor-filtered voltage. The peak inverse voltage across each diode is $2V_p$. If the diode were reversed, the output voltage across C_2 would have the opposite polarity.

Full-Wave Voltage Doubler A full-wave doubler is shown in Figure 2–68. When the secondary voltage is positive, D_1 is forward-biased and C_1 charges to approximately V_p, as shown in part (a). During the negative half-cycle, D_2 is forward-biased and C_2 charges to approximately V_p, as shown in part (b). The output voltage, $2V_p$, is taken across the two capacitors in series.



▲ FIGURE 2–68

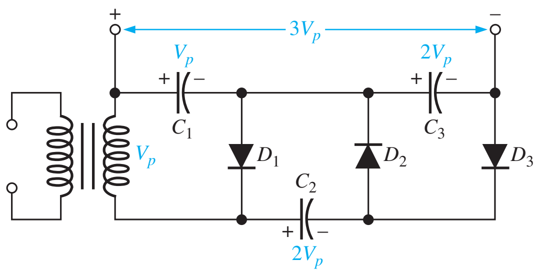
Full-wave voltage doubler operation.

Voltage Tripler

The addition of another diode-capacitor section to the half-wave voltage doubler creates a voltage tripler, as shown in Figure 2–69. The operation is as follows: On the positive half-cycle of the secondary voltage, C_1 charges to V_p through D_1. During the negative half-cycle, C_2 charges to $2V_p$ through D_2, as described for the doubler. During the next positive half-cycle, C_3 charges to $2V_p$ through D_3. The tripler output is taken across C_1 and C_3, as shown in the figure.

▶ FIGURE 2–69

Voltage tripler.

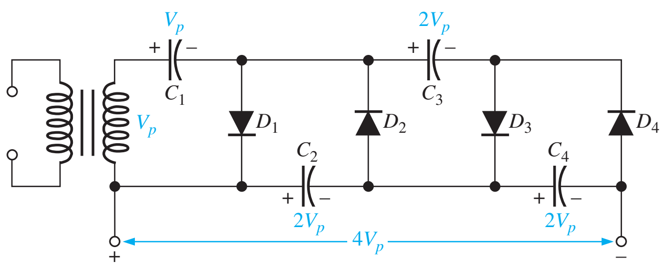


Voltage Quadrupler

The addition of still another diode-capacitor section, as shown in Figure 2–70, produces an output four times the peak secondary voltage. C_4 charges to $2V_p$ through D_4 on a negative half-cycle. The $4V_p$ output is taken across C_2 and C_4, as shown. In both the tripler and quadrupler circuits, the PIV of each diode is $2V_p$.

▶ FIGURE 2–70

Voltage quadrupler.



Reference

Electronic devices (Electron version) Floyd: Diodes Applications section Chapter 2