Fundamentals of ESD protection at system level

Introduction

Electrostatic discharge (ESD) are usually known as a sensation of electronic shock when walking across a carpet or opening a car door. The ESD definition given by https://www.esda.org is “the rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field”.

The most common way to charge electrically a material is to rub two materials and to separate them. The electron transfer between both materials, called triboelectric charge, generates an electrostatic field. The physics related to triboelectric generation is complex and driven by several parameters: surface roughness, temperature, strain, and other material properties. It is not very predictable and only broad generalizations can be made. The Table 1 reports typical voltages of static generation with various means of generation and relative humidity.

Table 1. Examples of static generation - typical voltage levels

Means of generation	10-25% relative humidity	65-90% relative humidity
Walking across carpet	35,000 V	1,500 V
Walking across vinyl tile	12,000 V	250 V
Worker at a bench	6,000 V	100 V
Poly Bag Picked up from Bench	20,000 V	1,200 V
Chair with Urethane Foam	18,000 V	1,500 V

ESD voltages are higher than typical electronics circuits voltages (few volts usually) and electronics circuits are not natively adapted to support them.

Specific strategies are employed to limit effect of ESD. They are based on ESD control plan development and on ESD control procedures and materials. These solutions are very efficient on a closed environment where electronics product are exposed to ESD events (electronics assembly plant, as example). These strategies do not eradicate ESD events but they put under control events and validate the level compatibilities with sensitive electronics devices. When facing to uncontrolled area (i.e. the real world), an electronics system without any ESD specific protection, will be faced to catastrophic field failure rate directly induced by the ESD.

1 Impact on electronic devices

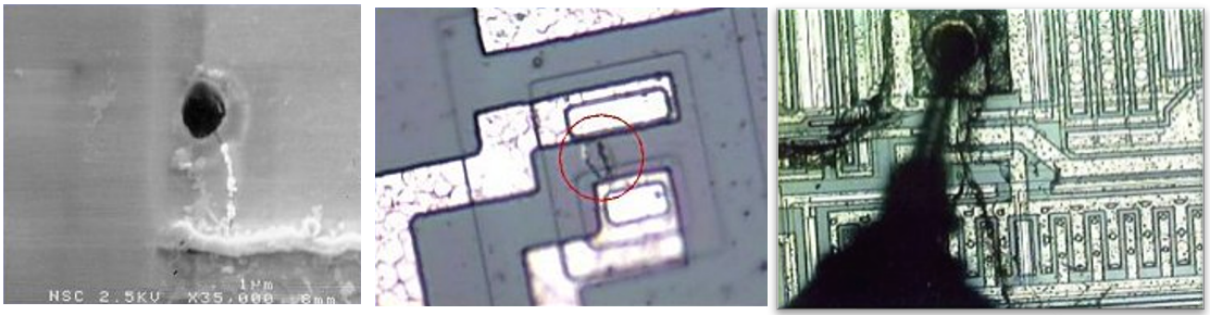
ESD is critical for electronic devices. As example, integrated circuits (ICs) can be affected at silicon level by ESD.

Three major failure mechanisms are illustrated on Figure 1 :

- Oxide punch-trough: the over-voltage induce by ESD exceed the dielectric breakdown strength. The oxide layer breakdown can generate a short circuit. Thinner the oxide is and more sensitive to ESD is.
- Junction damage or burn-out: the energy of ESD destroys the silicon p-n junction in short-circuit.
- Metallization / resistor fusing: the high current injection on metallization / resistor during the ESD event melts metal by joule heating. The results is an open circuit.

These impacts can be combined. As example, a junction damage can lead to metal tracks fuse due to its consecutive high current.

Figure 1. ESD induced damages (from left to right: oxide punch through, junction burnout and metallization fusing)



Listed ESD damages are catastrophic (short or open circuits). ESD events can also generate less severe defaults with as example a leakage current increases without functionality lost. But latent failures can also appear consecutively to ESD event.

The shrinkage, induced by technological evolutions, increases the IC sensitivity to ESD. Indeed, physical IC parameter sensitive to ESD are more and more constraint over technological nodes (oxide thicknesses reduction, metal track widths and thicknesses reduction, …). This is why ESD is becoming more and more critical for electronics hardware.

2 Protection against ESD

At circuit level, human body model (ANSI/ESDA/JEDEC JS-001) describes ESD waveform and test method approximating the discharge from the fingertip of a typical human being. It is intensively used to guaranty the robustness of circuits during manufacturing processes. All IOs (inputs/ouputs) of ICs must be protected.

The most common granted value is 2 kV but lower values can be observed for circuits manufactured with advanced technologies. Indeed, on-chip ESD protections are negatively impacted by scaling effect of technological node evolution. The dimension reduction trends to increase the sensitivity (oxide breakdown, metal trace fuse …) while the energy to dissipate is kept constant.

At system level, only IOs of ICs exposed to ESD from external world need to be protected (connectors, touch sensors, buttons and antenna tracks as example).

IEC 61000-4-2 standard describes test methods to perform ESD. It also defines ranges of test levels as reported on Table 2:

- In contact discharge, when the test generator is held in contact with the device under test (DUT)
- In air discharge, in which the charged electrode of the test generator is brought close to the DUT, and the discharge actuated by a spark to the DUT

The level correspond to a functional validation.

Table 2. IEC 61000-4-2 test levels

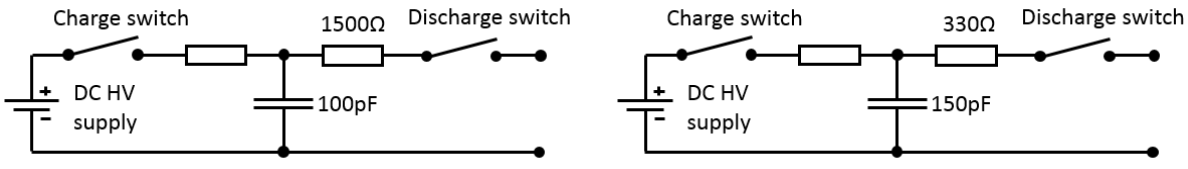
Contact discharge		Air discharge	
Level	Test voltage	Level	Test voltage
1	2 kV	1	2 kV
2	4 kV	2	4 kV
3	6 kV	3	8 kV
4	8 kV	4	15 kV

System regulations require various levels, as example, “EN 55024, Information technology equipment - Immunity characteristics - Limits and methods of measurement” imposes 4 kV contact discharge and 8 kV air discharge.

However, the most common level used on consumer applications is level 4 (8 kV contact – 15 kV air). Sometimes, more severe discharge level can be used to insure robustness based on use-case information (as example with hoovers that mechanically generate ESD).

HBM and IEC 61000-4-2 generator simplified schematics are presented on Figure 2.

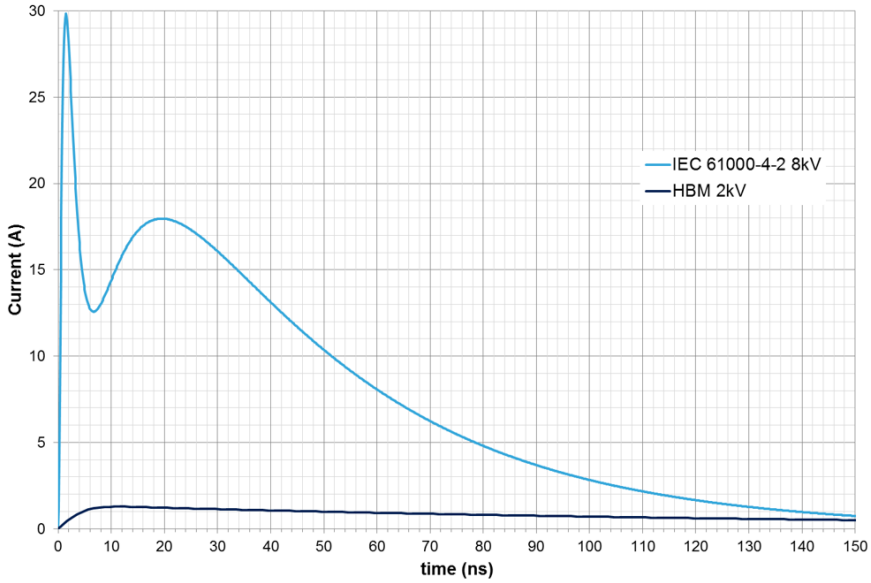
Figure 2. HBM (left) and IEC 61000-4-2 (right) generator simplified schematics



Basically, they correspond to a capacitor discharge thought a serial resistor that limits the current.

The Figure 3 shows the current as function of time of IEC61000-4-2 8 kV ESD and HBM 2 kV ESD, the most common ESD protection levels.

Figure 3. Current waveforms of IEC61000-4-2 8 kV and HBM 2 kV



The IEC 61000-4-2 8 kV waveform is based on an equation detailed on the standard. It is noticeable that a first current peak has very short rise time (less than 1ns) and a high current value. This first current peak require a faster ESD protection for IEC61000-4-2 8 kV than for HBM 2 kV waveform. The second peak of IEC61000-4-2 8kV is much more energetic with maximum current of 18 A than HBM 2 kV with a maximum current of 1.3 A.

These curves illustrate the severity of the 8 kV IEC 61000-4-2 system standard compared to 2 kV HBM component standard.

However, both standards require ESD protections:

- HBM is related to electronics components on ESD controlled environments for manufacturing. ICs are protected with integrated on-chip ESD protections on all IOs.
- IEC61000-4-2 is related to electronics system on end-user environment. Only exposed IOs of ICs need to be protected, thanks to external ESD protections added in parallel to integrated on-chip HBM protections.

3 External ESD protections

On one hand, an ESD protection must grant system integrity when ESD event is applied. It clamps the ESD voltage at a value lower than IO destruction value. It is its main feature.

On the other hand, the protection must be transparent when it does not work. Indeed, the ESD protection must have the less impact as possible on the system performances when system is working (consumption increase, bandwidth reduction as example).

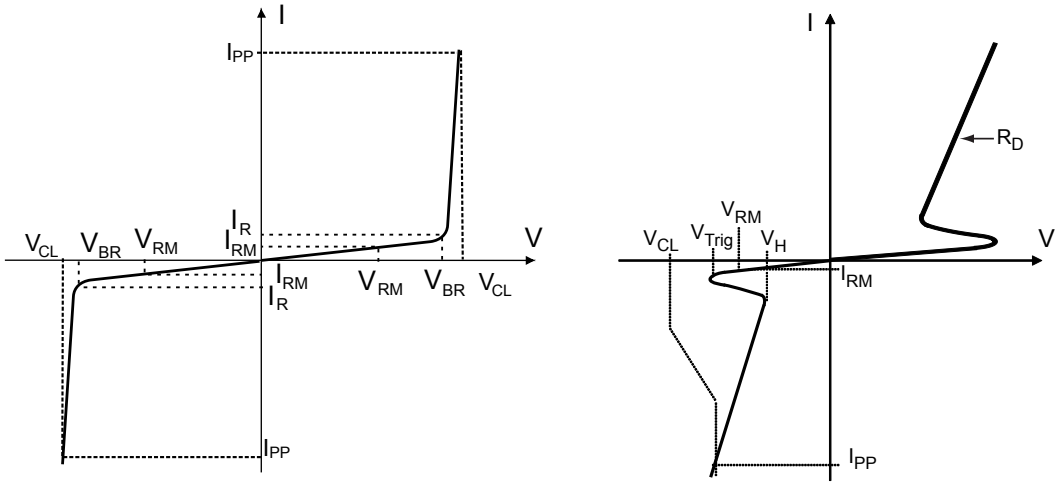
The selection of an external ESD protection must take into account both constraints.

External ESD protections can be grouped into two families:

- Standard series with a Zener like I/V curve (ESDV5-1BF4, as example)
- Snap-back series with a snap back effect on I/V curve (ESDZV5-1BF4, as example)

Electrical characteristics are presented on Figure 4.

Figure 4. ESD external protection electrical characteristics (left: standard, right: snap-back)



Main common parameters are:

- V_{RM}: maximal working voltage with associated maximum leakage current (I_{rm})
- C_{LINE}: line capacitance usually given at 0 V with 30 mV of oscillation voltage at 1 MHz. This value generally decreases with applied voltage. It also generally decreases with oscillation frequency.
- I_{PP}: peak pulse current correspond to maximal current for a given waveform. A clamping voltage (V_{cl}) is also associated to obtain P_{PP} (peak pulse power). Usually, V_{cl} presented on datasheet is measured with IEC 61000-4-2 8 kV ESD discharge. If several current waveforms are reported, there is no correspondence between V_{CL} values.
- R_D: dynamics resistance, it is obtained with the clamping voltage response when a 100 ns width square current waveform short pulse is applied.

Standard ESD protection is active at breakdown voltage (V_{BR}) usually define at 1 mA DC.

Snap-back ESD protection turns-on at trigger voltage (V_{Trig}). The protection voltage has a snap-back effect in order to lower the clamping voltage. The holding voltage (V_H) is the lowest voltage when the protection has turned-on and as consequence a lower voltage induce the turn-off of the protection.

The lower is the holding voltage, the better is clamping voltage with constant R_D.

4 Product selection

4.1 When protection is off: transparency

When protection is off, it must be as transparent as possible.

The first parameter to ensure a good transparency is to determine minimum and maximum voltage signal to be protected. The V_{rm} of the ESD protection must be higher than the signal voltage amplitude. If the signal is negative and positive, the protection must be bi-directional to avoid rectifier phenomenon. If the signal to be protected is only positive, an unidirectional protection is preferred especially for negative ESD clamping voltage. A bidirectional protection can also work.

A too high leakage current can, not only, affect the system overall consumption but also, it can change a data line voltage through a pull-up resistor. Usually, it is below 1 µA at V_{rm} (as example, ESDZV5-1BF4 and HSP053-4M5 I_{rm} is 100 nA maximum). This value is much lower than IC consumption, i.e., few order of magnitude lower than ICs lowest supply current in run mode. Pull-up resistors are usually between few 1 kΩ to few 10 kΩ. With 100 kΩ pull up resistor, a leakage current of 100 nA induces a line voltage shift of 10 mV. It is acceptable compared to nominal voltage of standard ICs (3.3 V or 5 V, as example).

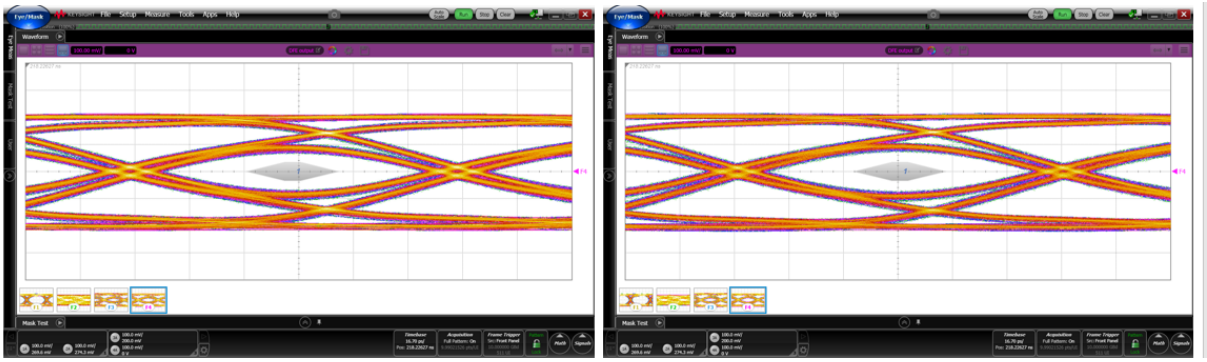
The protection line capacitance and the bandwidth are key factors for high speed lines (digital or RF lines).

HSP053-4M5 product has a very low capacitance (0.35 pF at 2.5 GHz).

It presents a -3 dB cut-off frequency of 18 GHz. Analog signal frequency must be lower than this value, for example, the attenuation at 2.4 GHz is lower than 0.5 dB.

For digital signals, eyes diagram of thru lines with and without protections are reported according the mask given on the standard. Figure 5 shows measurements of eye diagram for USB 3.1 Gen2 at 10.0 Gbps per channel.

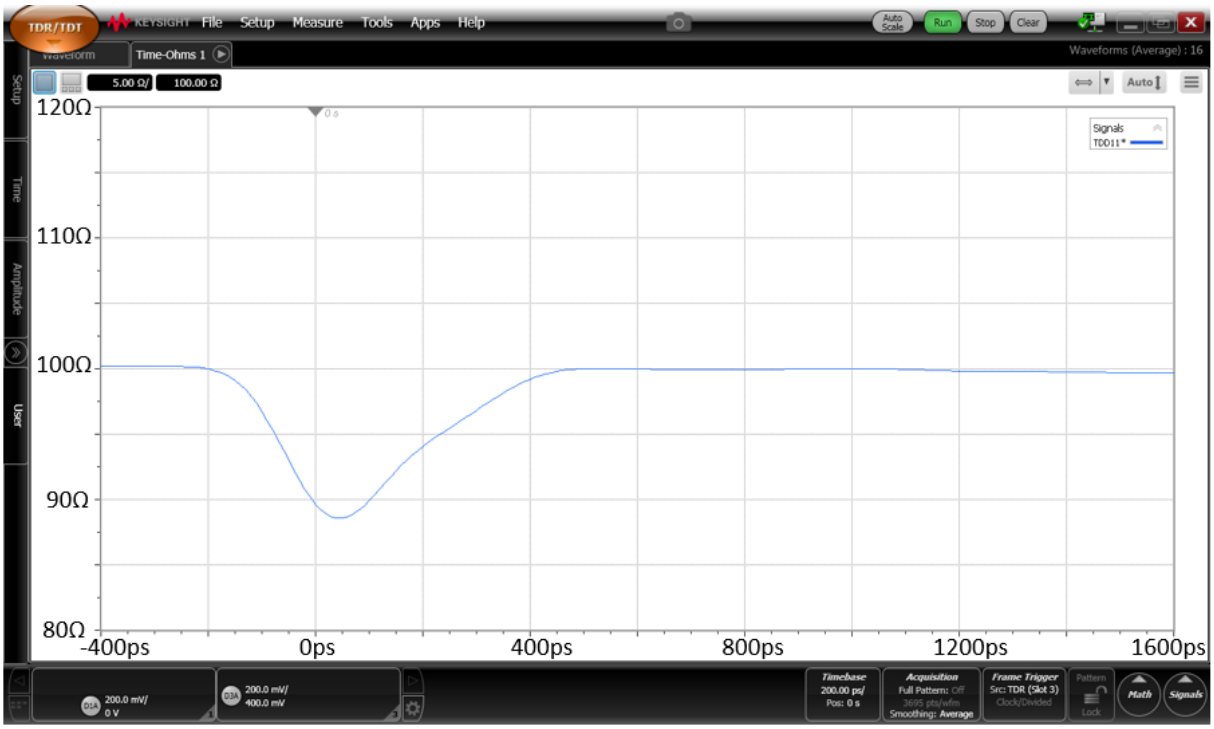
Figure 5. Eye diagram - USB 3.1 Gen2 mask at 10.0 Gbps per channel (Type-C connector, reference cable, EQ with DC = 6 dB and DFE).Eye diagram without HSP053-4M5 on left and with HSP053-4M5 on right.



The comparison of both images illustrates the negligible impact of HSP053-4M5 on data transmission for USB 3.1 at 10.0 Gbps per channel. This figure of merit shows the protection ability to be transparent from a transmission point of view. The standard conditions (voltages, rise and fall times …) are then validated with the protection.

Another numerical parameter is the impedance on a matched line measured with time domain reflectometry (TDR). Figure 6 presents the mismatch induced by the HSP053-4M5 placed in a 100 Ω line.

Figure 6. TDR measurement induced by induced by the HSP053-4M5 placed in a 100 Ω line with 200 ps rise time

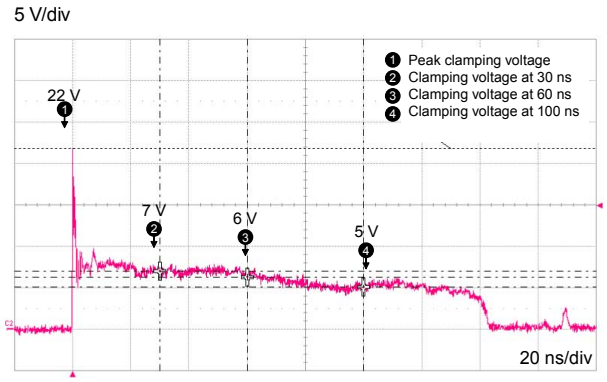


This figure of merit shows the ability of the protection system to stay transparent from a reflection point of view. The main driver is protection capacitance but line impedance modification done for protection footprint implementation is also validated.

4.2 When protection is on: efficiency

In order to be close to the worse application conditions, IEC61000-4-2 level 4 (+/-8kV) contact discharge are applied to the component. The temporal response of ESDZV5-1BF4 is presented on Figure 7.

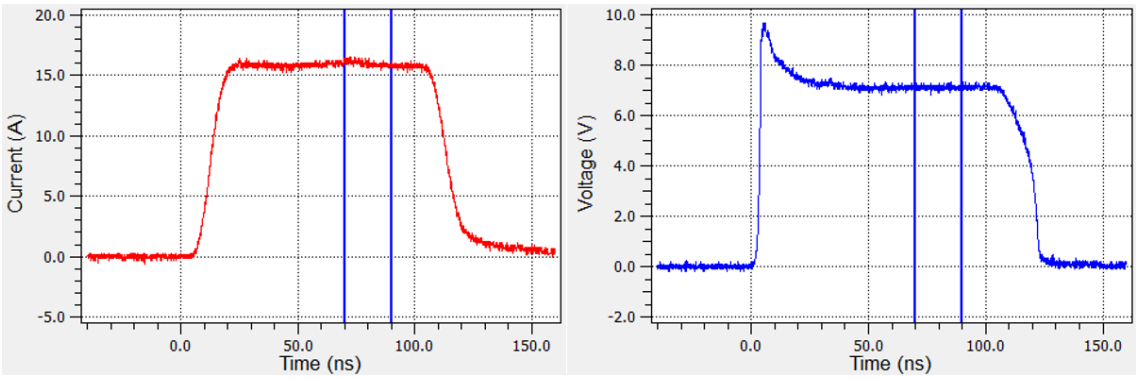
Figure 7. ESDZV5-1BF4 ESD response to IEC 61000-4-2 (+8 kV contact discharge)



A noticeable value is the 30 ns voltage. This is the usual definition of clamping voltage of an ESD protection. This key parameter reveals the protection efficiency against an ESD event, indeed, it corresponds to the ability of the ESD protection to limit the voltage when an ESD event is present and then to protect the IC placed behind the ESD protection.

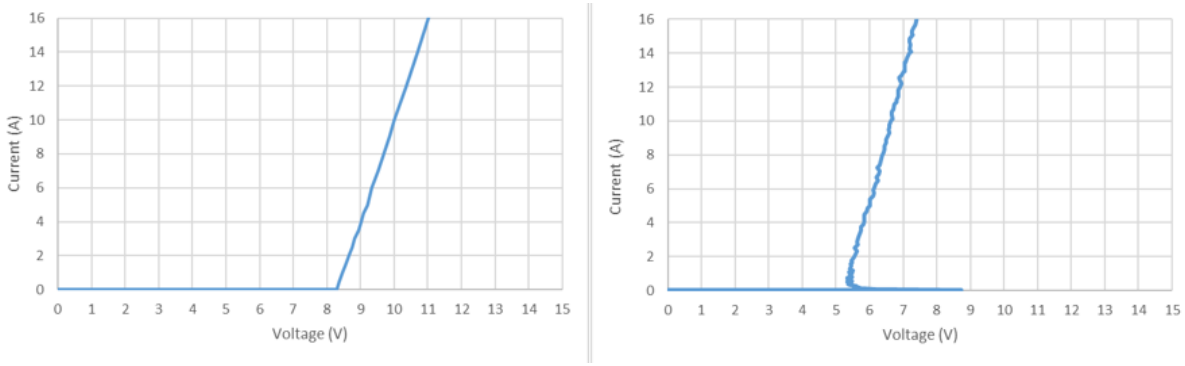
The clamping voltage can also be studied using the transmission line pulse (TLP) method. It is a high voltage 50 Ω cable discharge on the ESD protection. The incident current waveform parameters are described on ANSI/ESD STM5.5.1 : 100 ns square waveform with 10 ns or less rise time (see Figure 8 left as example) . The resulting voltage is an average on the 70 ns - 90 ns windows in order to measure a stabilized voltage before fall (see Figure 8 right).

Figure 8. ESDZV5-1BF4 TLP (16 A – 100 ns width – 10 ns rise time) time responses (current on left and voltage on right)



TLP time responses with various incident currents enable the construction of clamping voltage as function of the incident current (see Figure 9).

Figure 9. TLP response of ESD051-1BF4 (left) and ESDZV5-1BF4 (right)



- $V_{cl} = V_{br} + I_{pp} \times R_d$ for standard ESD protection (ESD051-1BF4 as example)
- $V_{cl} = V_h + I_{pp} \times R_d$ for snap-back ESD protection (ESDZV5-1BF4 as example)

The clamping voltage obtained at 30ns with IEC61000-4-2 8 kV discharge corresponds 16 A TLP response. Indeed, the current flowing at 30 ns with IEC61000-4-2 8 kV discharge is 16 A (see Figure 3).

ESD over-voltages are always higher than trigger voltage of snap-back protection, as consequence, snap-back ESD protections always turn-on when an ESD occurs.

5 Product integration on system

Once the external ESD protection selected in respect to transparency and efficiency, the system integration can be checked.

5.1 ESD system safe operating area

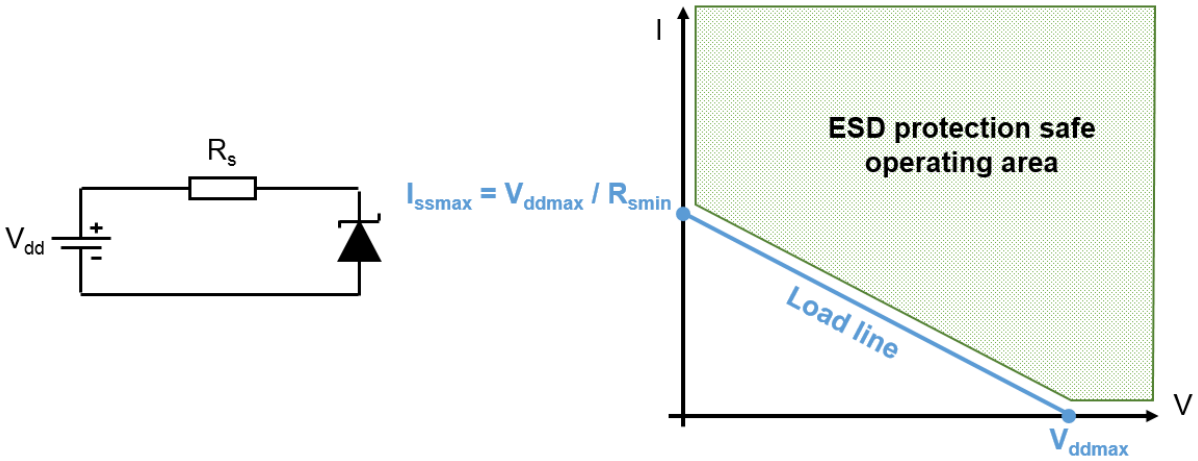
The ESD system SOA (Safe Operating Area) is critical for snap-back ESD protections. The ESD system SOA method ensures a return to normal operation after an ESD event (i.e. avoid latch-up).

Latch-up of the external protection is possible when a continuous voltage V_{dd} is present on the protected line (power supply or level '1' as example). Left schematic of Figure 10 shows the voltage, V_{dd}, the serial resistor R_s, and the external ESD protection D.

Several R_s values can be consider, as example:

- Power supply with a very low R_s value (usually less than 0.1 Ω)
- Push-pull output at level '1' with low R_s value (usually few Ω)
- Pull-up resistor with high R_s value (usually few 10 kΩ)

Figure 10. Schematic representation of protected schematic (left) and graphical representation of the circuit load line and ESD system SOA (right)



ESD system SOA area is above source load line (see Figure 10 right), on this area the ESD protection is latch-up free.

Reporting source load line and ESD protection I/V curve on same graphic (see Figure 11), two cases are possible:

- Figure 11, (a), (b), (c) and (d) curves cross the source load line only at V_{dd}. There is only a single solution that leads to normal state with negligible current on ESD protection.
- Figure 11, (e) curve cross the source load line at V_{dd} and also at V_I. Then, two solutions are possible. When the protection has not triggered, system voltage is V_{dd} and leakage current of ESD protection is negligible. It is the normal state. When, the ESD protection has been triggered by an ESD event, system is latched at V_I with a current I_I. This state is not suitable because a line reset is then required to return to normal state.

Figure 11. Protected circuit load line with various ESD protection I/V curves

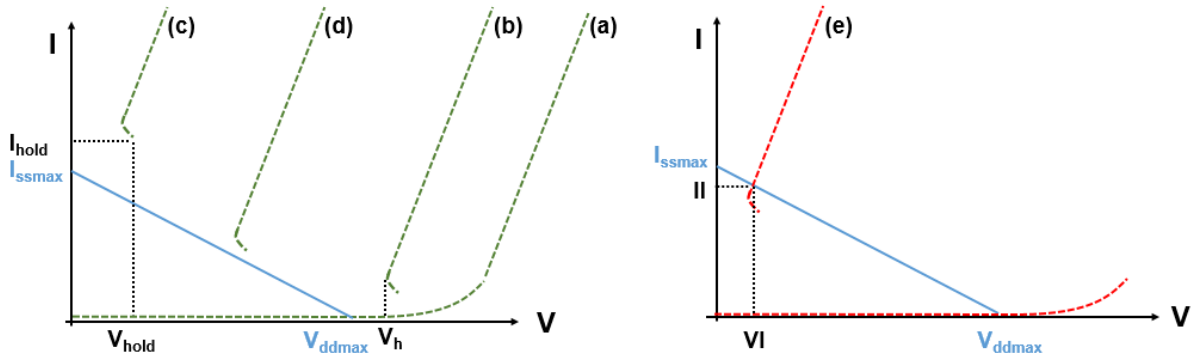


Figure 11 illustrates several cases :

- Curve (a): a non-snap-back ESD protection is latch-up free
- Curve (b): a snap-back ESD protection with a $V_h > V_{dd\ max}$ prevents the latch-up phenomena
- Curve (c): a snap-back ESD protection with a $I_{hold} > I_{ss\ max}$ prevents the latch-up phenomena
- Curve (d): a snap-back ESD protection with a couple (V_{hold}, I_{hold}) located in the safe operating area prevents the latch-up phenomena
- Curve (e): outside the SOA, the ESD protection stay latched after an ESD event

Slope of source load line is a key. As example, deep snap back ESD protections as SCR (i.e. ESD protection with holding voltage lower than V_{dd}) cannot be used with power supply. Nevertheless, these protections are mandatory for high speed data line that require low clamping voltage. On that case, minimum pull-up resistor and maximum V_{dd} must be taken into account to select protection on ESD system SOA (as example, HDMI lines: V_{dd_max} = 3.47 V and R_{s_min} = 45 Ω).

5.2 System efficient ESD design

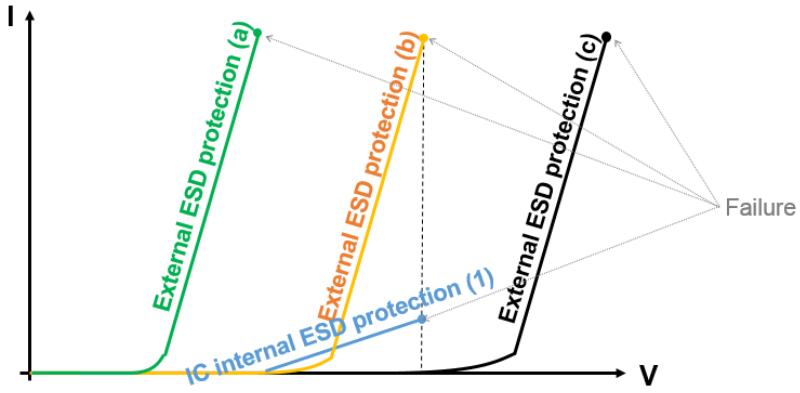
System efficient ESD design (SEED) is a method that grants a good co-working of external ESD protection and ESD protection inside the IC to be protected.

TLP response of external ESD protection has been presented previously. Same kind of curve can be obtain with IC internal ESD protection. Internal ESD protection is mainly dedicated to HBM and as consequence is much less robust than external ESD protection.

While reporting TLP responses of internal ESD protection and external ESD protection on same graphic (see Figure 12), 3 noticeable cases can be reported:

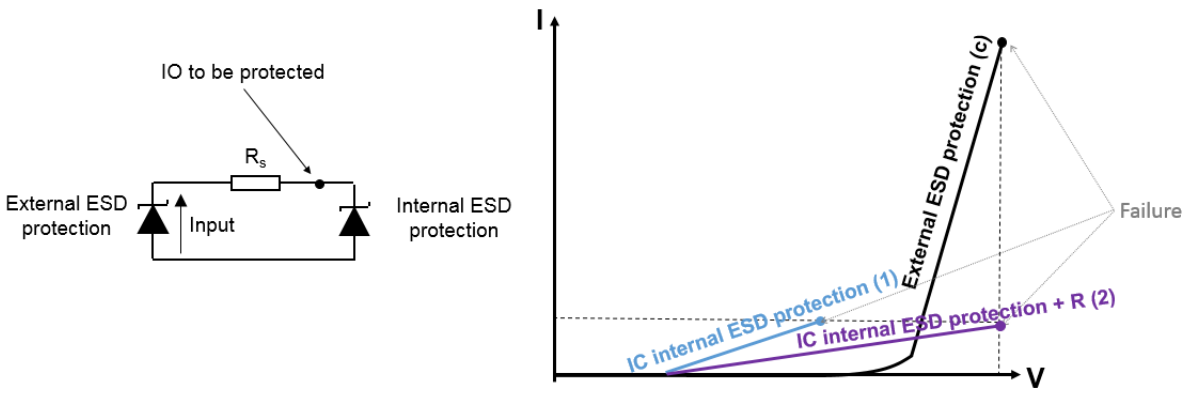
- External ESD protection triggered and failed before internal ESD protection has triggered (curve a). The system is well protected and the system ESD robustness correspond to the external ESD protection robustness.
- Internal and external ESD protections have triggered before failure of one protection. The current is shared between 2 protections. A specific case is noticeable when the failure of internal ESD protection and external ESD protection (curve b) are reached at same voltage. Then, the maximum current allowed before destruction is the sum of maximum current of internal and external ESD protection. In other words, the system robustness is the sum the robustness of both protection. It is an optimal co-working for internal and external ESD protection.
- Internal ESD protection triggered and failed before external ESD protection has triggered (curve c). The external ESD protection is not efficient alone to grant the system robustness.

Figure 12. Internal and external ESD protection TLP curves



To solve the last case weakness on ESD system robustness, a serial resistor is placed between the IO to be protected and the external ESD protection (see Figure 13) to obtain an Z-R-Z structure.

Figure 13. Z-R-Z structure (left) and associated TLP curves (right)



TLP curves are then (Figure 13 right):

- IC internal ESD protection (curve 1)
- External ESD protection (curve c), that does not grant ESD system robustness alone as explained on previous example
- External ESD protection with the serial resistor R_s (curve d), the resistor lower the slope compared to the curve without resistor

The voltage drop between Figure 13 (1) and (2) is only due to the serial resistor R_s.

The equivalent system seen by the TLP on system input is two protections in parallel:

- The external ESD protection
- The internal ESD protection with the serial resistor R_s

Thanks to a good selection of R_s, it is possible to obtain the optimal co-working as presented above when both protections fails at same time.

The resistor value must be acceptable from a transparency point of view (as example, do not modify too much line impedance and as consequence the eye diagram).

SEED method allows a prediction and an optimization of the ESD system robustness. Unfortunately, while ESD external protection datasheets present TLP curves, IOs of IC exposed to external ESD events (GPIOs of microcontroller, specific IOs of ASIC, connector ports, antenna ports ...) usually do not present TLP curves. Then, the SEED method can be experimentally adapted with a serial resistor increase to maximize iteratively the system ESD robustness. Usually, few Ohms are enough with an external ESD protection V_{rm} selected close to the maximal system voltage.

6 Conclusion

Technological evolutions inexorably increase electronics devices ESD sensitivity. Silicon manufacturers grant IC compatibility with assembly plant but IOs exposed to the real world need external ESD protections.

An external ESD protection selection must complies with two mains items:

- The transparency: the external ESD protection must not impact system performances or, at least, impacts them the less as possible.
- The efficiency: the external ESD protection must protect against system level ESD event.
- Both items have been discussed and impacts on external ESD protection parameters have been detailed. Then, the external ESD protection integration on the system is also presented because it also affects product selection.

ESD related choices must be done at early design phase to avoid any complicated fixes on the validation phase or dramatics solutions when done on the field.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
07-Nov-2018	1	Initial release.

Contents

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