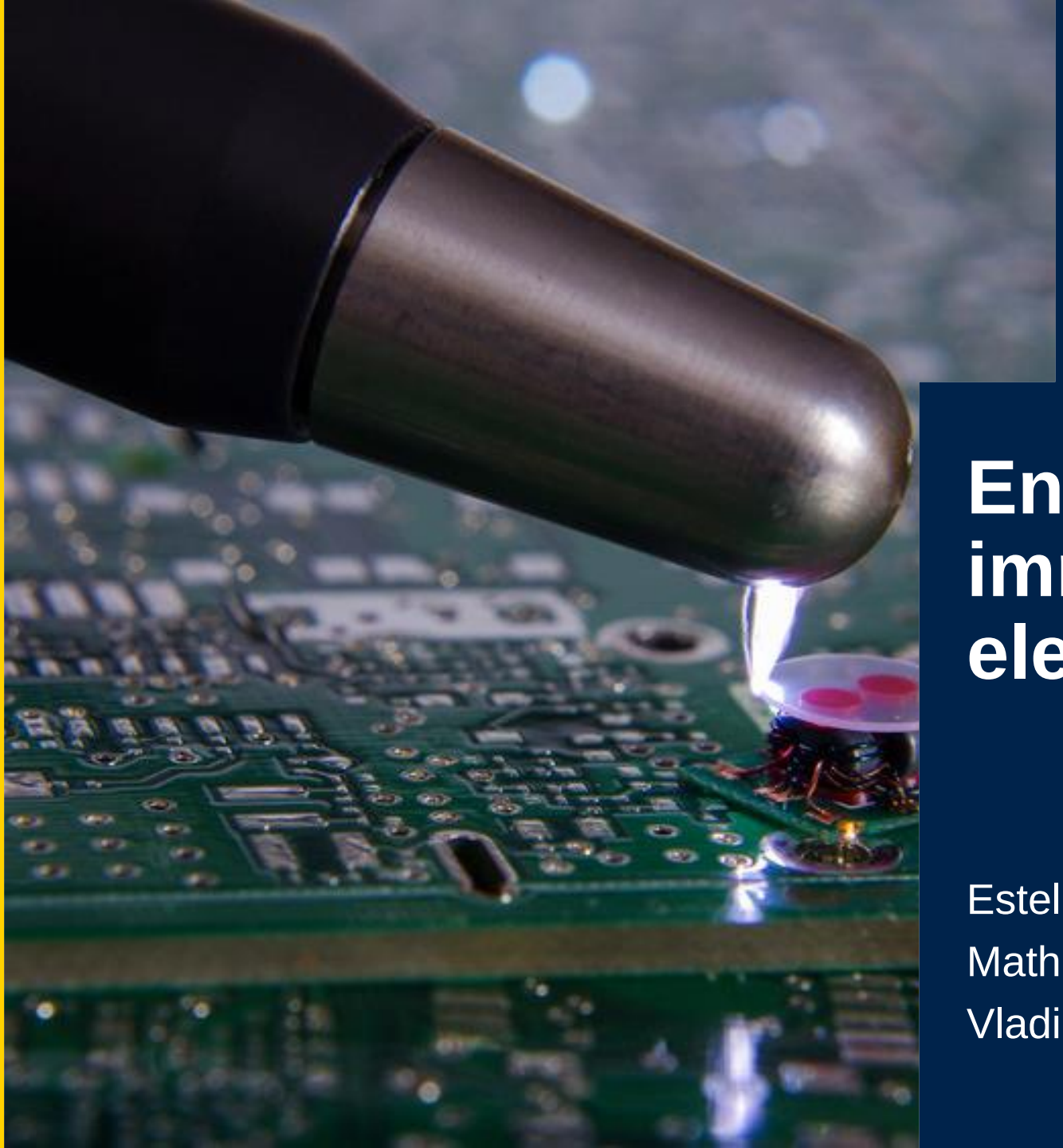

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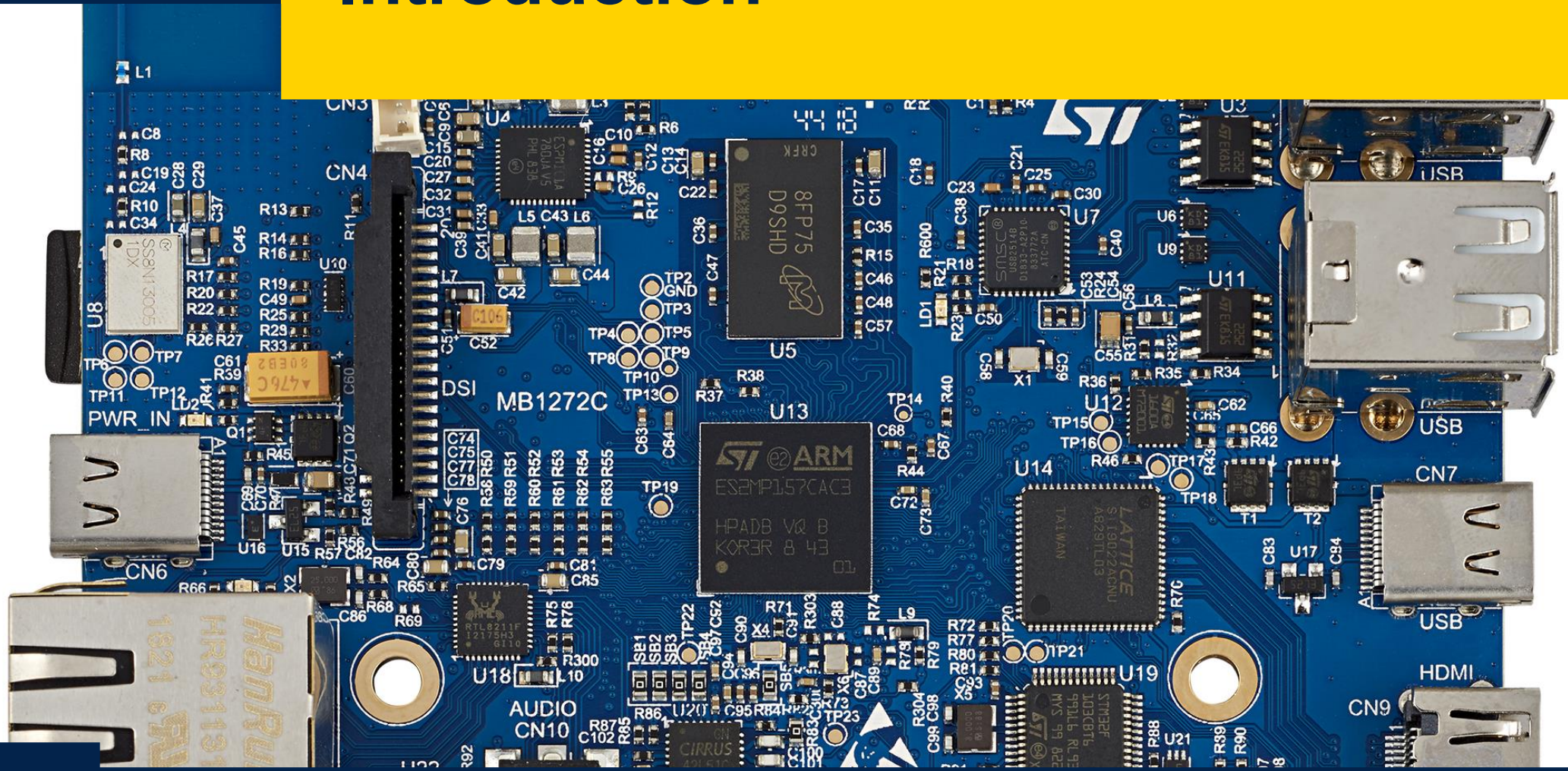
Ensuring system immunity against electrostatic discharges

Estelle ASTAR, Product Marketing Engineer
Mathieu ROUVIERE, Application Engineer
Vladimir JANOUSEK, Application Team Manager

Introduction



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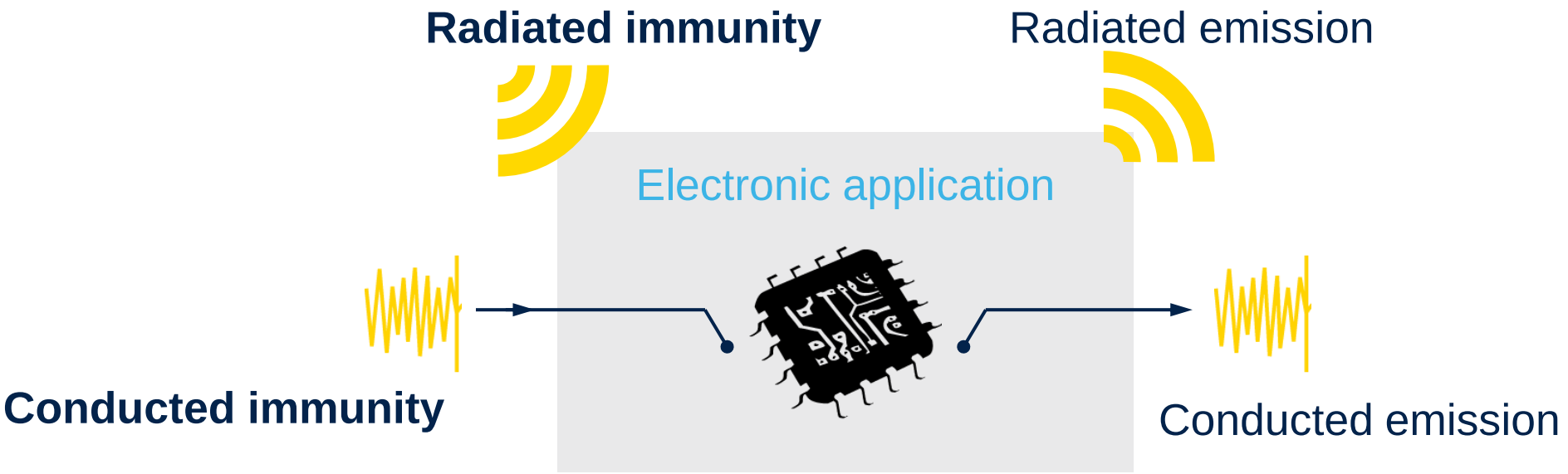
Defining EMC immunity

What is EMC immunity ?

EMC Immunity is the ability of an equipment to properly operate in its electromagnetic environment by limiting the interference of electromagnetic energy that may cause physical damage.



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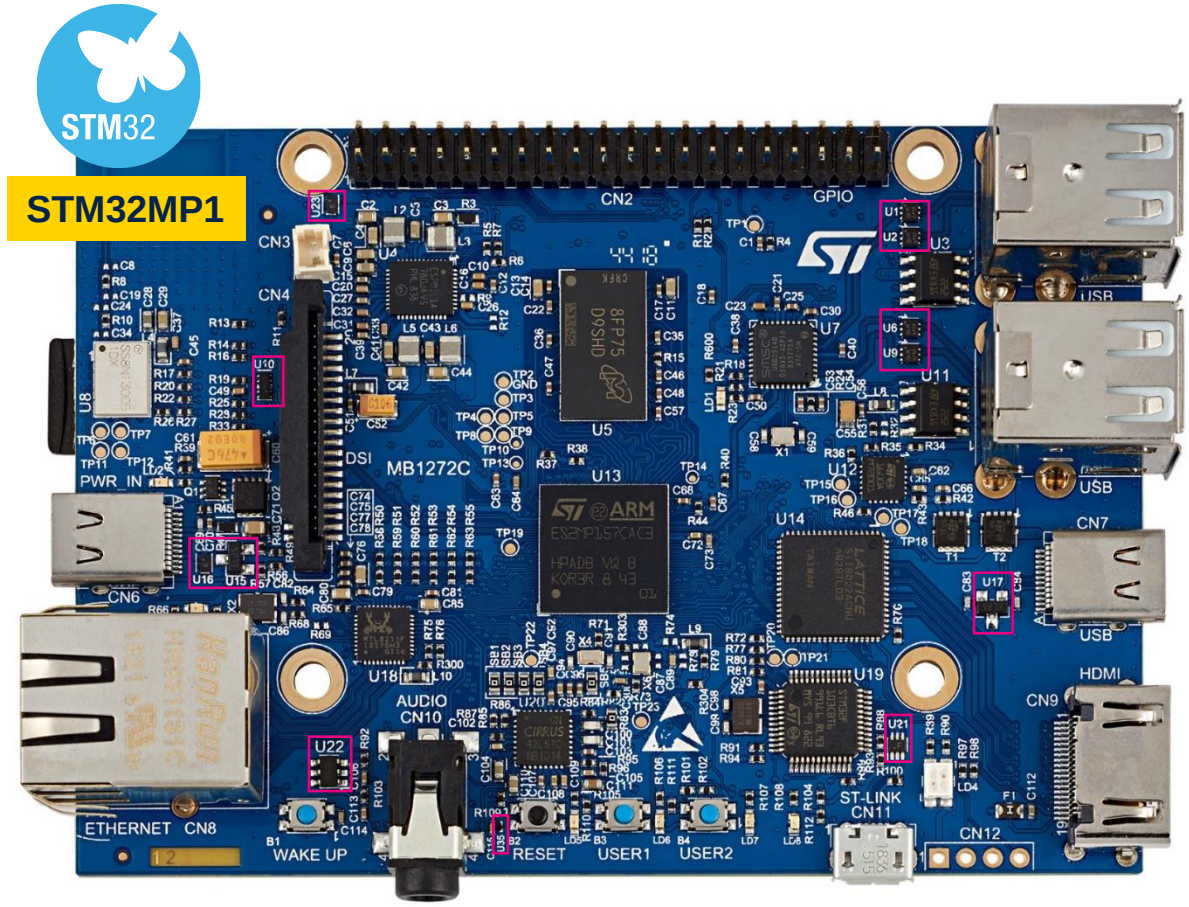
EMC immunity example discovery kit: STM32MP157A-DK1



MORPHO CONNECTOR
ESDA7P120-1U1M
5V Vin

MICRO SD CARD
HSP051-4M10 (x2)
SDMMC dataline

USB Type-C Power Delivery
ESDA7P120-1U1M, ESDA25L
VBUS
CC1, CC2

ETHERNET
HSP053-4M5

USB HOST x2 (Dual USB Type-A)
ESDA7P120-1U1M (x2), ECMF02-2AMX6 (x2)
VBUS
DP, DM

USB HOST x2 (Dual USB Type-A)
ESDA7P120-1U1M (x2), ECMF02-2AMX6 (x2)
VBUS
DP, DM

USB Type-C DRP (Source Only)
ESDA7P120-1U1M, ESDA25L, ECMF02-2AMX6
VBUS
CC1, CC2
DP, DM

HDMI
ECMF04-4HSWM10 (x2), ESDALC6V1-5M6
TMDS datalines
CEC, I2C, HPD

AUDIO
ESDA6V1BC6: 4-line ESD protection
OUTA, OUTB, MIC IN

USER BUTTONS
ESDALC6V1-1U2

ST-LINK USB CONNECTOR
USBLC6-2P6
DP, DM, VBUS

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STM32 MPU by

Agenda

1 ESD Protection at System Level

2 How to select an ESD protection device?

3 ESD Layout Guidelines

4 Application Examples

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ESD protection at system level

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How is ESD generated ?

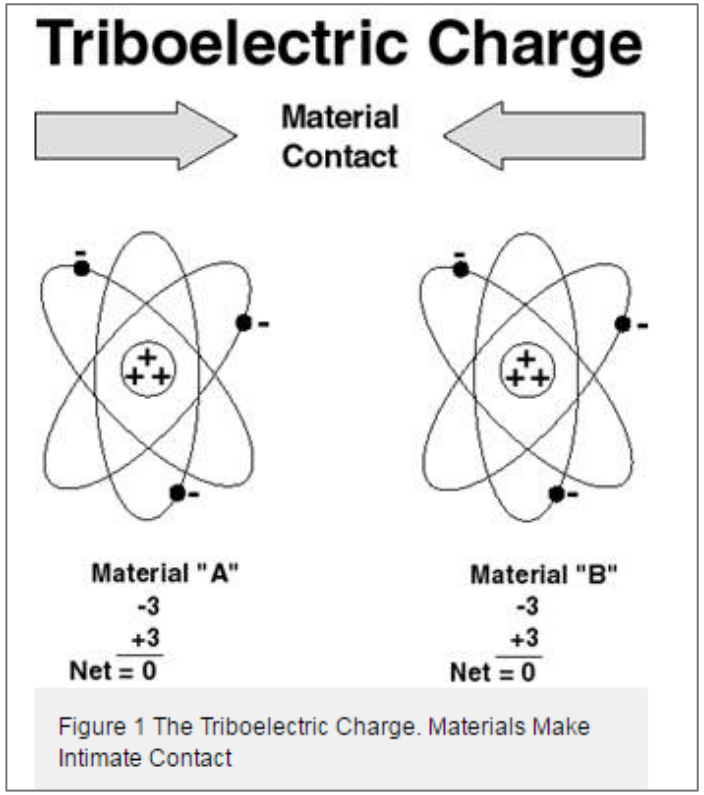


Figure 1 The Triboelectric Charge. Materials Make Intimate Contact

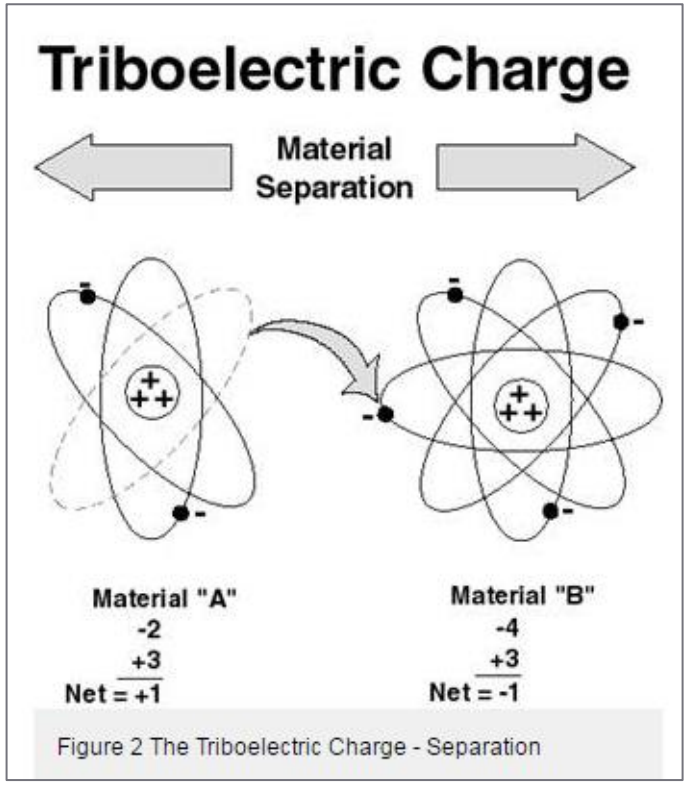


Figure 2 The Triboelectric Charge - Separation

Table 1 Examples of Static Generation - Typical Voltage Levels		
Means of Generation	**10-25% RH**	**65-90% RH**
Walking Across Carpet	35,000V	1,500V
Walking Across Vinyl Tile	12,000V	250V
Worker at a Bench	6,000V	100V
Poly Bag Picked up from Bench	20,000V	1,200V
Chair with Urethane Foam	18,000V	1,500V

Source: https://www.esda.org/about-esd/esd-fundamentals/part-1-an-introduction-to-esd/

ESD damages to ICs

White Paper on Electrical Overstress - EOS Industry Council on ESD Target Levels

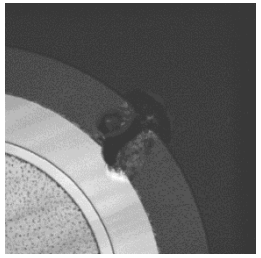
In preparation for this white paper, the Industry Council conducted a worldwide survey of the electronics industry concerning EOS. Results confirmed the long held view that EOS is consistently one of the “high bars” on product failure Pareto charts. Looking at the EOS survey, respondents reported greater than 20% of total failures being EOS-related or **30% of total electrical failures being EOS-related**, making EOS the largest bar on the Pareto chart of that responder’s known causes of returns.

Source:https://pdfs.semanticscholar.org/235b/0bfd01dd5f0c6c2c99df3b93bc27f56a9cfd.pdf

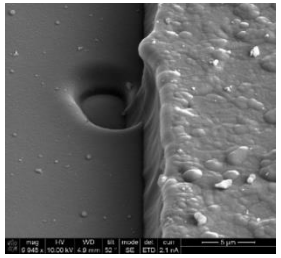
“30% of total electrical failure is EOS -related”

Source: STMicroelectronics

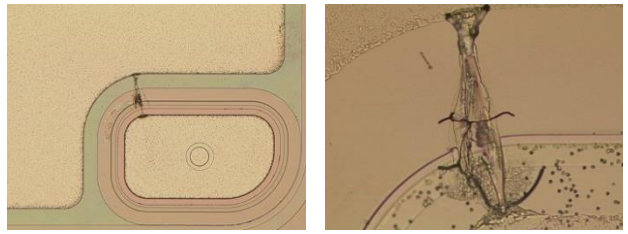
Silicon melting



Hole in the oxide



Melting Flash



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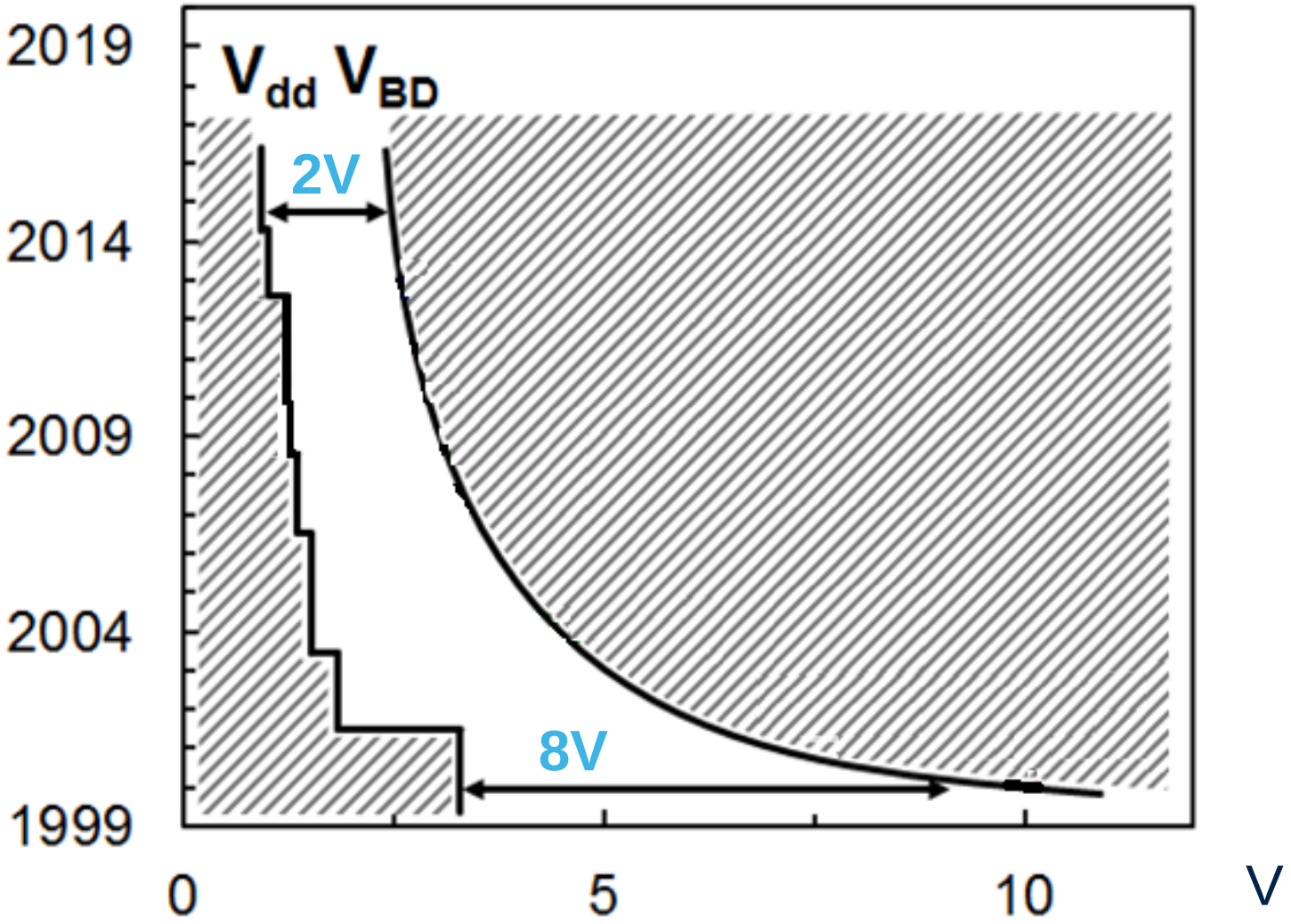
ESD sensitivity is increasing



V_{dd} = power supply voltage
V_{BD} = breakdown voltage

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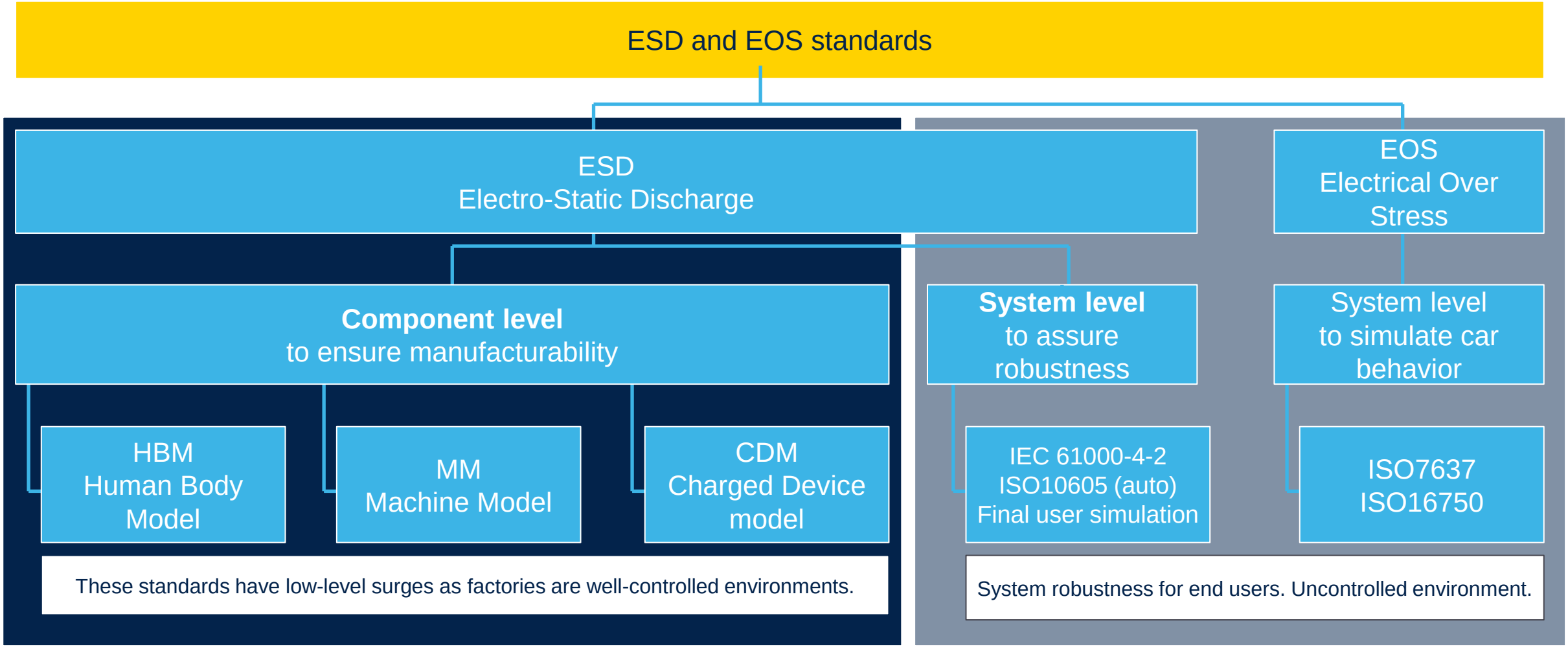
ESD and EOS standards



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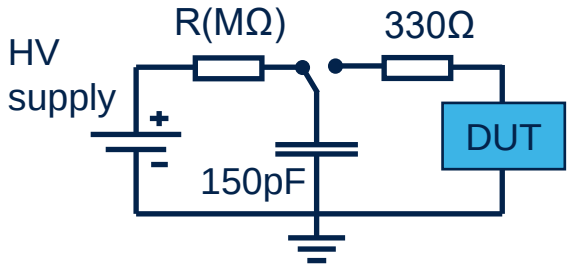
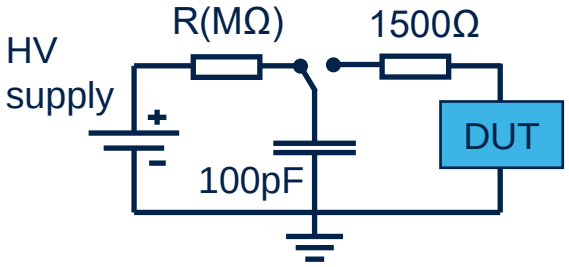
HBM and IEC standards

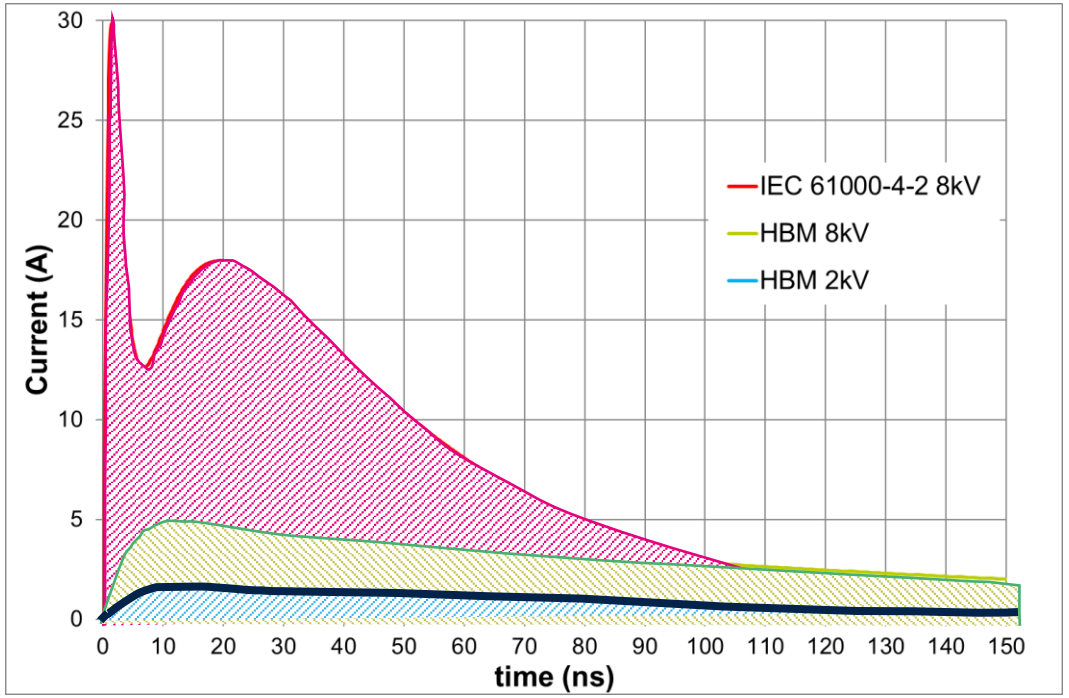
Difference in standards : IEC 61000-4-2 carries more energy than HBM

IEC 61000-4-2 for system
(+/-8kV for level 4)



Human Body Model for IC
(+/-2kV for most of IC)





Energy for 8kV IEC 61000-4-2

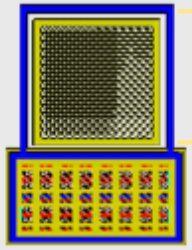
Energy for 8kV HBM

Energy for 2kV HBM

Component VS system level silicon die area comparison

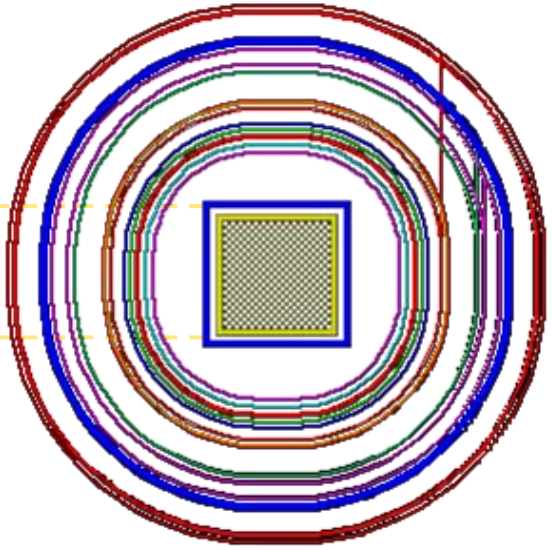
Silicon die area for component level ESD

(2 kV HBM)



Silicon die area for system level ESD

(8 kV IEC contact)



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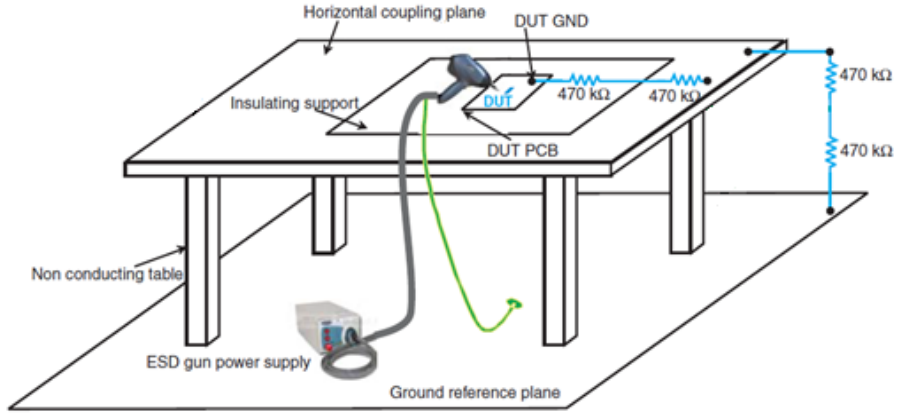
System-level ESD protection standard
IEC 61000-4-2 test bench

	Contact discharge	Air discharge	
Stress Level	Test Voltage (kV)	Test Voltage (kV)	Number of discharges
1	2	4	At least 10 single discharges at 1 Hz in the most sensitive polarity
2	4	6	
3	6	8	
4	8	15	



System state as a result of system–level ESD stress	
A	Normal performance
B	Temporary loss of function or degradation of performance which cease after the disturbance ceases. The DUT recover its normal performance , without operator intervention
C	Temporary loss of function or degradation of performance , the correction of which requires operator intervention
D	loss of function or degradation of performance, no recovery possible

Self-restored

Require a system reset

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ESD in automotive: ISO10605

Configuration	Mode	Component acessible from:	Test (A= Air C= contact)	Capacitance	Resistance	Max test voltage	Operating conditions	Min number of discharges	Min. time interval	Max suggested severity levels (ISO10605 Annex C)
Component	Direct	Inside	A & C	330 pF	330 ohm	-	Powered	3	1s	15 kV C 25kV A
Component	Direct	Outside	A & C	150 pF	330 ohm	-	Powered	3	1s	15 kV C 25kV A
Component	Indirect	Inside	C	330 pF	330 ohm	-	Powered	50	50ms	20kV C
Component	Indirect	Outside	C	150 pF	330 ohm	-	Powered	50	1s	20kV C
Component packaging and handling	Direct	NA	A & C	150 pF	330 or 2000 ohm	-	Unpowered	3	1s	
Vehicle test	Direct	Inside	A & C	330 pF	330 or 2000 ohm	15 kV	Engine drive or idle	3	1s	8kV C 15kV A
Vehicle test	Direct	Outside	A & C	150 pF	330 or 2000 ohm	25 kV	Engine drive or idle	3	1s	8kV C 25kV A

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How to select an ESD protection device

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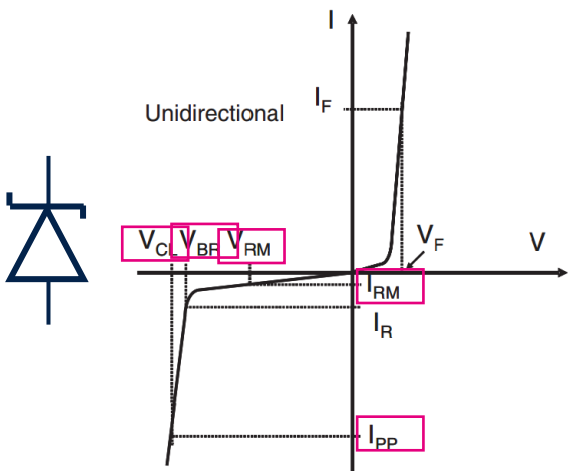
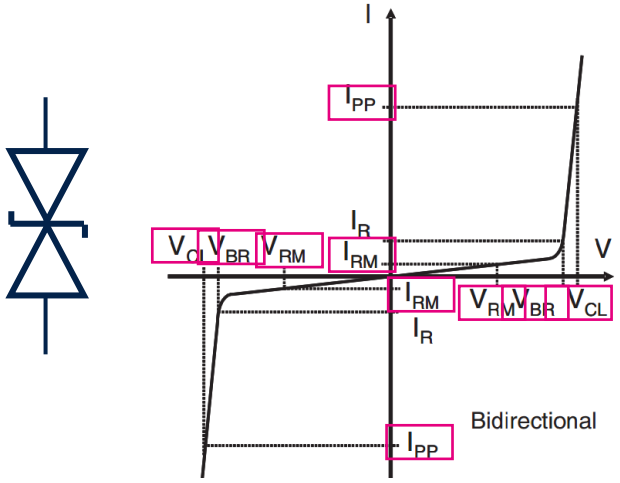
Key parameters

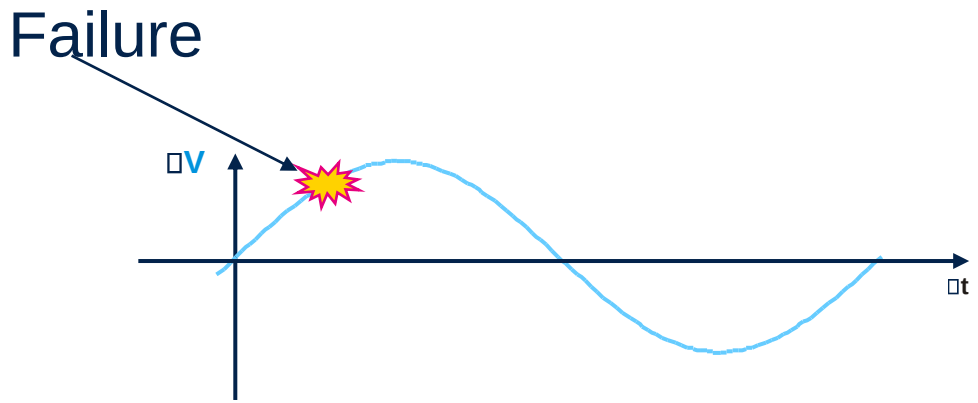
Parameters	Description
V_{RM}	Stand-off voltage (normal condition voltage)
I_{RM}	Leakage current
V_{BR}	Breakdown voltage (voltage when the ESD protection starts working)
V_{CL}	Clamping voltage (maximum voltage accross the ESD protection)
I_{PP}	Peak Pulse Current (maximum current in the ESD protection)
C	Line capacitance (impacts signal integrity)



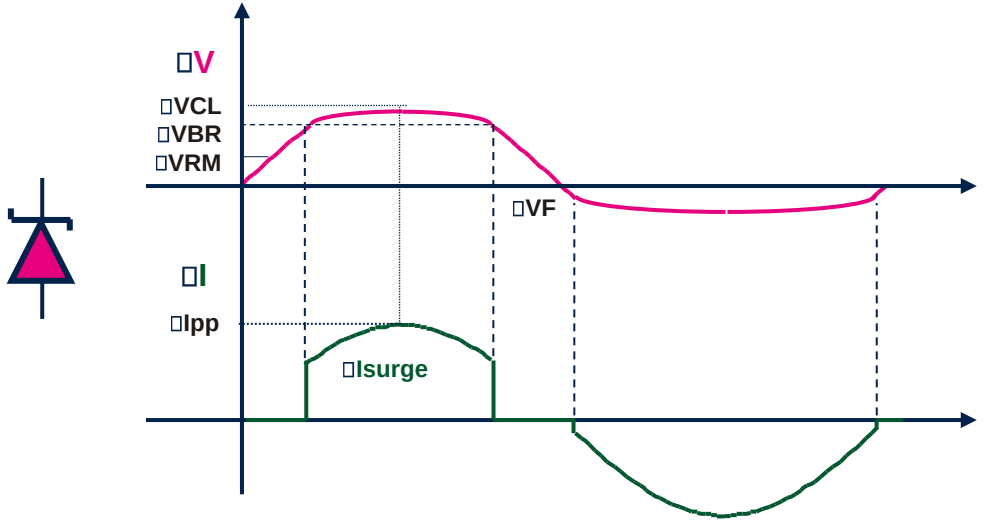


Protection selection key parameter : voltage

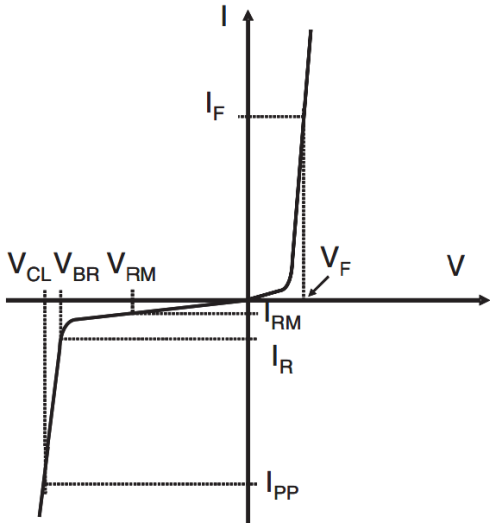
No TVS protection



With TVS protection



Uni-directional



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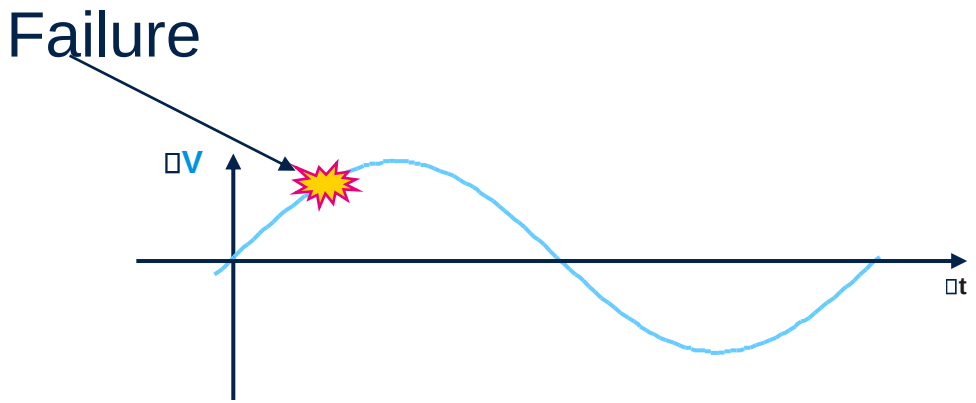
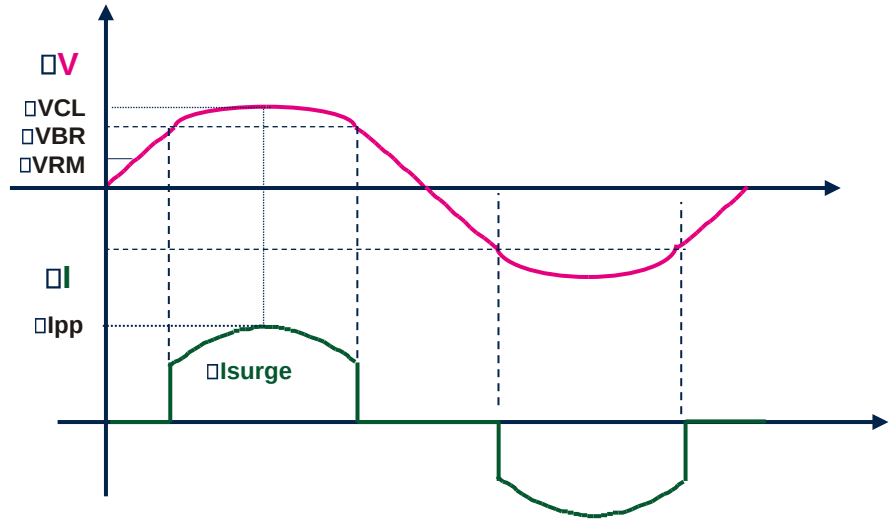
Key parameters voltage polarity

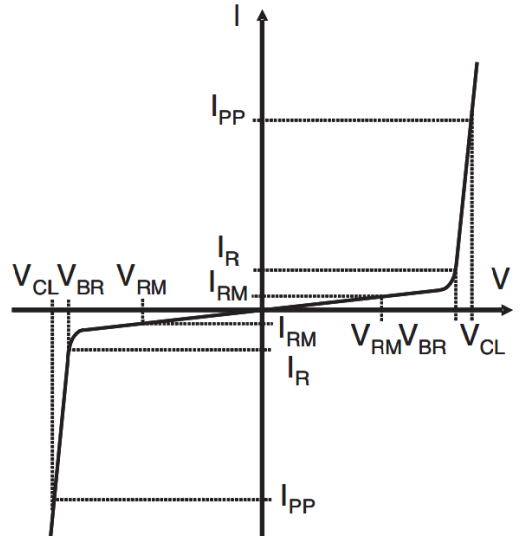
No TVS protection



With TVS protection



Bi-directional



- Mandatory for audio and RF signals

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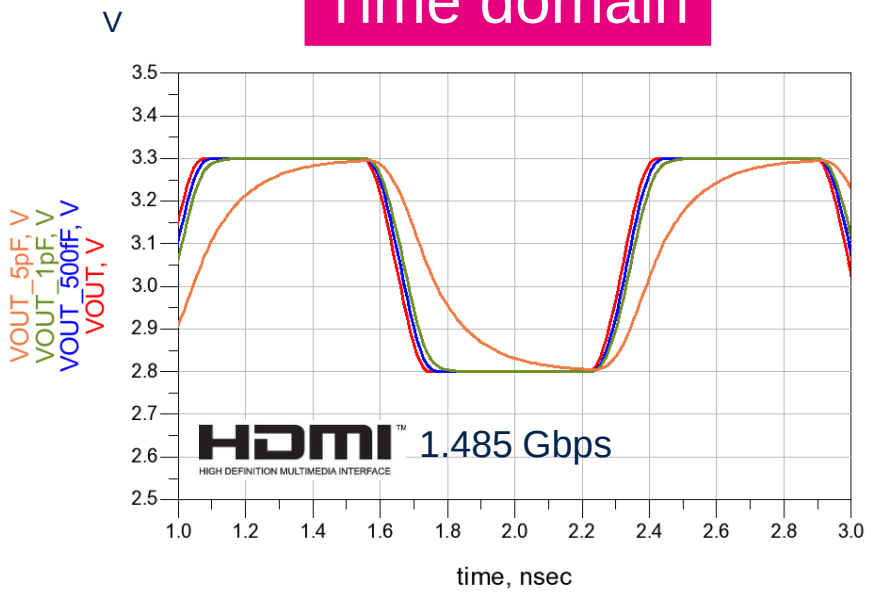
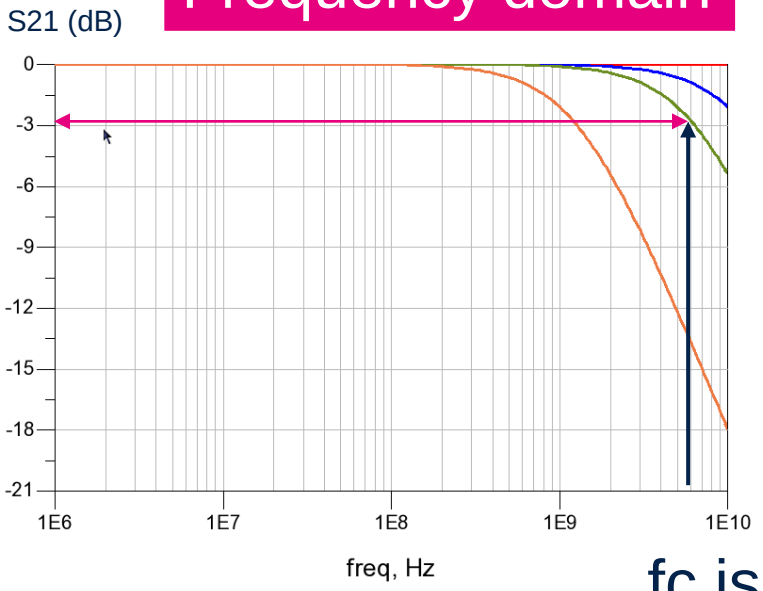
Key parameters capacitance value

- Example of the impact of parasitic capacitance on high-speed signal simulated with discrete capacitance

Time domain



Frequency domain



$$fc = \frac{1}{\pi t_r}$$

fc is high enough to comply with HDMI 1.485 Gbps

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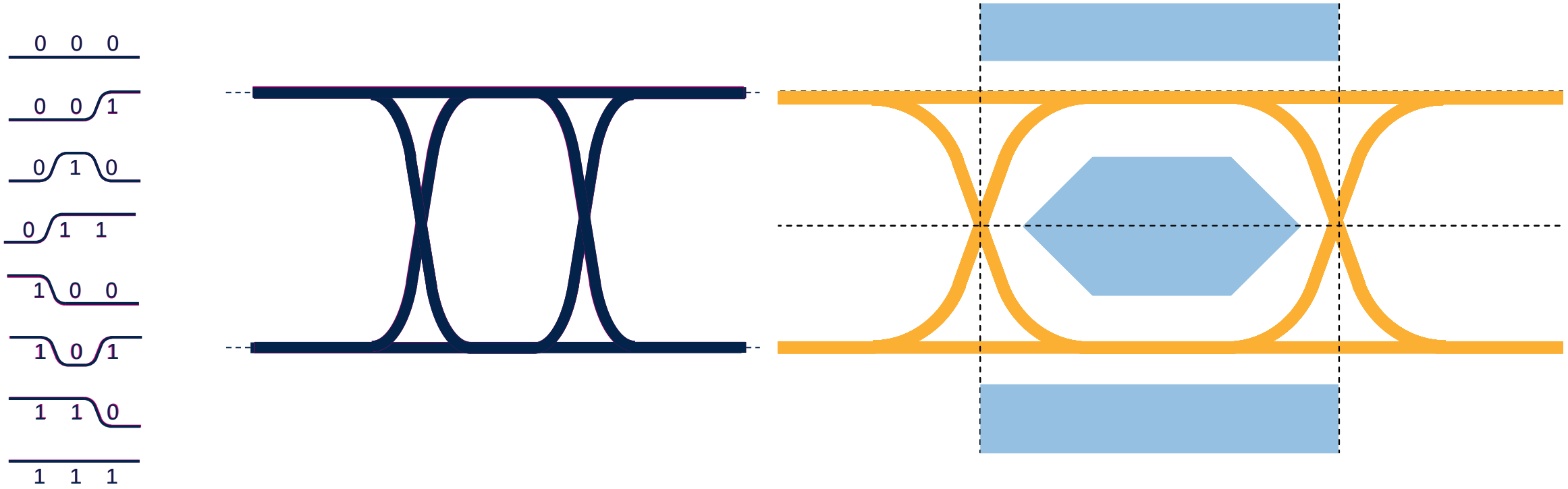
Eye diagram
what is an eye diagram?



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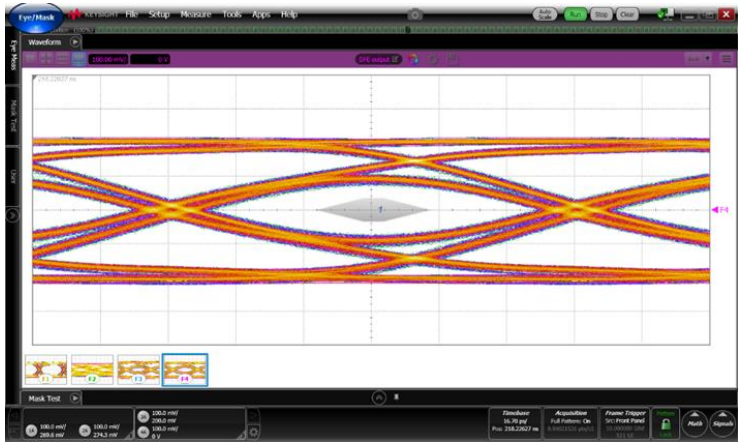
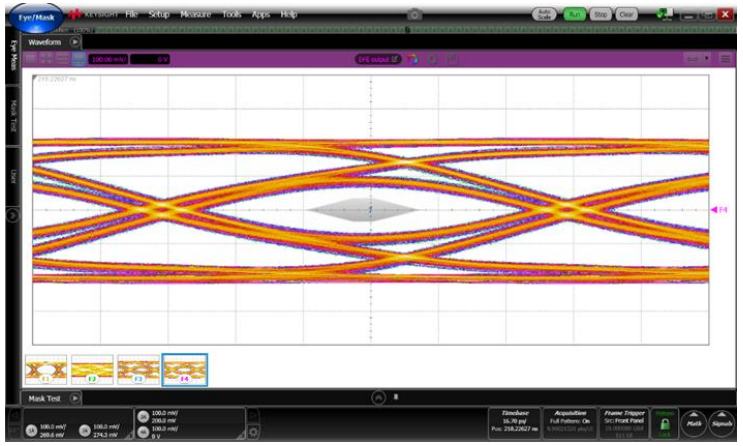
Impact on data-lines eye diagram integrity

- USB 3.1 Gen2 mask at 10.0 Gbps per channel
  (Type-C connector, reference cable, EQ with DC=6dB and DFE)



Line without HSP053-4M5



Line with HSP053-4M5

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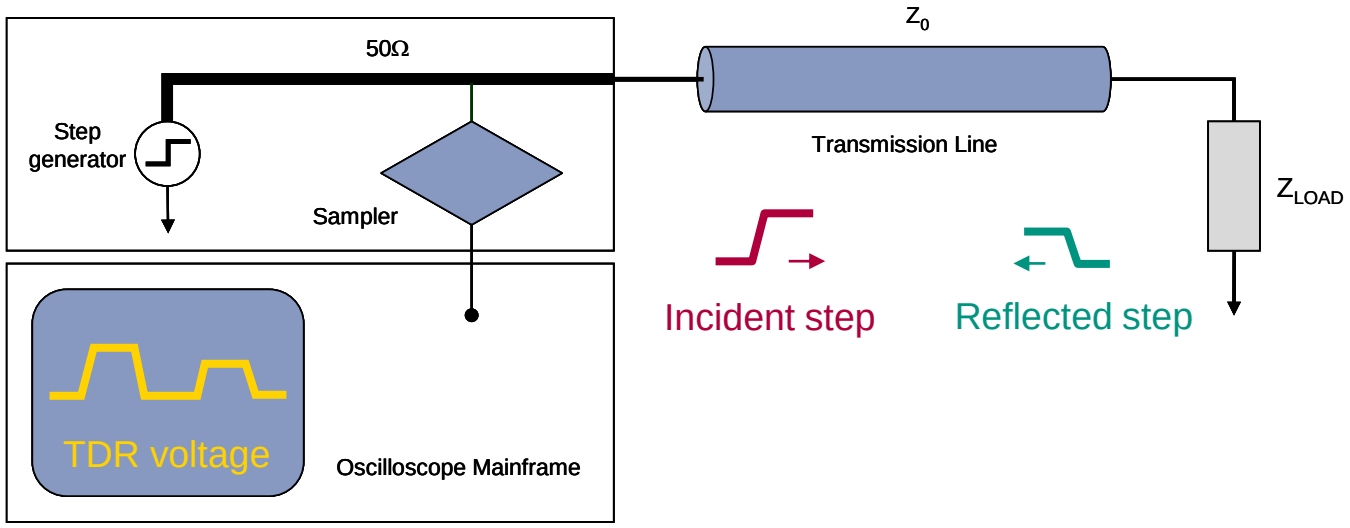
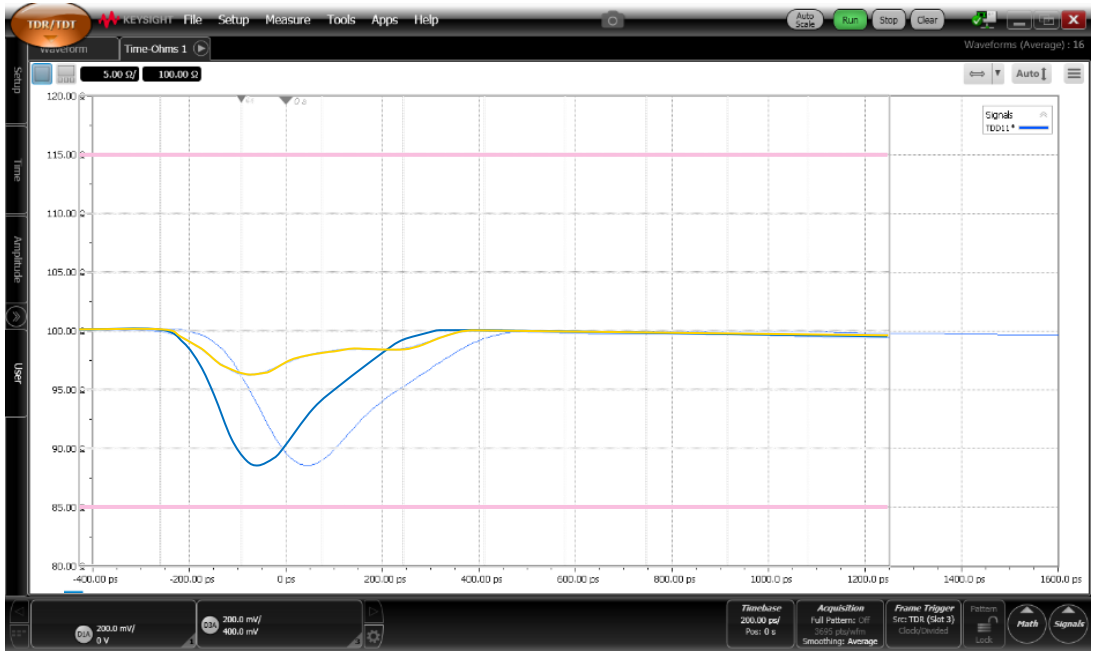
Impact on data-lines time domain reflectometer impedance



TDR with 200ps pule rise time impedance of 100Ω line without / with HSP053-4M5



HDMI 2.0b TDR specification : 100Ω ±15Ω

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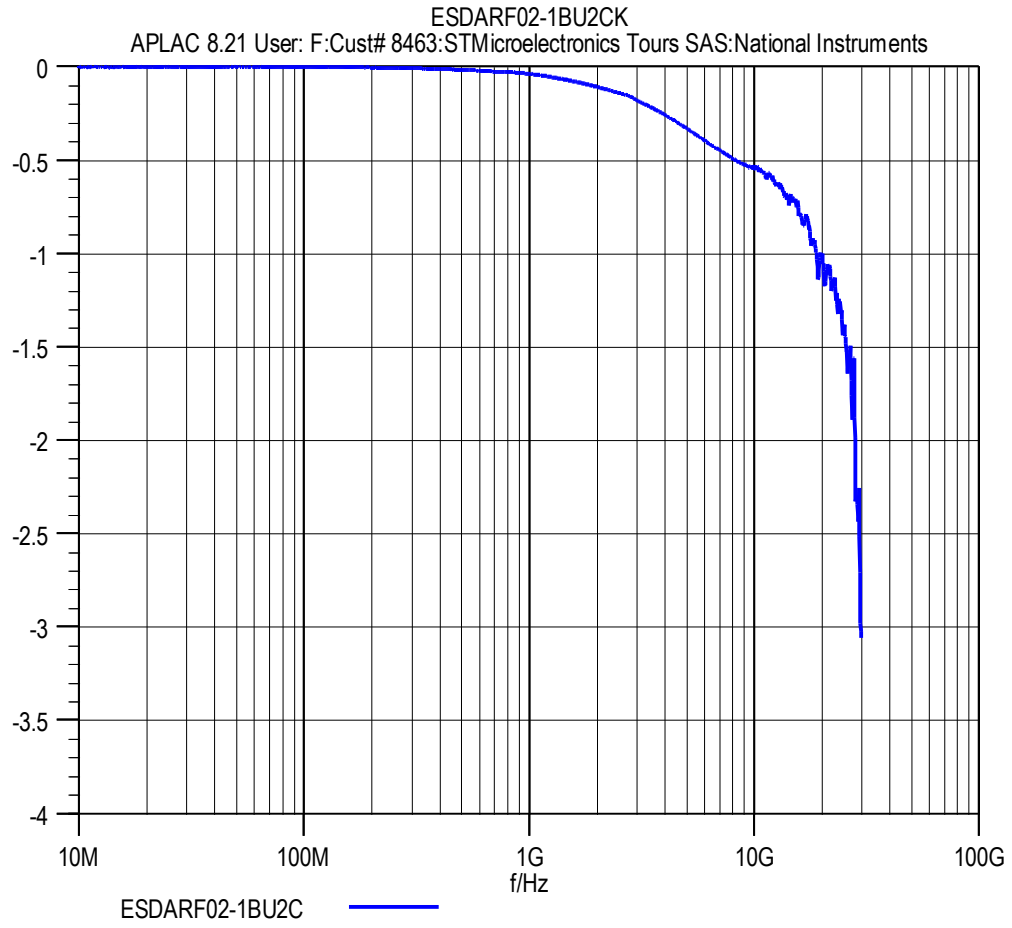
Impact on RF signal S21 attenuation

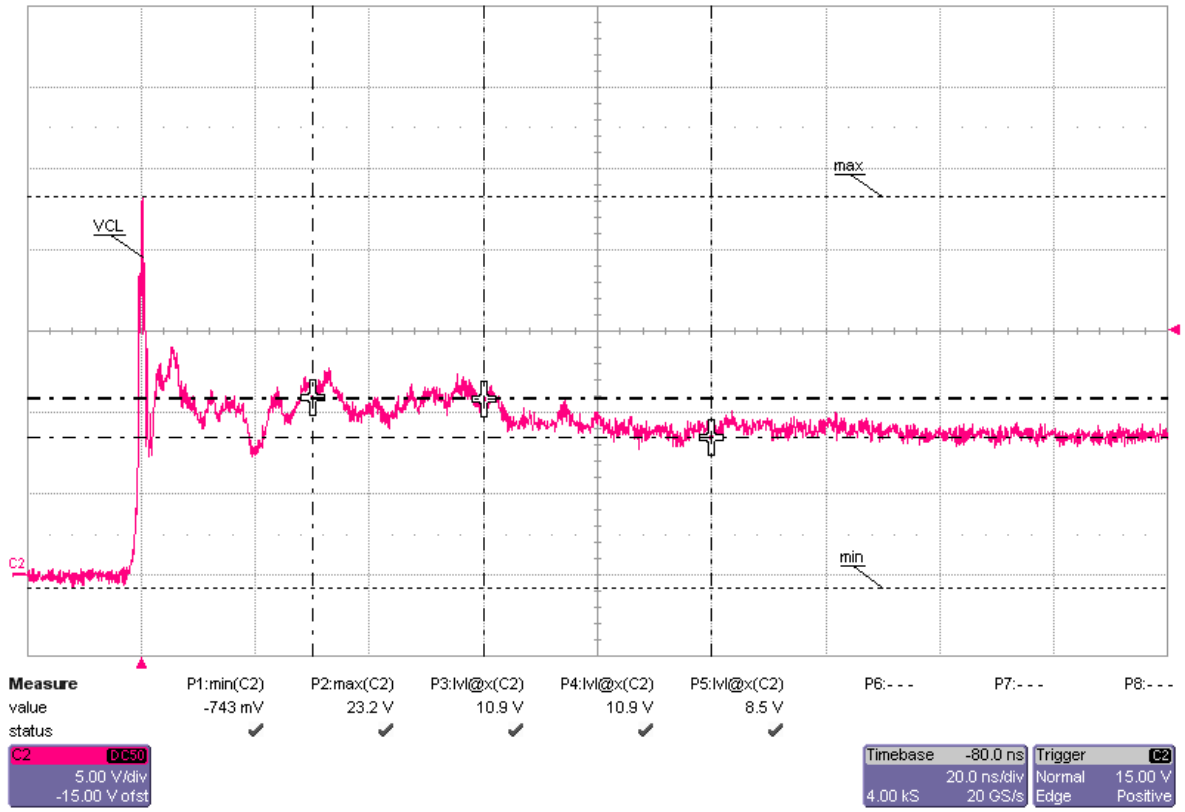
- ESDARF02-1BU2CK S21
  - 30 GHz at -3 dB
  - 8 GHz at -0.5 dB
- Negligible impact major frequencies for teleco
  - FM radio : 87.5 MHz - 108.0 MHz
  - Numerical TV : 400 MHz – 900 MHz
  - Cellular phones : 700 MHz … 4.7 GHz
  - GNSS : 1.6 GHz
  - Bluetooth : 2.4 GHz
  - Sub-GHz industrial : 400 MHz … 1.1GHz
  - WiFi : 2.4 / 5.0 GHz



ESD protection
IEC 61000-4-2 +/-8kV ESD response

- IEC 61000-4-2 response of ESD051-1BF4 :
  - First peak : 23V (low energy, CDM like)
  - 30ns clamping : 11V (clamping voltage)

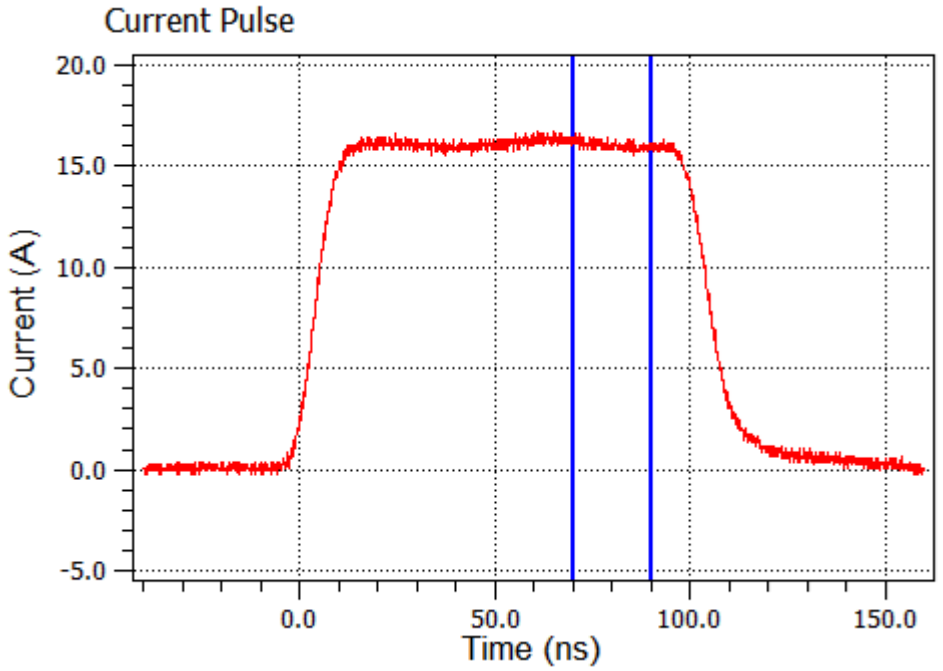
ESD051-1BF4 +8kV IEC 61000-4-2 response



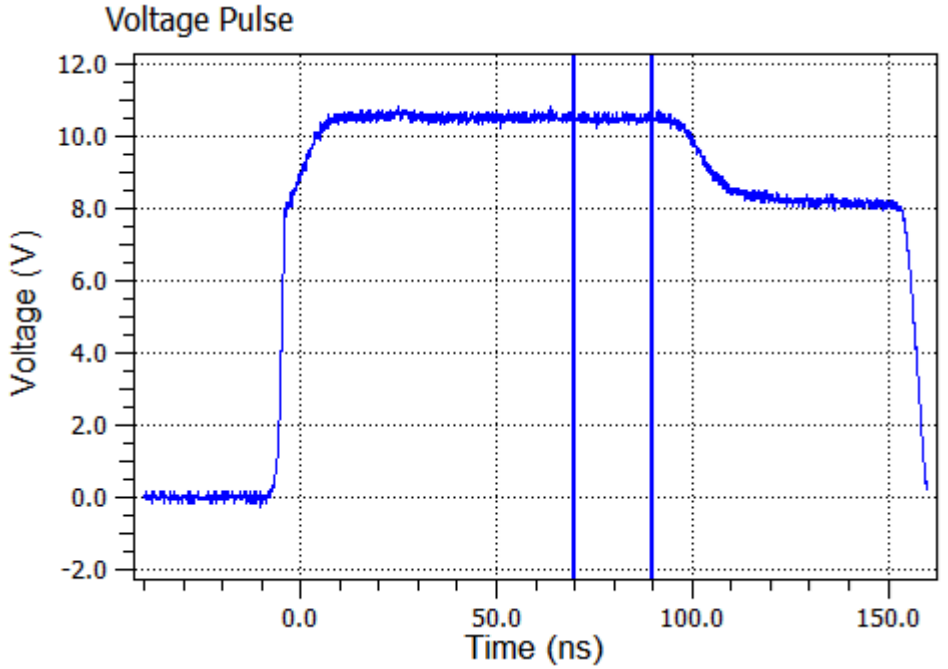
ESD protection
Transmission Line Pulse

- IEC 61000-4-2 8 kV 30 ns clamping voltage ↔ TLP* 16 A 100 ns 70 - 90% voltage

Injected current :
16A – 100ns square current



Measured voltage on 70% – 90% windows on ESD051-1BF4 : 10.5V



*ANSI / ESD STM5.5.1-2014

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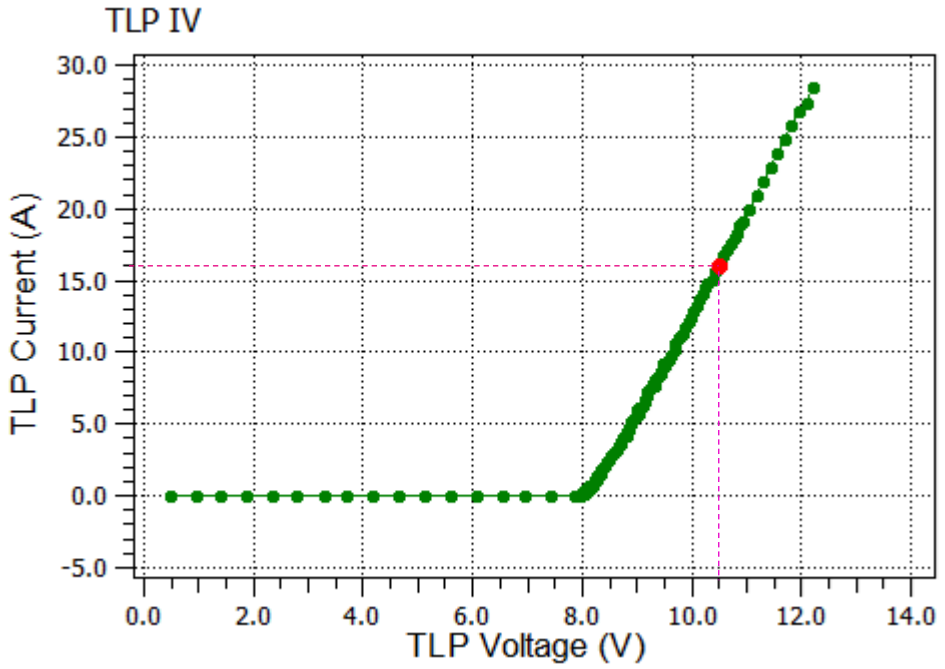
ESD protection
Transmission Line Pulse I/V curve

- I/V TLP* curve is done with several pulses

ESD051-1BF4 TLP* I/V curve



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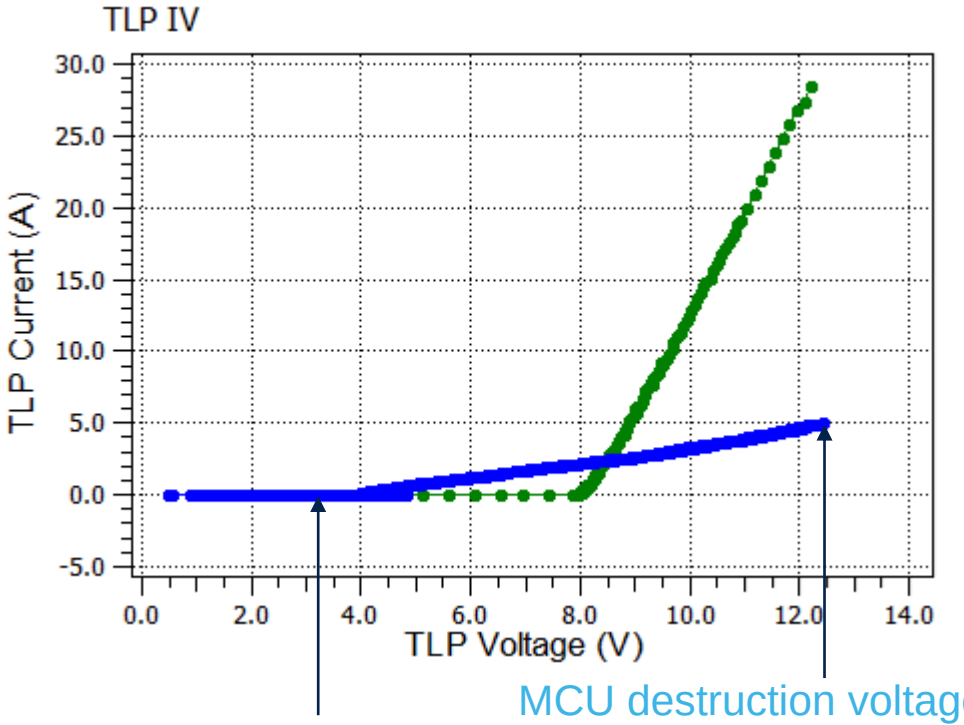
*ANSI / ESD STM5.5.1-2014

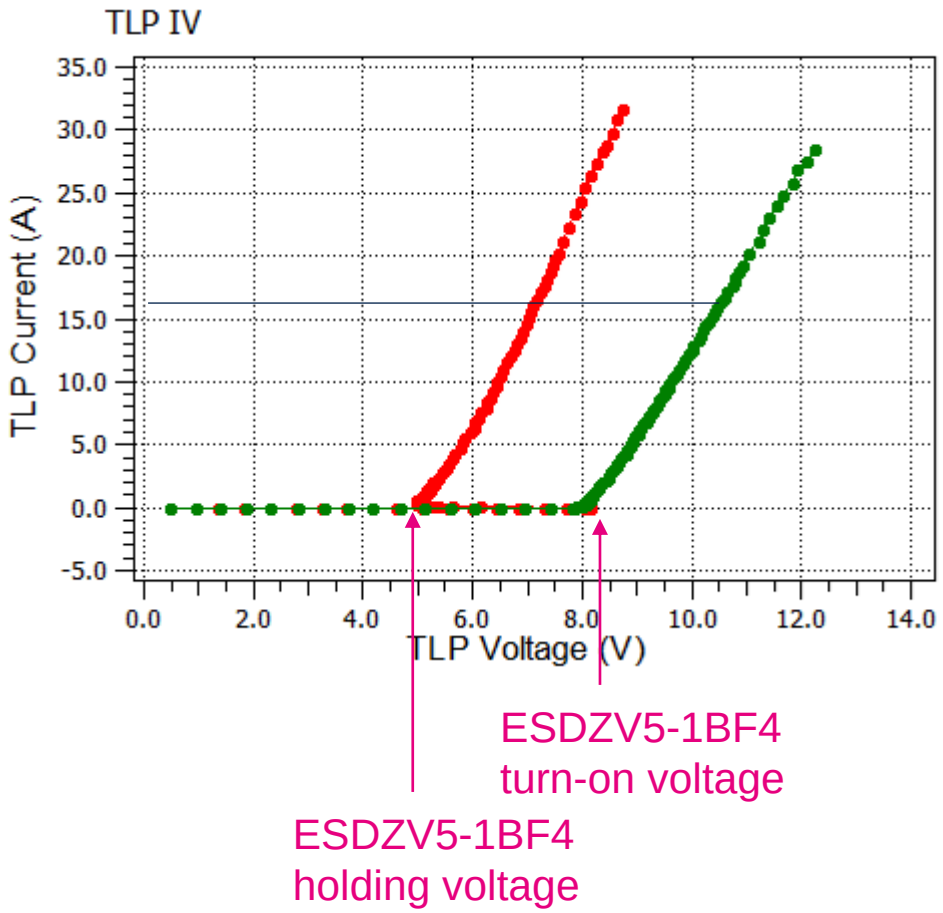
System-efficient ESD design methodology

- TLP input current shared between high performance MCU FT input and ESDA5-1BF4
- High performance MCU + ESDA5-1BF4 robustness reach more than 8kV IEC 61000-4-2
  - Even if, ESD5-1BF4 clamping voltage > High Performance MCU FT input AMR
- ESD051-1BF4
  - 11V clamping voltage at +8kV ESD 61000-4-2
- High Performance MCU FT input
  - 3.6 V max operating
  - 2 kV HBM ESD
  - 250 V CMD ESD
  - 5.5 V AMR



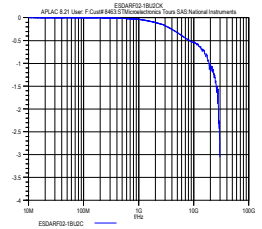
Snap-back protections system integration

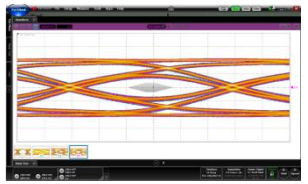
- Snap-back protection (ESDZV5-1BF4) clamping voltage lower than standard protection (ESD051-1BF4) clamping voltage
- Protected line DC voltage MUST be lower than holding voltage
  - To avoid protection latch-up
    i.e. continuous leakage current flowing into the protection



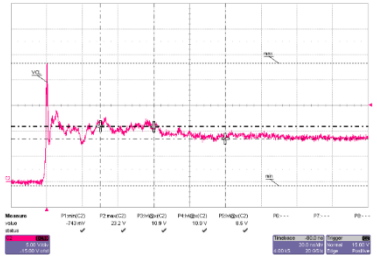
Recap
basics of ESD protection

- Transparency :
  - Capacitance must be in-line with application bandwidth / data rate





- Efficiency :
  - VRM must be slightly higher than maximum line voltage
    To obtain a low clamping voltage



- System integration of snap-back protection :
  - Holding voltage must be higher than DC voltage

AN5241, Fundamentals of ESD protection at system level

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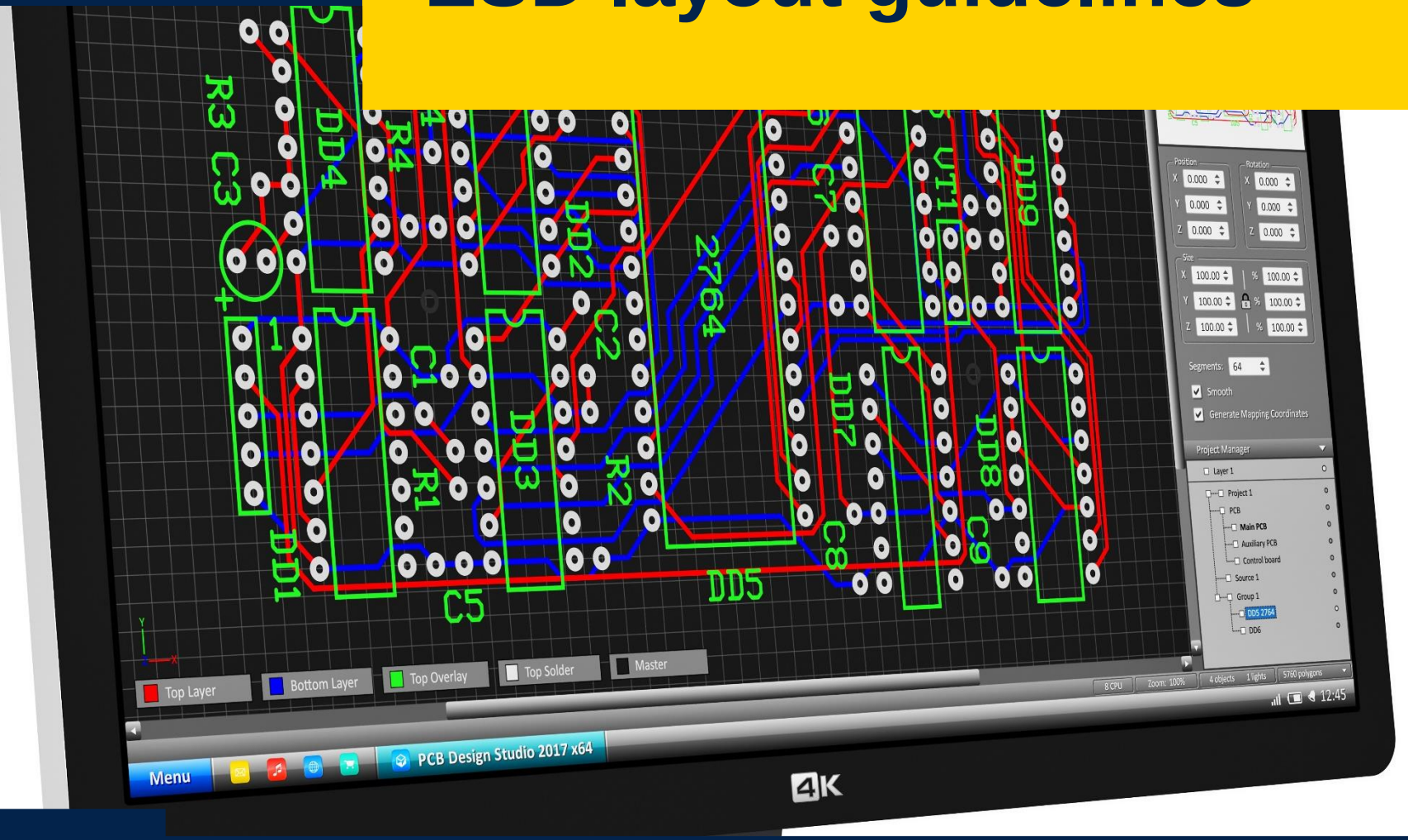
ESD layout guidelines



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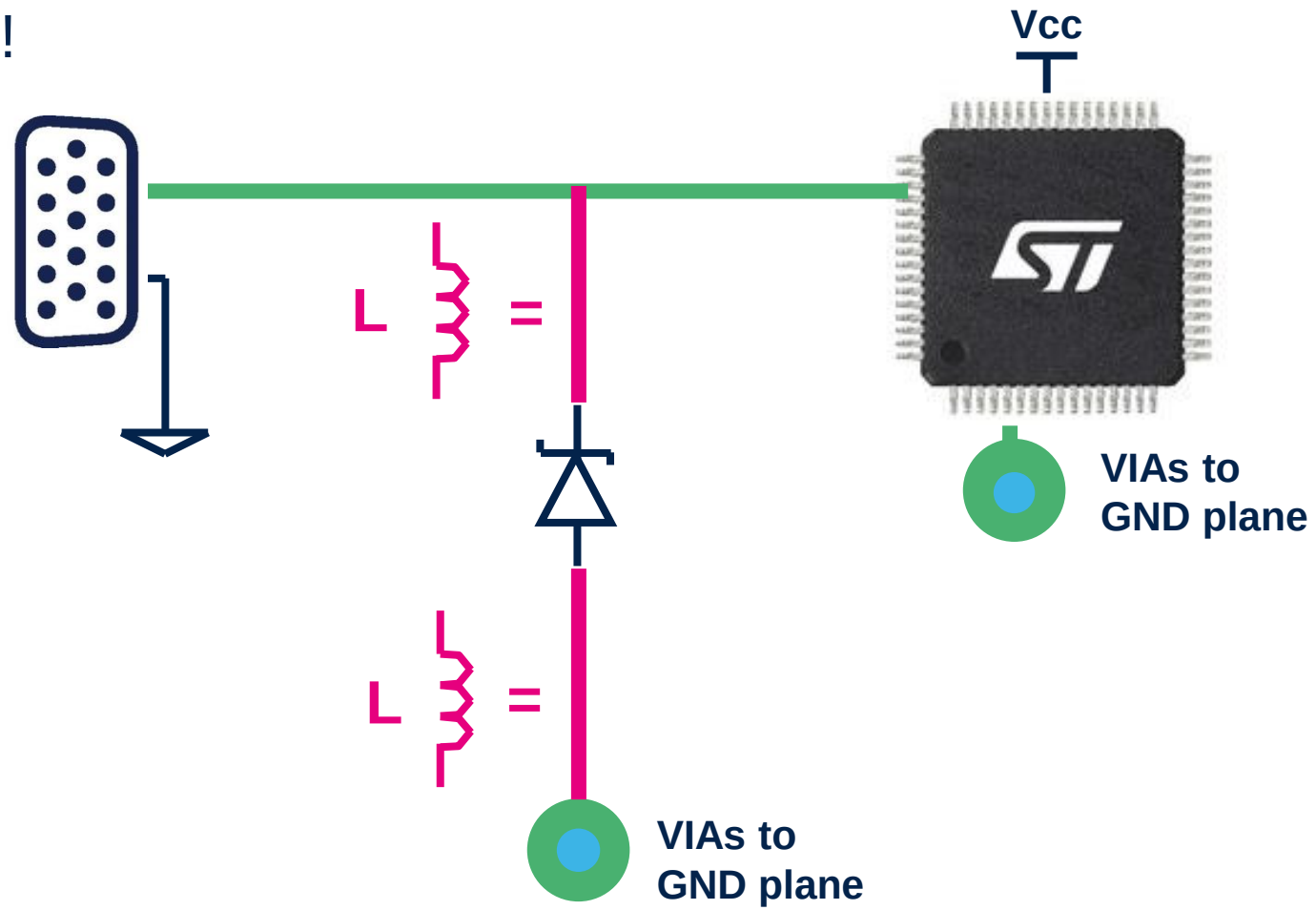
ESD robustness
PCB layout impact

- PCB Tracks must be under control !
- For protection device length connection of ~1cm from side to side, 35µm copper, 0.5mm wide (microstrip)
- 2 x L = 5 nH !



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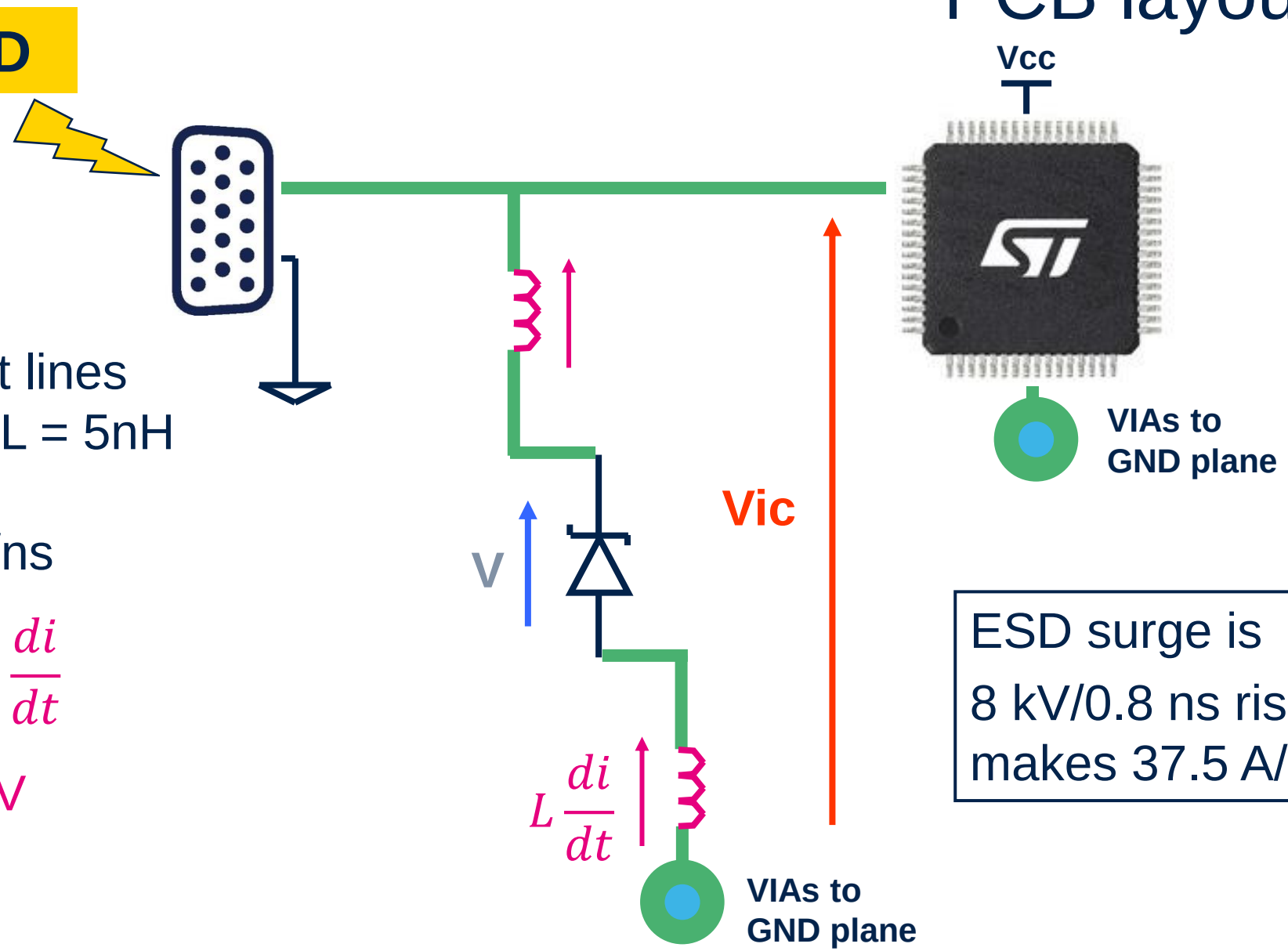
ESD robustness
PCB layout impact

- $L\frac{di}{dt}$



Assuming that lines inductance is L = 5nH

di/dt = 37.5 A/ns

Vic= V + 2 x $L\frac{di}{dt}$

Vic= V + 375 V

ESD surge is

8 kV/0.8 ns rise time, this makes 37.5 A/ns

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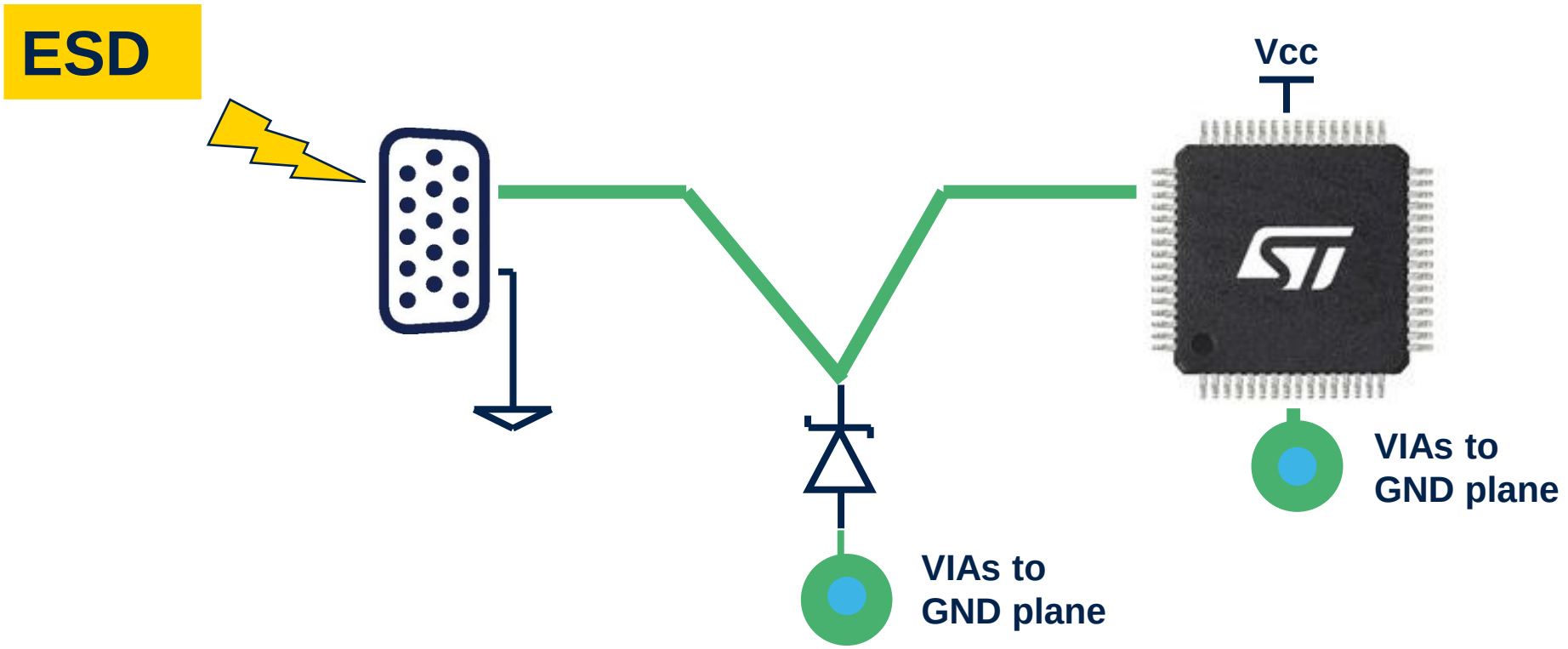
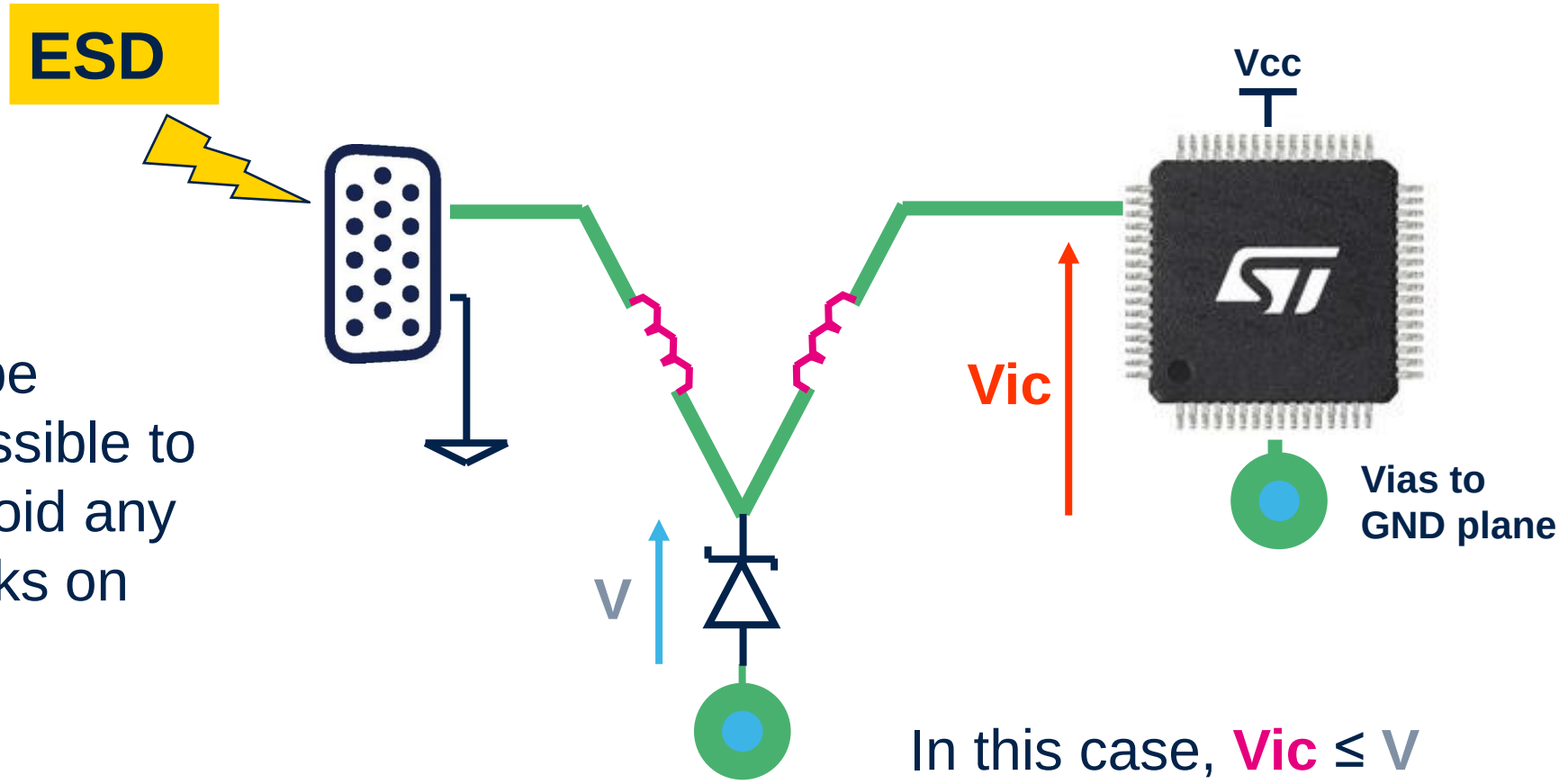
ESD robustness
PCB layout recommendation



VIAs to GND plane as close as possible to the product GND

ESD robustness
PCB layout recommendation

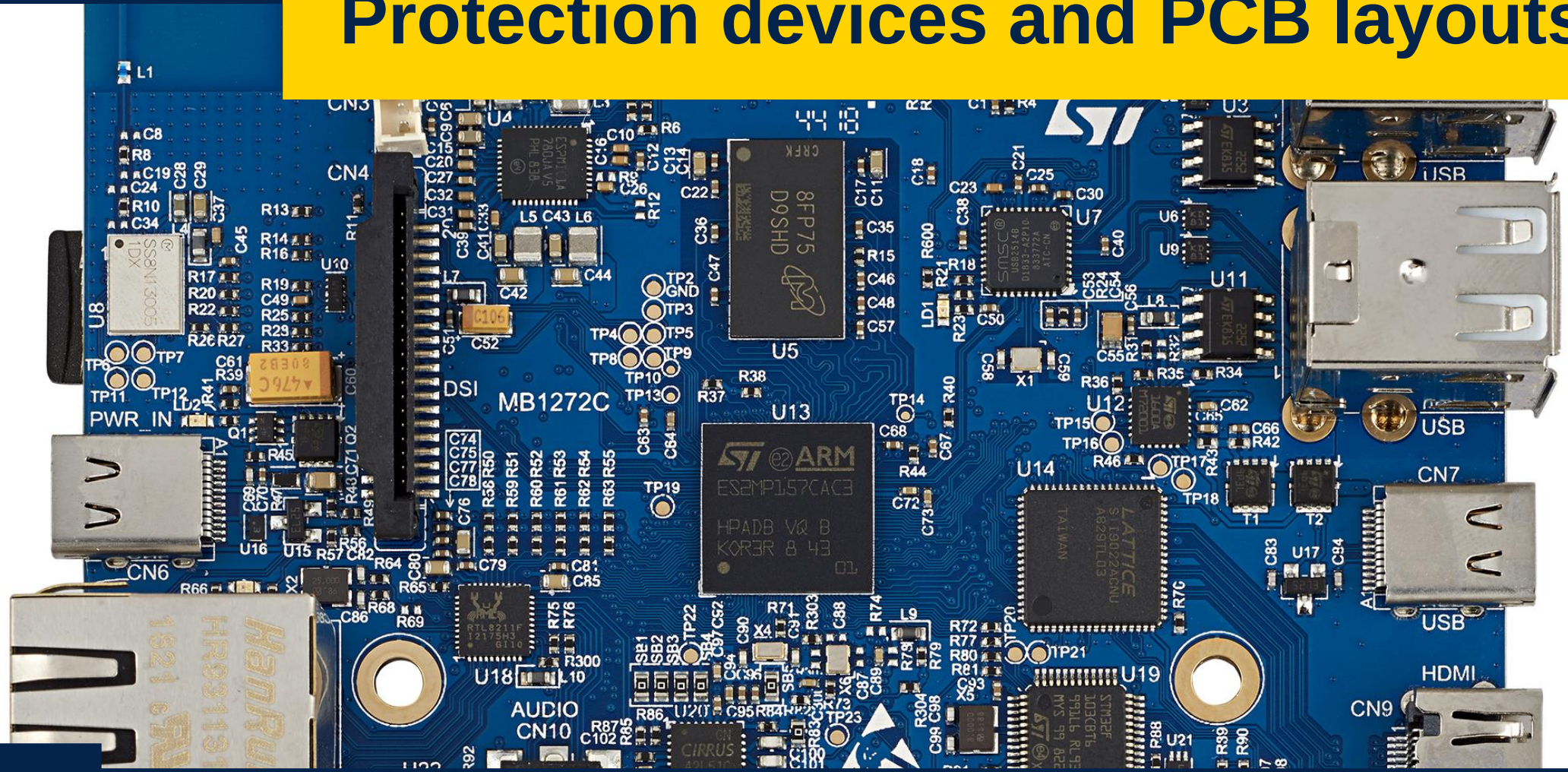
- PCB Layout recommendations in Application note AN1751



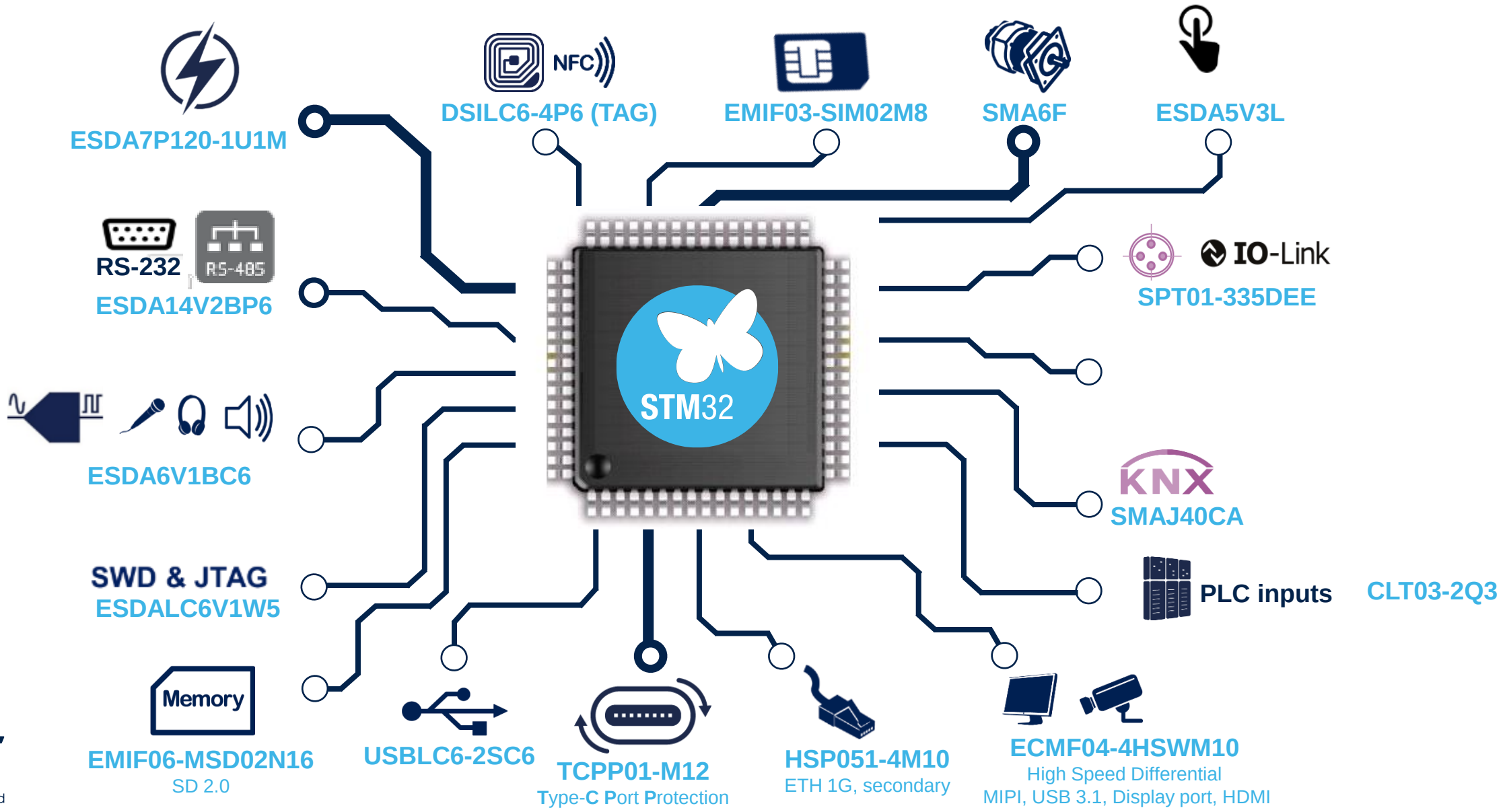
- ESD protection must be placed as close as possible to the ESD source, to avoid any coupling between tracks on the PCB.

In this case, **Vic** ≤ **V**

Application examples
Protection devices and PCB layouts

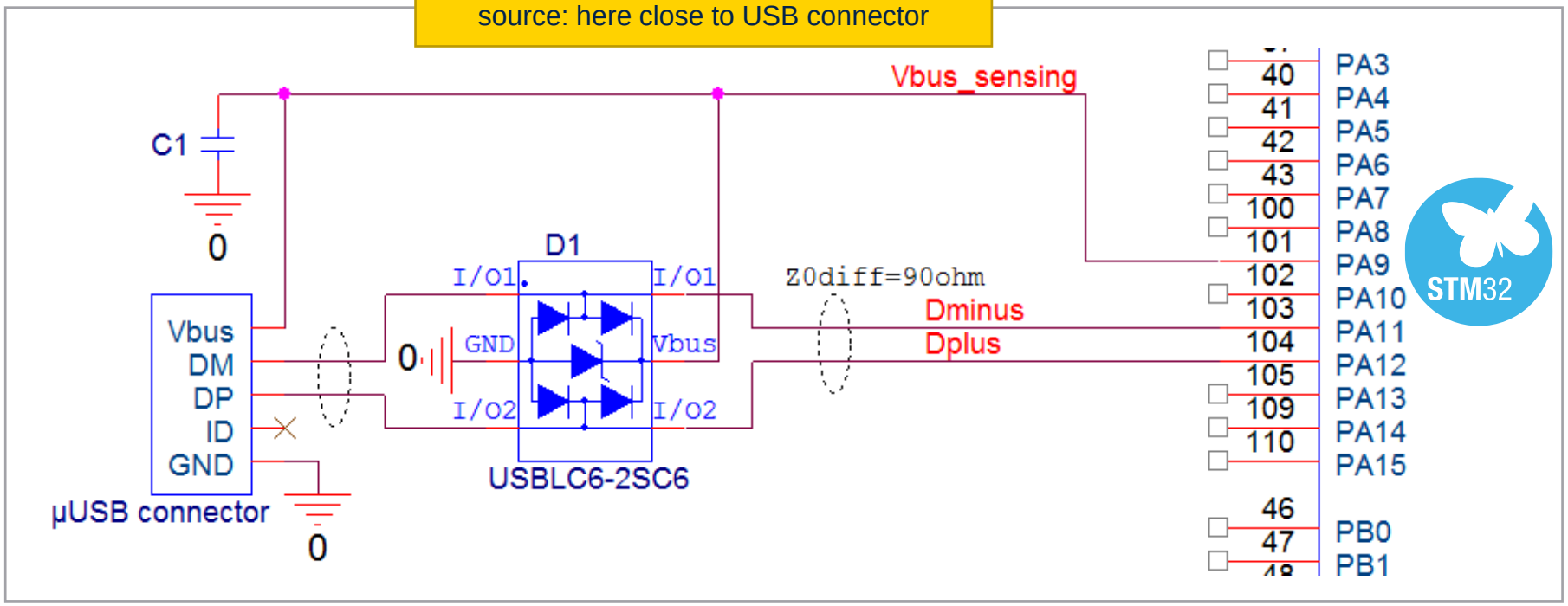


Protections and filters around MCUs



Usb 2.0 full speed without OTG

DESIGN TIP:
Place the ESD protection close to ESD source: here close to USB connector



Reuse gerber file
STM32L4R9I-EVAL

USBLC6-2SC6

SOD323-6L

- Compliant with USB 2.0 eye diagram
- ESD robustness: ± 15 kV contact discharge IEC61000-4-2

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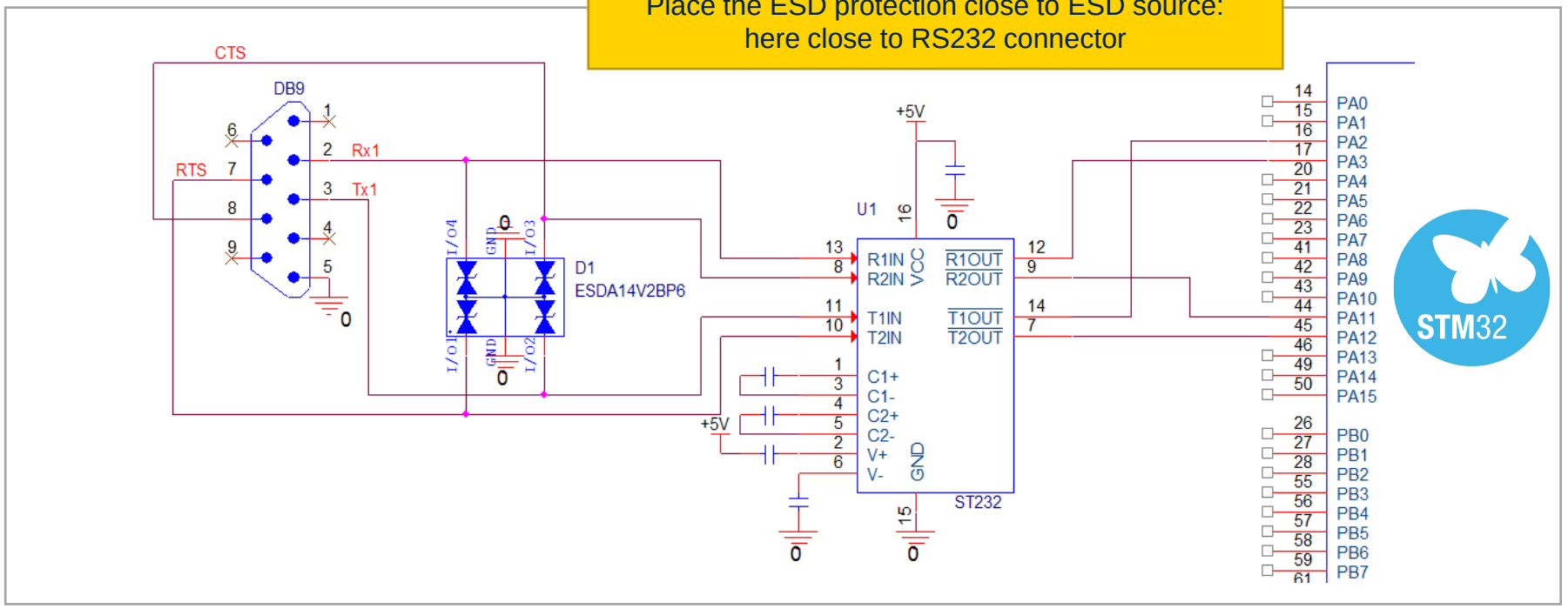
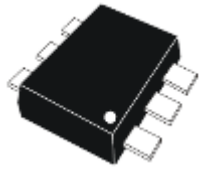
RS232

DESIGN TIP:
Place the ESD protection close to ESD source:
here close to RS232 connector



Reuse gerber file
STM32L4R9I-EVAL

ESDA14V2BP6



SOT666-6L

- Low capacitance, 4-line, bi-directional ESD protection
- ESD protection as per IEC61000-4-2 Level 4: ± 8kV contact

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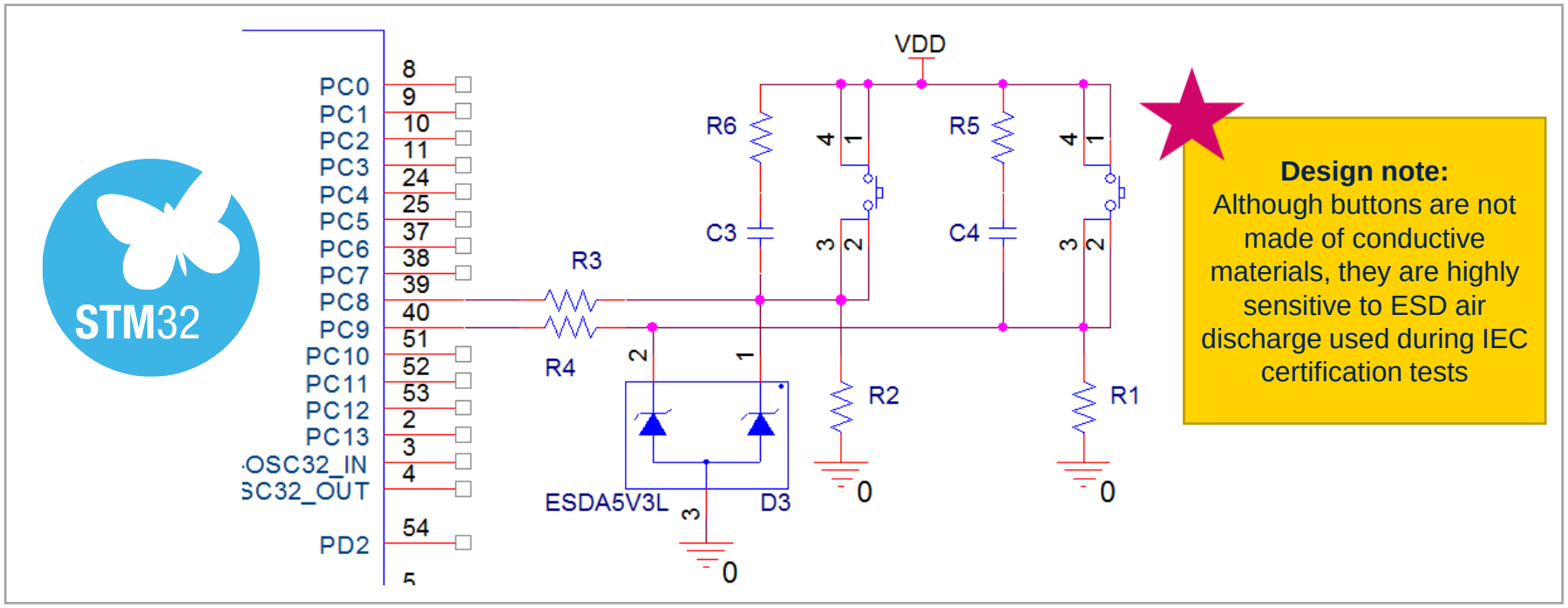
User button
MCU GPIO input



Design note:
Although buttons are not made of conductive materials, they are highly sensitive to ESD air discharge used during IEC certification tests

Reuse gerber file
STM32L4R9I-EVAL

ESDA5V3L

SOT23-3L

- PCB space saving: 2 diodes array
- ESD robustness: ± 30 kV contact discharge IEC61000-4-2

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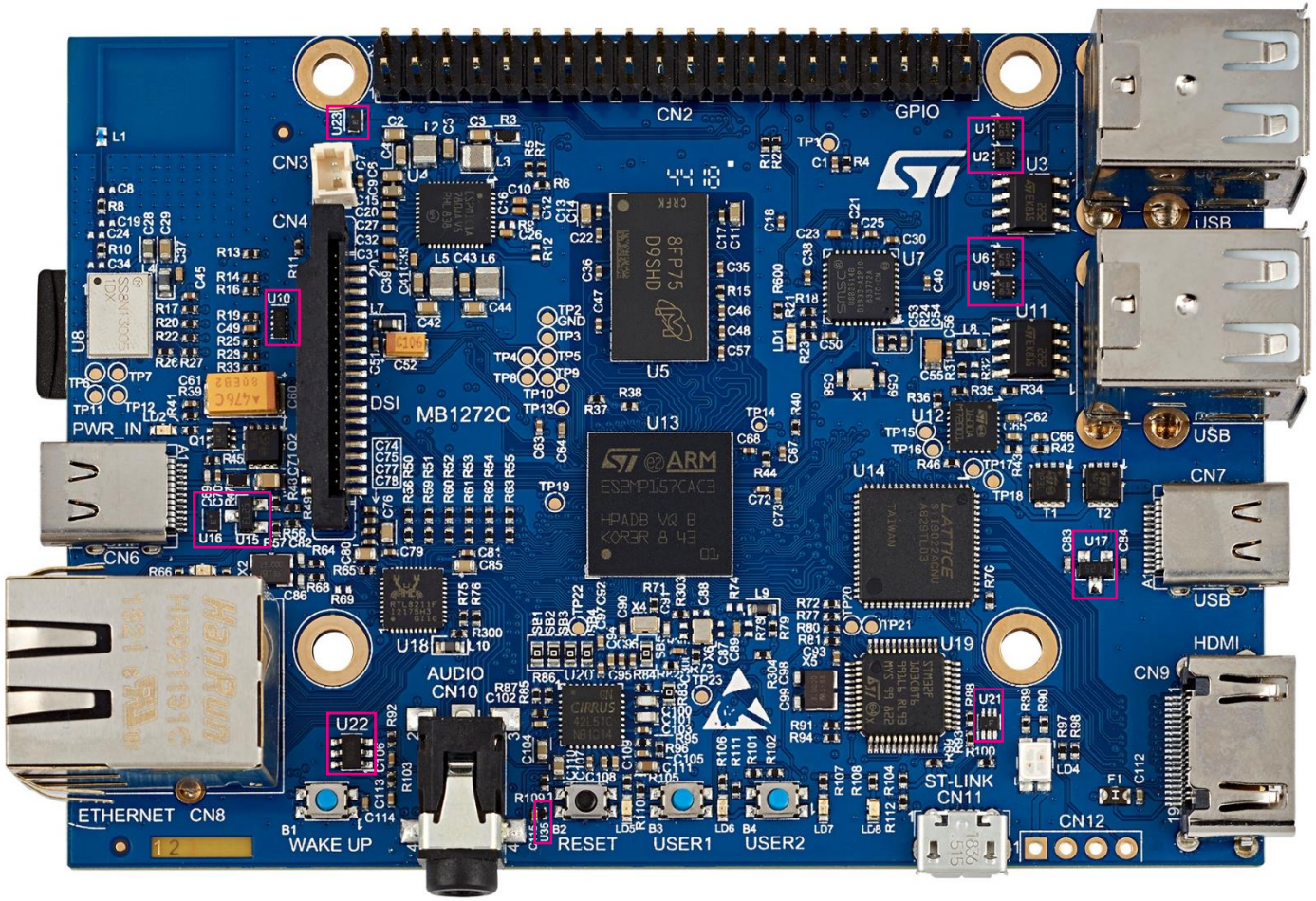
STM32MP1-DK2 discovery
ESD protections and filters

MORPHO CONNECTOR
ESDA7P120-1U1M
5V Vin

MICRO SD CARD
HSP051-4M10 (x2)
SDMMC dataline

USB Type-C Power Delivery
ESDA7P120-1U1M, ESDA25L
VBUS
CC1, CC2

ETHERNET
HSP053-4M5



USB HOST x2 (Dual USB Type-A)
ESDA7P120-1U1M (x2), ECMF02-2AMX6 (x2)
VBUS
DP, DM

USB HOST x2 (Dual USB Type-A)
ESDA7P120-1U1M (x2), ECMF02-2AMX6 (x2)
VBUS
DP, DM

USB Type-C DRP (Source Only)
ESDA7P120-1U1M, ESDA25L, ECMF02-2AMX6
VBUS
CC1, CC2
DP, DM

HDMI
ECMF04-4HSWM10 (x2), ESDALC6V1-5M6
TMDS datalines
CEC, I2C, HPD

AUDIO
ESDA6V1BC6: 4-line ESD protection
OUTA, OUTB, MIC IN

USER BUTTONS
ESDALC6V1-1U2

ST-LINK USB CONNECTOR
USBLC6-2P6
DP, DM, VBUS

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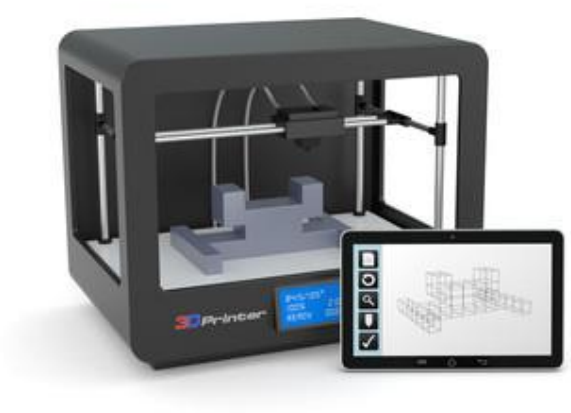
STM32MP1

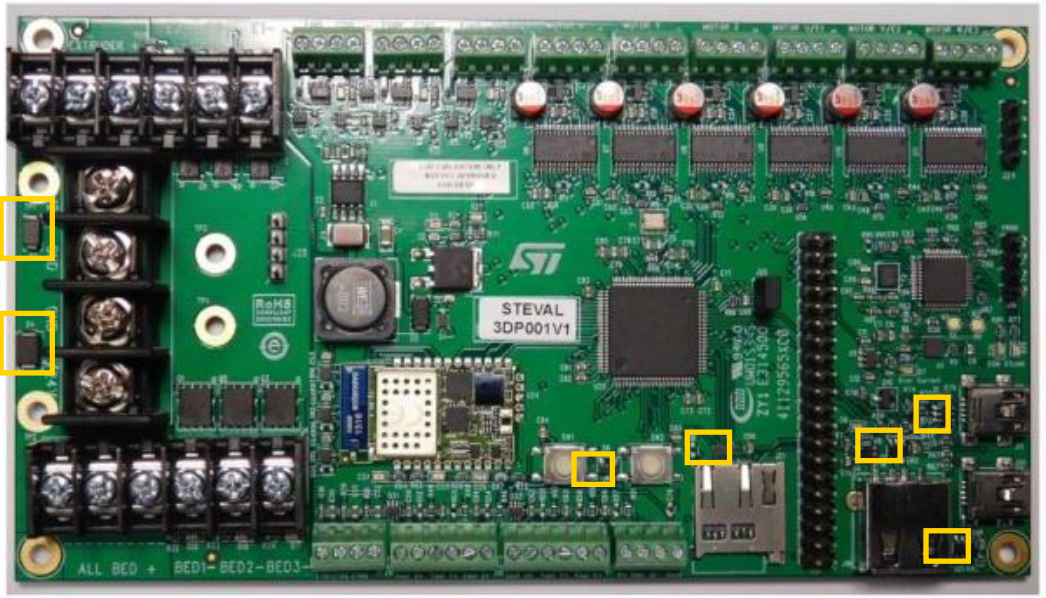
Electronic boards must be protected
3D printer control board



SMAJ12A

SMBJ24A

EMIF06-MSD02N16



ESDA5V3L

3x USBLC6-2SC6

- Protections on the application PCB
  - Power lines → surge protection : IEC 61000-4-5
  - Connector
  - Button
  - SD card

ESD protections for system: IEC 61000-4-2

  - Integrated on all ICs → ESD protection for manufacturing is JEDEC HBM

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Resources
application notes and videos

- AN5241, Fundamentals of ESD protection at system level
- AN4871, USB Type-C protection and filtering
- AN5121, HDMI ESD protection and signal conditioning products for STBs
- AN3353, IEC 61000-4-2 standard testing
- AN2689, Protection of automotive electronics from electrical hazards, guidelines for design and component selection
- AN1826, TRANSIENT PROTECTION SOLUTIONS: Transil™ diode versus Varistor
- AN5241 : Fundamentals of ESD Protection
- Video - ESD Protection: why and how to protect microcontrollers efficiently

ST protection finder mobile app

- ST PROTECTION FINDER is an application available for Android™ and iOS™ that allows you to explore ST's TVS product portfolio.
  - Parametric or series search engine
  - Efficient part number search engine

豌豆荚 Wandoujia SnapPea

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GET IT ON Google Play

Download on the App Store

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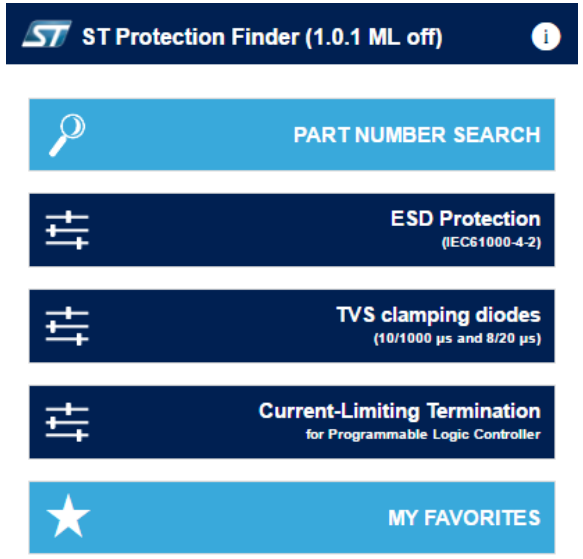
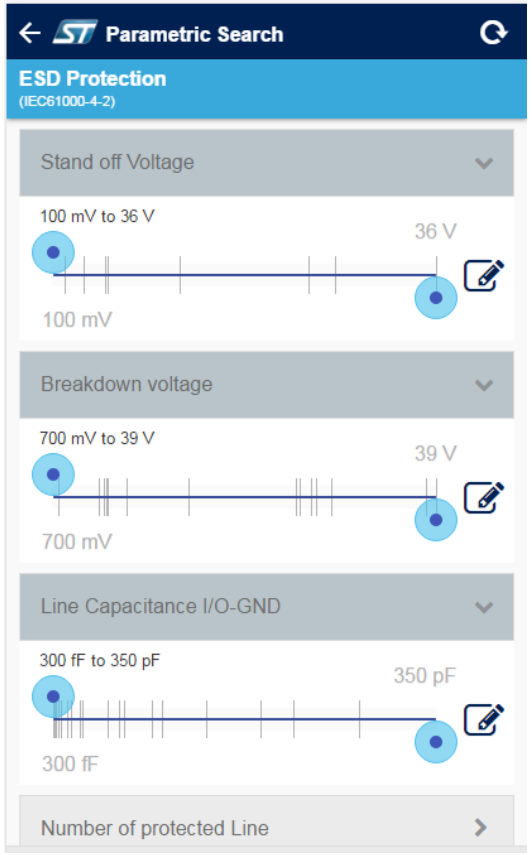
4 steps to discover ST's portfolio

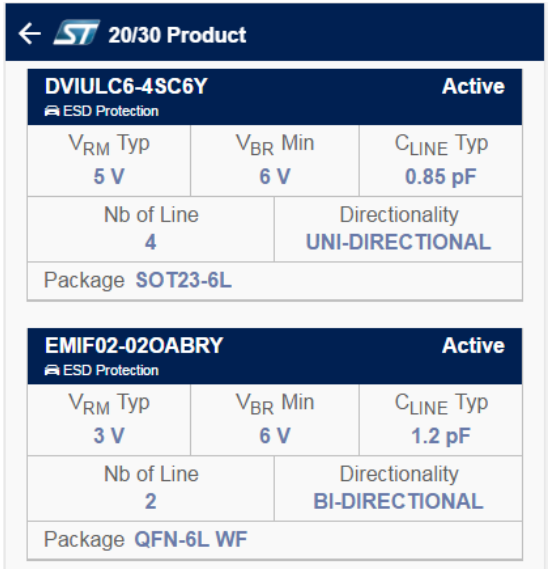
1 - OPEN application



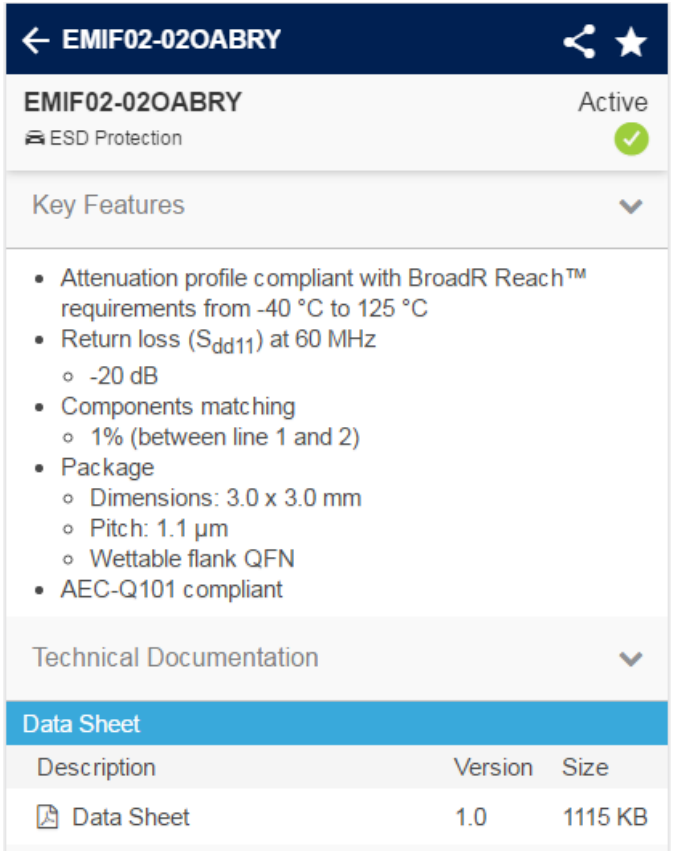
2-SELECT parameter



3- CHOOSE product



4- GET datasheet



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Thank you

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