MAX38909

2A High-Performance nMOS LDO Linear Regulator

General Description

The MAX38909 is a fast transient response, high PSRR nMOS linear regulator that delivers up to 2A of load current.

The regulator supports a wide input supply range from 0.9V to 5.5V, and BIAS voltage range from 2.7V to 20V to provide wider supply options in a variety of applications. ±1% output accuracy is maintained over line, load, and temperature variations, requiring only 300mV of input-to-output headroom at full load for a good PSRR. The output voltage can be adjusted to accommodate customers that desire to specify a single LDO in the BOM for multiple voltage rails.

The output voltage on the MAX38909 is programmed to a value in the range of 0.6V to 5.0V by using two external feedback resistors.

The LDO is fully protected from damage by internal circuitry that provides programmable inrush current limiting, output overcurrent limiting, reverse-current limiting, and thermal overload protection.

The MAX38909 is offered in 14-pin, 3mm x 3mm TDFN and 5 x 3 bump, 0.4mm pitch WLP packages.

Applications

- FPGAs and DSPs
- Medical, Audio, and Instrumentation
- Server Microcontrollers
- Portable Cameras
- PLCs
- Base Stations

Benefits and Features

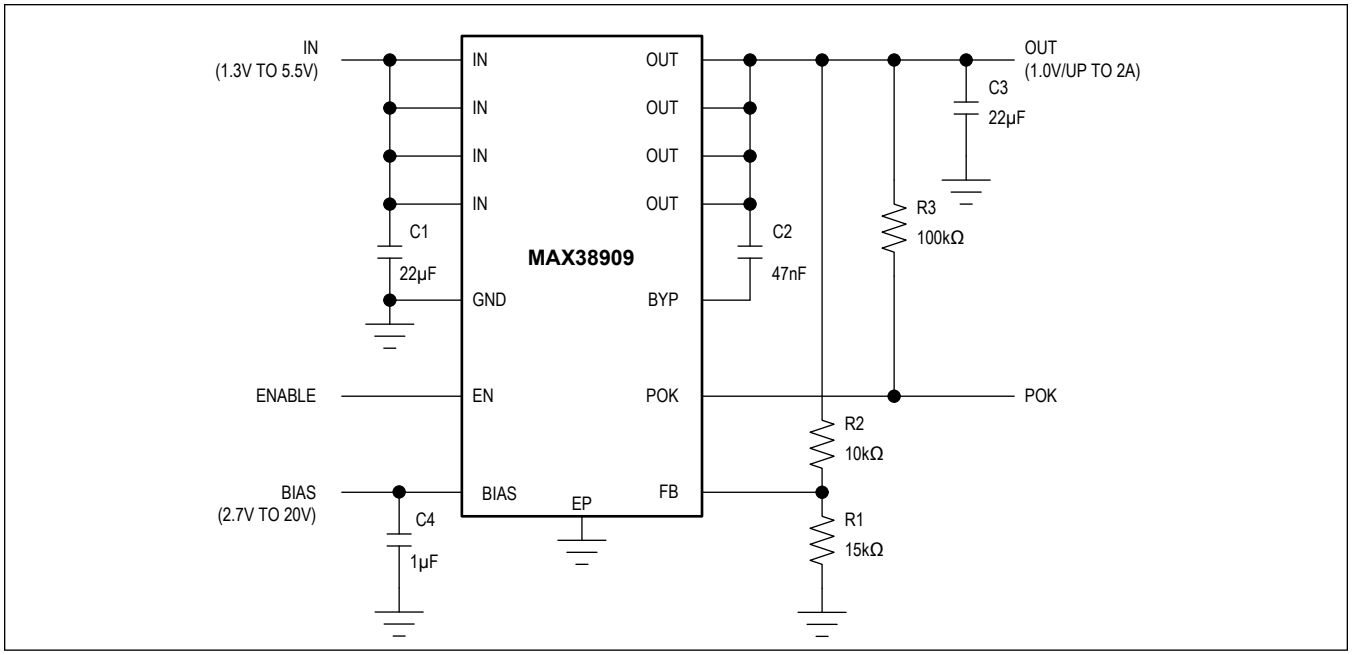
- Delivers Flexible Operating Range
  - 0.9V to 5.5V Input Voltage Range
  - 2.7V to 20V BIAS Voltage Range
  - 0.6V to 5.0V Programmable Output Voltage
  - 2A Maximum Output Current
  - 27mV Dropout at 2A Load Current
  - 1.6mA Operating BIAS Supply Current
- Reduces Noise and Improves Accuracy
  - ±1% DC Accuracy Over Load, Line, and Temperature
  - 15mV 2A Load Transient Excursion
  - 52dB IN PSRR at 10kHz at 300mV Input-to-Output Headroom
- Enables Ease-of-Use and Robust Protection
  - Stable with 10µF (Minimum) Output Capacitance
  - Programmable Soft-Start Rate
  - Overcurrent and Overtemperature Protection
  - Output-to-Input Reverse Current Protection
  - Power-OK Status Pin
- Reduces Size, Improves Reliability
  - 14-Pin (3mm x 3mm) TDFN and 5 x 3 Bump, 0.4mm Pitch WLP Packages
  - -40°C to +125°C Operating Temperature

***Ordering Information* appears at end of data sheet.**

19-100950; Rev 1; 11/20

maxim integrated™

Typical Application Circuit



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Absolute Maximum Ratings

IN, FB, OUT, BYP, POK to GND ..... -0.3V to +6V
BIAS to GND ..... -0.3V to +22V
EN to GND.....-0.3V to V_{BIAS} + 0.3V
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4mW/°C, T_A = +70°C)..... 1951.2mW
WLP (derate 16.2mW/°C, T_A = +70°C).....1312mW
Operating Junction Temperature Range.....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

14 TDFN

Package Code	T1433+2C
Outline Number	21-0137
Land Pattern Number	90-0063
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	54°C/W
Junction to Case (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

WLP

Package Code	N151C2+1
Outline Number	21-100372
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θJA)	61.65°C/W
Junction to Case (θJC)	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 1.5V, V_{OUT} = 1.0V, V_{BIAS} = 10V, T_J = -40°C to +125°C, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 1nF, unless noted otherwise.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by output accuracy, $V_{OUT} < V_{IN} - V_{DO}$	0.9		5.5	V

Electrical Characteristics (continued)

(V_{IN} = 1.5V, V_{OUT} = 1.0V, V_{BIAS} = 10V, T_J = -40°C to +125°C, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 1nF, unless noted otherwise.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bias Voltage Range	V_{BIAS}			2.7		20	V
Input Undervoltage Lockout	V_{IN_UVLO}	V_{IN} rising, 60mV hysteresis		0.35	0.45	0.55	V
Bias Undervoltage Lockout	V_{BIAS_UVLO}	V_{BIAS} rising, 100mV hysteresis		2.45	2.55	2.65	V
Output Voltage Range	V_{OUT}	Guaranteed by output accuracy		0.6		5.0	V
Output Capacitance	C_{OUT}	Effective capacitance required for stability and proper operation		10	22		µF
Input Supply Current	I_Q	V_{EN} = 3.6V, V_{BIAS} = 5.0V, I_{OUT} = 0mA			70.5	150	µA
Input Shutdown Current	I_{SD}	V_{EN} = 0V	T_J = +25°C		0.001	1	µA
			T_J = +125°C		1		
Bias Supply Current	I_{BIAS}	V_{EN} = 3.3V, V_{BIAS} = 5.0V, I_{OUT} = 0mA			1.5	4	mA
		V_{EN} = 3.3V, V_{BIAS} = 5.0V, I_{OUT} = 2A			1.6		
	I_{BIAS_SD}	V_{EN} = 0V			0.75	4	µA
Feedback Voltage Accuracy	V_{FB}	I_{OUT} from 10mA to 2A, V_{IN} from V_{OUT} + 0.3V to 5.5V, V_{BIAS} > 2.7V, V_{BIAS} from V_{OUT} + 2V to 20V, V_{OUT} from 0.6V to 5.0V		0.594	0.6	0.606	V
Load Regulation		I_{OUT} from 0.1mA to 2A, C_{BYP} = 47nF			0.05		%
Load Transient		I_{OUT} = 20mA to 2A and 2A to 20mA, di/dt = 1A/µs, C_{OUT} = 3 x 10µF, C_{BYP} = 47nF			15		mV
Line Regulation		V_{IN} from V_{OUT} + 0.3V to 5.5V, I_{OUT} = 1A, C_{BYP} = 47nF			0.04		%/V
Line Transient		V_{IN} = 1.0V to 1.2V to 1.0V, 10V/ms V_{IN} slew rate, I_{OUT} = 2A, V_{OUT} = 0.8V, C_{BYP} = 47nF			4.5		mV
Dropout Voltage (*Note 2*)	V_{DO}	I_{OUT} = 2A, V_{OUT_NOM} = 1.2V	V_{BIAS} = 5.0V, TDFN		36	80	mV
			V_{BIAS} = 5.0V, WLP		27	80	
			V_{BIAS} = 3.3V, TDFN		50	100	
			V_{BIAS} = 3.3V, WLP		43	100	
		I_{OUT} = 2A, V_{OUT_NOM} = 2.5V	V_{BIAS} = 5.0V, TDFN		44		
			V_{BIAS} = 5.0V, WLP		36		
		I_{OUT} = 2A, V_{OUT_NOM} = 5.0V	V_{BIAS} = 12V, TDFN		36		
			V_{BIAS} = 12V, WLP		27		
Current Limit	I_{LIM}	$V_{OUTS/OUT}$ = 0.9 x V_{OUT_NOM}, V_{IN} - V_{OUT} = 300mV		2.2	2.8	3.4	A

Electrical Characteristics (continued)

(V_{IN} = 1.5V, V_{OUT} = 1.0V, V_{BIAS} = 10V, T_J = -40°C to +125°C, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 1nF, unless noted otherwise.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		I_{OUT} = 0.5A, 10Hz to 100kHz, V_{OUT} = 1.2V	C_{BYP} = 47nF		21.2		μV_{RMS}
IN Power Supply Rejection Ratio	PSRR	V_{IN} - V_{OUT} = 0.3V, I_{OUT} = 1A, C_{OUT} = 4 x 10µF, C_{BYP} = 47nF, V_{BIAS} > 2.7V, V_{BIAS} = V_{OUT} + 2V, T_A = +25°C	f = 1kHz		59		dB
			f = 10kHz		52		
			f = 100kHz		42		
BIAS Supply Rejection Ratio	PSRR	V_{IN} - V_{OUT} = 0.3V, I_{OUT} = 1A, C_{OUT} = 4 x 10µF, C_{BYP} = 47nF, V_{BIAS} = V_{OUT} + 5V, T_A = +25°C	f = 1kHz		90		dB
			f = 10kHz		78		
			f = 100kHz		69		
BYP Capacitor Range	C_{BYP}	Regulator remains stable; guaranteed by design		0.001		0.1	µF
BYP Soft-Start Current	I_{BYP}	From BYP to GND during startup			50		µA
EN Input Threshold	V_{IH}	EN rising			1.0	1.6	V
	V_{IL}	EN falling		0.4	0.9		
EN Input Leakage Current	I_{EN_LK}	V_{EN} from 0V to 5.5V, V_{BIAS} from 8V to 20V	T_A = +25°C	-1	+0.001	+1	µA
			T_J = +125°C		0.01		
POK Threshold		V_{OUT} when POK switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		
POK Voltage, Low	V_{OL}	I_{POK} = 1mA			10	100	mV
POK Leakage Current	I_{POK_LK}	V_{POK} = 5.5V	T_A = +25°C	-1	+0.001	+1	µA
			T_J = +125°C		0.01		
IN Reverse-Current Threshold		V_{OUT} = 1.2V, V_{BIAS} = 10V			700		mA
Thermal Shutdown Threshold		TJ when output turns on/off	T_J rising		165		°C
		T_J when output turns on/off	T_J falling		150		

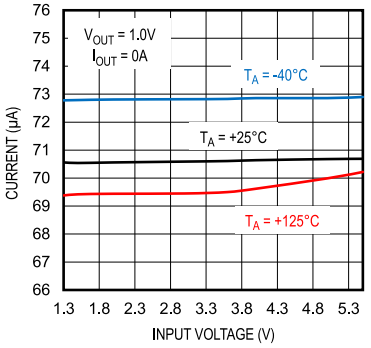
Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

Note 2: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 95% of its nominal value.

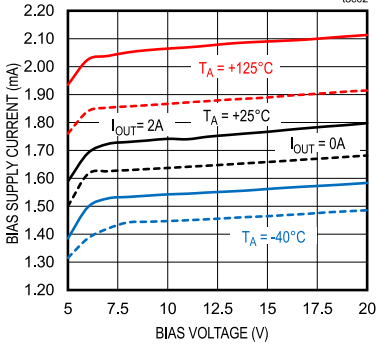
Typical Operating Characteristics

(V_{IN} = 1.5V, V_{BIAS} = 12V, V_{OUT} = 1.0V, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 47nF, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted)

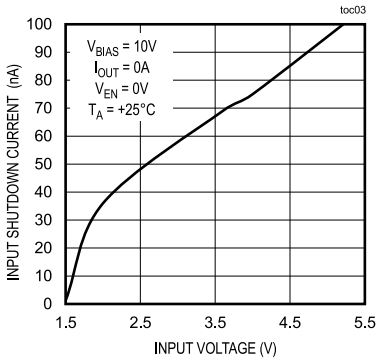
INPUT SUPPLY CURRENT vs INPUT VOLTAGE



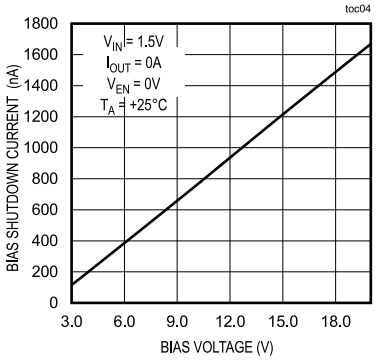
BIAS SUPPLY CURRENT vs BIAS SUPPLY



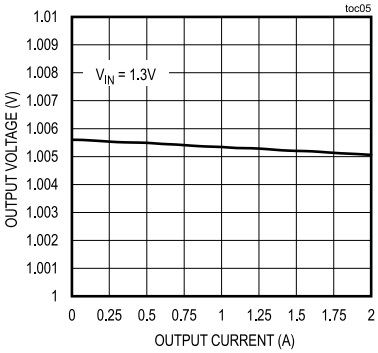
INPUT SUPPLY SHUTDOWN CURRENT vs INPUT VOLTAGE



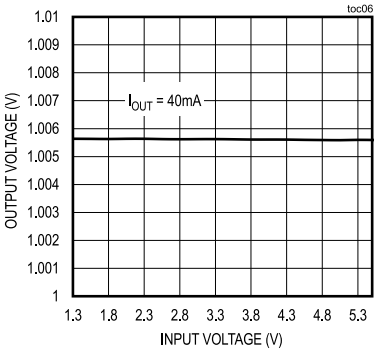
BIAS SUPPLY SHUTDOWN CURRENT vs BIAS VOLTAGE



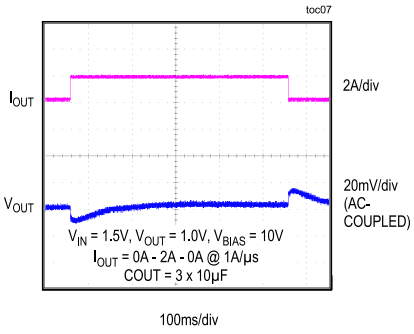
LOAD REGULATION



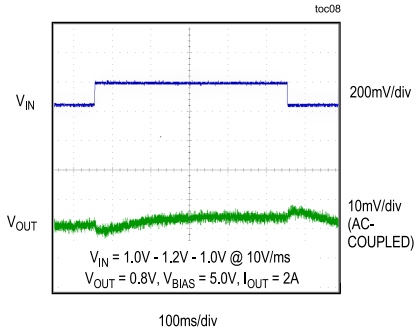
LINE REGULATION



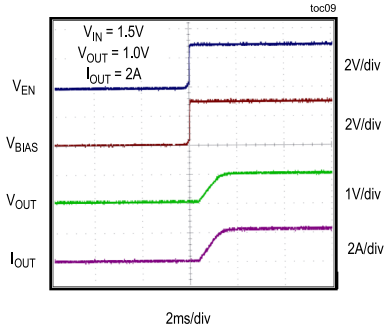
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



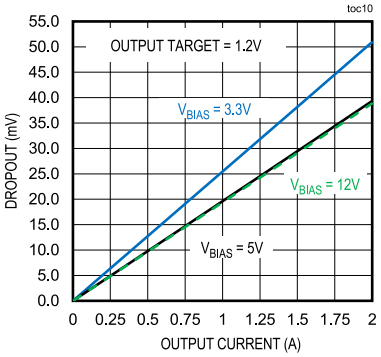
START UP RESPONSE



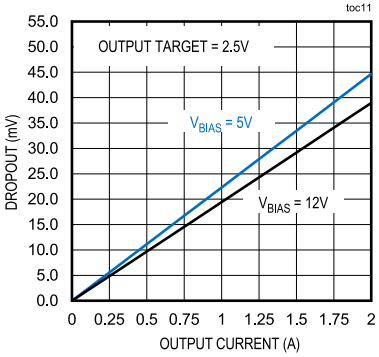
Typical Operating Characteristics (continued)

(V_{IN} = 1.5V, V_{BIAS} = 12V, V_{OUT} = 1.0V, C_{IN} = 22µF, C_{OUT} = 22µF, C_{BYP} = 47nF, C_{BIAS} = 1µF, T_A = +25°C, unless otherwise noted)

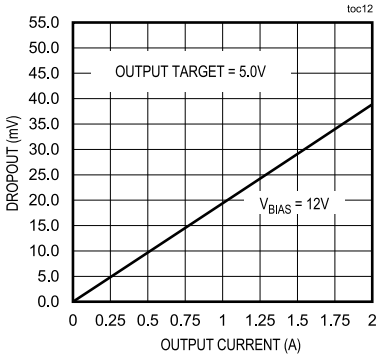
DROPOUT vs LOAD CURRENT



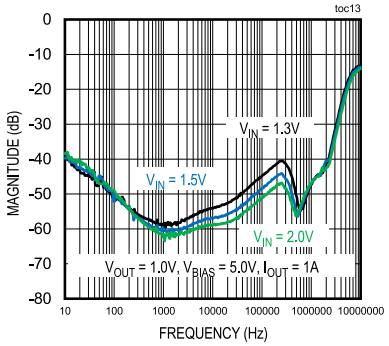
DROPOUT vs LOAD CURRENT



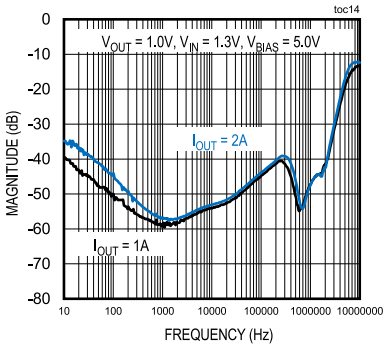
DROPOUT vs LOAD CURRENT



INPUT SUPPLY PSRR vs. FREQUENCY



INPUT SUPPLY PSRR vs. FREQUENCY



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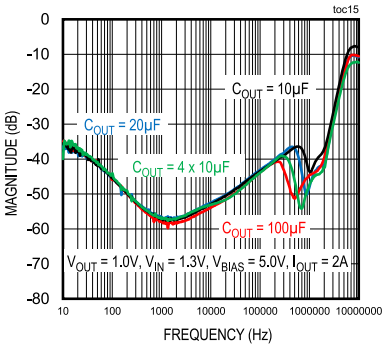

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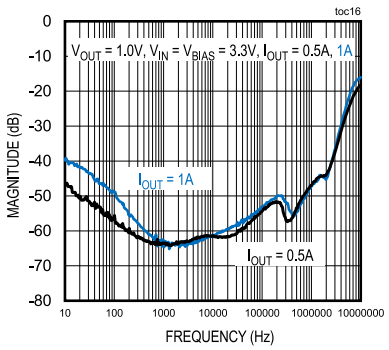
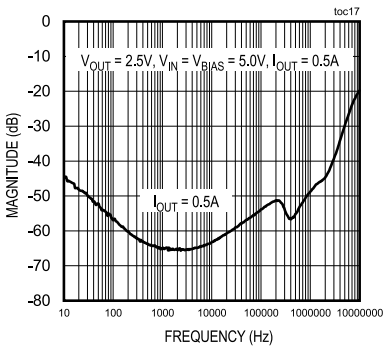
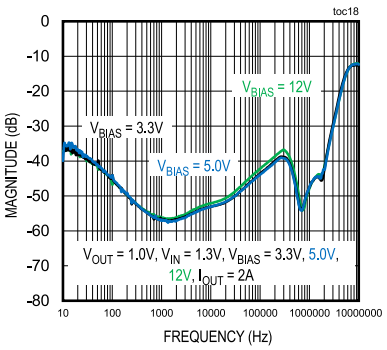


INPUT SUPPLY PSRR vs. FREQUENCY



INPUT SUPPLY PSRR vs. FREQUENCY



Typical Operating Characteristics (continued)

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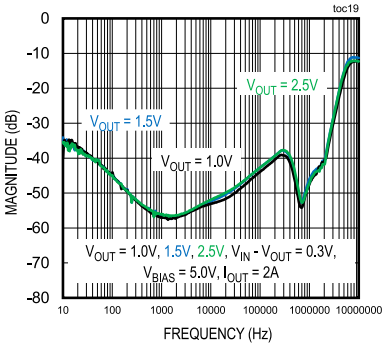
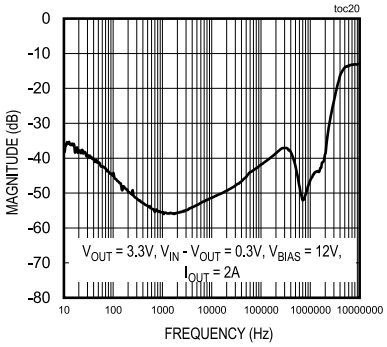
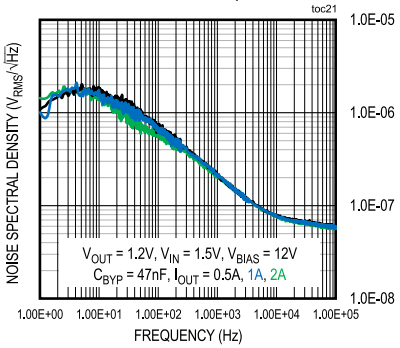


INPUT SUPPLY PSRR vs. FREQUENCY



OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



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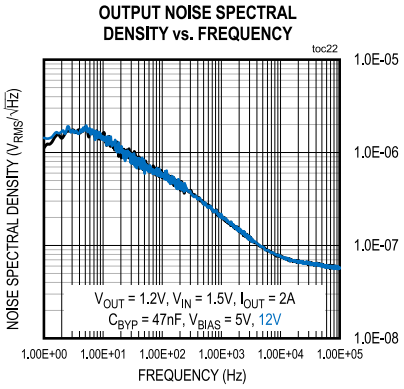

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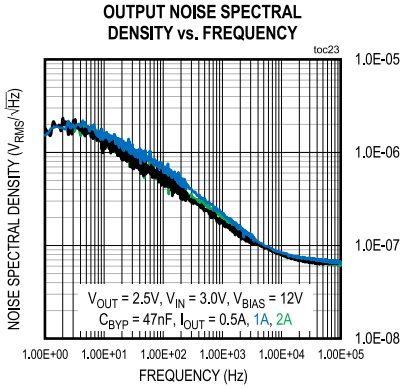
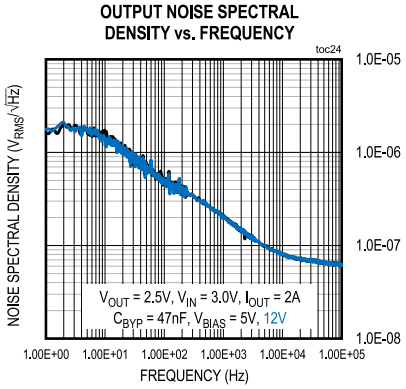
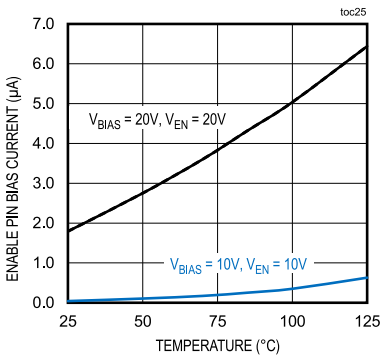


OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY

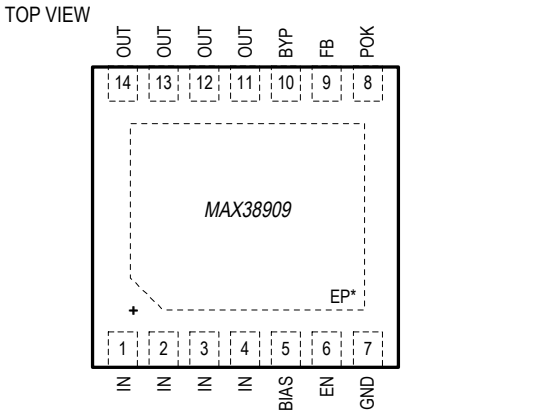


ENABLE PIN BIAS CURRENT vs TEMPERATURE



Pin Configurations

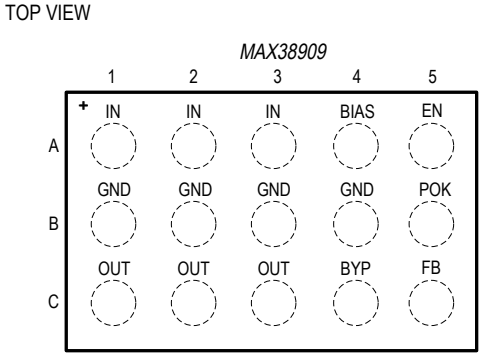
14 TDFN



TDFN-EP
3mm x 3mm

*EP = EXPOSED PAD

WLP



5 x 3, 0.4mm PITCH

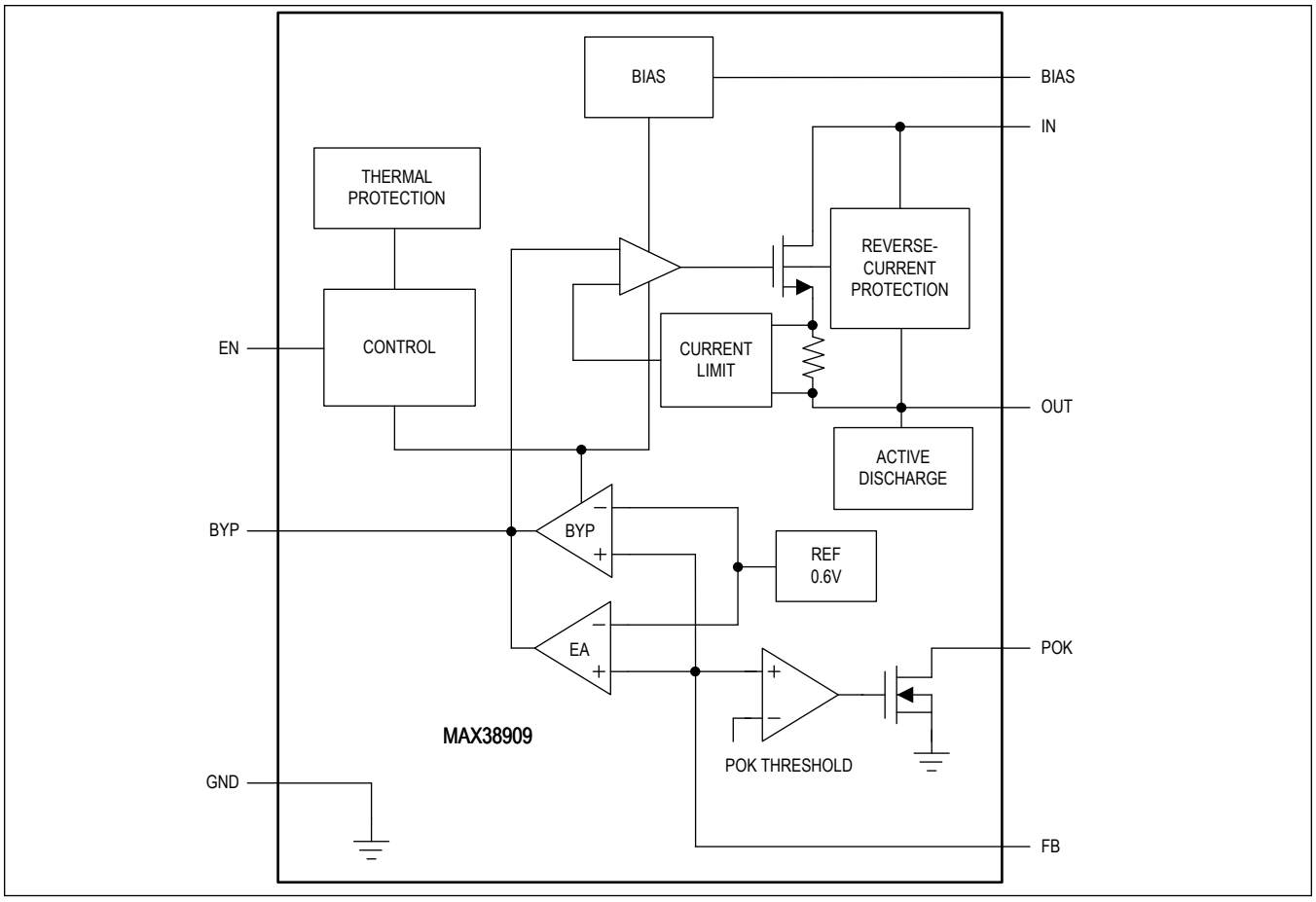
Pin Description

PIN		NAME	FUNCTION
14 TDFN	WLP		
1–4	A1–A3	IN	Regulator Supply Input. Connect to a voltage between 0.9V and 5.5V and bypass with a 22µF ceramic capacitor from IN to GND.
5	A4	BIAS	Bias Supply Input. Connect to a voltage between 2.7V and 20V and bypass with a 1µF capacitor from BIAS to GND. BIAS must be 2.0V or more above the V_{OUT} target.
6	A5	EN	Enable. Connect this pin to a logic signal to enable (V_{EN} high) or disable (V_{EN} low) the regulator output. Connect to BIAS to keep the output enabled whenever a valid supply voltage is present.
7	B1–B4	GND	Regulator Ground. Bring IN and OUT bypass capacitor GND connections to this pin for best performance.

Pin Description (continued)

PIN		NAME	FUNCTION
14 TDFN	WLP		
8	B5	POK	Power-On Reset Output. Connect a pullup resistor from this pin to a supply to create a reset signal that goes high after the regulator output has reached its regulation target voltage.
9	C5	FB	Output Voltage Feedback Input. Connect resistor divider across OUT and GND with the center connected to this pin to set any output voltage between 0.6V and 5.0V.
10	C4	BYP	Bypass Capacitor Input. Connect a 0.001µF to 0.1µF capacitor between OUT and BYP to reduce output noise.
11–14	C1–C3	OUT	Regulator Output. Sources up to 2A at the output regulation voltage. Bypass this pin with 22µF ceramic capacitor to GND. It is pulled low with a 70Ω resistance when the regulator is disabled.
—	—	EP	Exposed Pad (TDFN Only). Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heat sinking.

Functional Diagram



Detailed Description

The MAX38909 is a fast transient, high PSRR linear regulator that delivers up to 2A of load current. The regulator supports a wide input supply (0.9V to 5.5V) and BIAS (2.7V to 20V) voltage ranges, making it suitable for variety of applications. The output voltage regulation accuracy of ±1% is maintained across load, line, and temperature variations, requiring only 300mV of input-to-output headroom at full load for good PSRR. The output voltage can be adjusted to accommodate customers that desire to specify a single LDO in the BOM for multiple voltage rails.

The output voltage is programmed to a value in the range of 0.6V to 5.0V by using two external feedback resistors. The LDO is fully protected from damage by internal circuitry that provides programmable inrush current limiting, output overcurrent limiting, reverse current-limiting, and thermal overload protection.

Enable

The MAX38909 includes an enable pin (EN). The enable signal is an active-high digital signal that enables the device when its voltage passes the rising threshold ($V_{EN} \geq V_{IH}$ (EN)) and disables the device when its voltage is below the falling threshold ($V_{EN} \leq V_{IL}$ (EN)). While in the shutdown (V_{EN} = 0V), the MAX38909 consumes 1nA of current from the input supply. If a separate shutdown signal is not available, connect EN to BIAS. When EN is driven by a host its bias current will vary with the BIAS supply level. See the Typical Operating Characteristics for more information.

Bypass

The capacitor connected from BYP to OUT filters noise at the reference, feedback resistors and regulator input stage. It provides a high-speed feedback path for improved transient response. A 10nF capacitor rolls off noise at around 32Hz.

The slew rate of the output voltage during startup is also determined by the BYP capacitor. The MAX38909 features programmable, monotonic, soft-start set by this capacitor. Its use is highly recommended to minimize inrush current into the output capacitor. A 10nF capacitor sets the slew rate to 5V/ms. This startup rate results in a 110mA slew current drawn from the input at startup to charge 22µF output capacitance.

The BYP capacitor value can be adjusted from 1nF to 100nF to change the startup slew rate according to the following formula:

Startup slew rate = 5V/ms x $10nF/C_{BYP}$

where C_{BYP} is in nF.

This slew rate applies until V_{OUT} reaches 75% of the target after which the V_{OUT} slew rate is reduced.

Also, note that being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Power OK

The power-OK (POK) function monitors the voltage at the feedback pin to indicate the output voltage is in regulation. Its operation versus the output voltage is shown in Figure 1.

The POK pin is open-drain and requires a pullup resistor to an external supply to properly report the device regulation status to other devices so it can be used for sequencing. Check if the external pullup supply voltage results in a valid logic levels for the receiving device or devices.

The range of the pullup resistance is between 10kΩ and 100kΩ. Its lower limit comes from a pulldown strength of the POK transistor while the higher limit is determined by maximum leakage current at the POK pin.

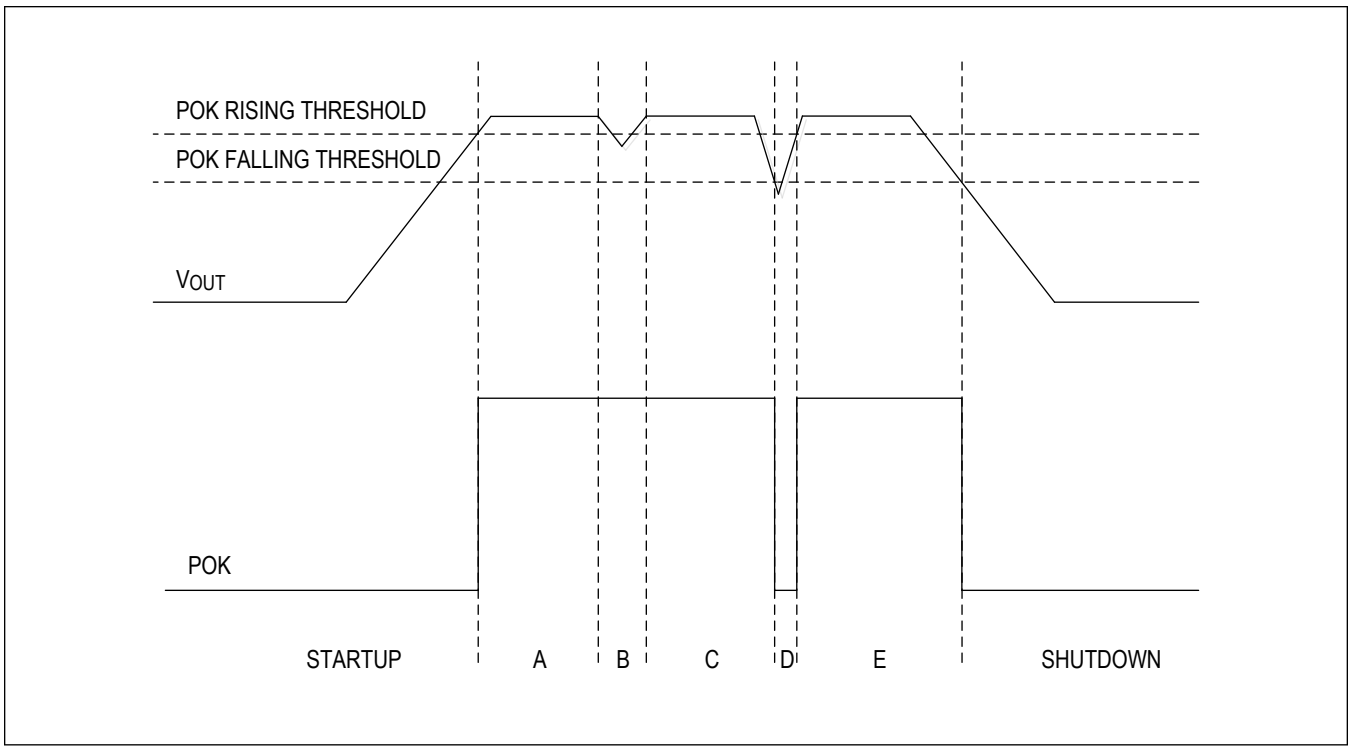


Figure 1. Typical POK Operation

The POK operation versus the output voltage is shown in the Figure 1 above. Different operating regions are:

A: The device is in regulation.

B: V_{OUT} sags, but does not reach the POK falling threshold.

C: The device is in regulation.

D: V_{OUT} sags low enough to cross the POK falling threshold. The POK is driven low until V_{OUT} recovers above the POK rising threshold.

E: The device is in regulation.

Protection

The MAX38909 is fully protected from an output short-circuit by a current-limiting and thermal overload protection circuit. If the output is shorted to GND, the output current is limited to 2.8A (typ). Under these conditions, the device quickly heats up. When the junction temperature reaches +165°C, a thermal limit circuit shuts the output device off. Once the device cools to 150°C, the output turns back on to reestablish regulation. If the fault persists, the output current cycles on and off as the junction temperature slews between +150°C and +165°C. Continuously operating in the fault conditions or above +125°C junction temperature is not recommended since long-term reliability might be reduced. In dropout, the current limit triggers at 4A (typ). Once the limit is triggered, the device limits the current to 2.8A (typ).

The thermal protection can also be triggered when the device is exposed to excessive heat in the system causing the die temperature to reach undesired levels.

The MAX38909 provides the reverse-current protection when the output voltage is higher than the input. If extra output capacitance is used at the output, a power-down transient at the input would normally cause a large reverse-current through a conventional regulator. The MAX38909 include a reverse-voltage detector that trips when IN drops 6.5mV below OUT shutting off the regulator and opening the body diode connection preventing any reverse current. The reverse current is a current that flows through the body diode of the pass element and is undesired due to its impact on power

dissipation and long-term reliability especially at higher current levels. The conditions where the reverse current can be flowing back to IN are:

• If the device has a large C_{OUT} and the input supply collapses quickly; OUT has little or no-load current,

• The output is biased when the input supply is not established, or

• The output is biased above the input supply.

The MAX38909 blocks reverse currents that exceed about 0.7A by opening a switch in series with the pass device body diode.

Undervoltage Lockout (UVLO)

The MAX38909 undervoltage lockout (UVLO) circuits respond quickly to glitches on IN or BIAS and attempts to disable the output of the device if either of these rails collapse. The local input capacitance prevents transient brownouts in most applications.

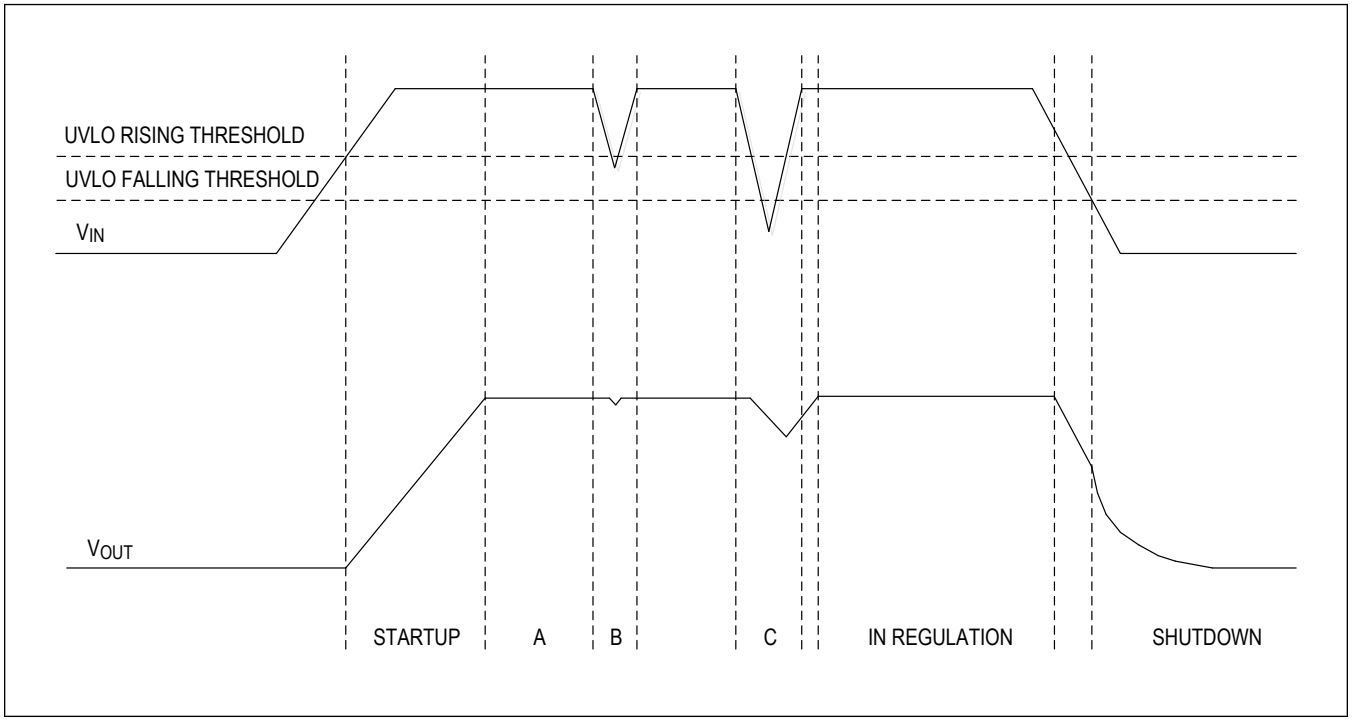


Figure 2. Typical IN UVLO Operation

The Figure 2 above reflects UVLO operation. The different operation regions are:

STARTUP: The device begins the soft-start once the input voltage crosses its UVLO rising threshold providing the BIAS voltage is already above its UVLO rising threshold and the device is enabled ($V_{EN} > V_{IH}$).

A: The device is in regulation.

B: An input supply brownout condition where V_{IN} can sag below UVLO rising threshold but not below the falling threshold. The device is enabled. Note the output sags once the device is in dropout.

C: An input supply brownout condition where V_{IN} sags below UVLO falling threshold. The device is disabled when V_{IN} crosses its UVLO falling threshold. V_{OUT} drops due to load current. The regulator gets enabled again once V_{IN} recovers to the UVLO rising threshold. Note the output starts to sag once the device is in dropout.

SHUTDOWN: The output voltage starts to ramp down once the device gets into dropout. It is disabled when the input

voltage drops below its UVLO falling threshold.

During V_{IN} power-up, the MAX38909 begins V_{OUT} soft-start after V_{IN} crosses the V_{IN} UVLO rising threshold. This assures proper V_{OUT} ramp up and transition to regulation. V_{OUT} soft-start rate should be kept as or slower than the V_{IN} slew rate to avoid entering the dropout. In some situations, V_{IN} transients can place the regulator into dropout. As V_{IN} starts climbing again and the device comes out of the dropout, the output can overshoot, as shown in Figure 3. This condition is avoided by using an enable signal or by increasing the soft-start time with larger C_{BYP}.

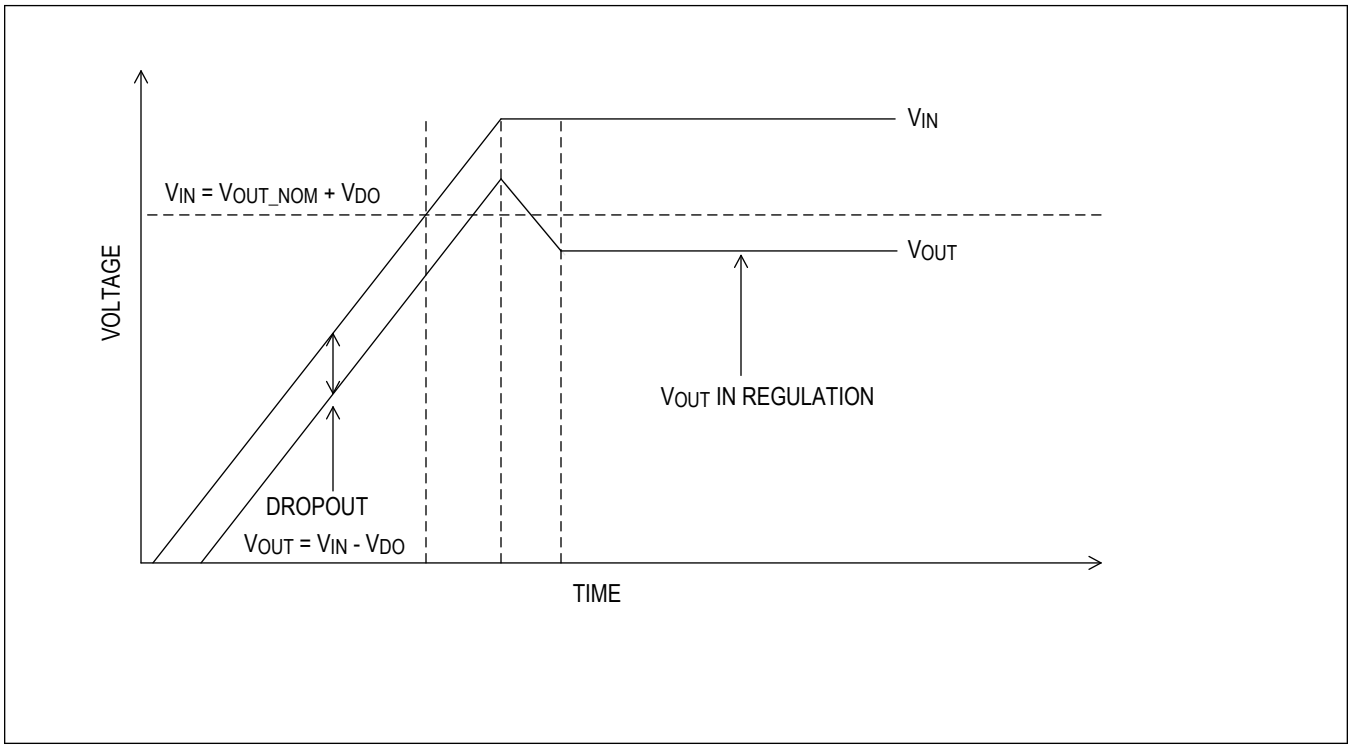


Figure 3. Startup into Dropout

Active Discharge

When EN is low or BIAS supply is below its falling UVLO threshold, the MAX38909 connects a 70Ω resistor from V_{OUT} to GND in order to discharge the output capacitance.

Voltage Selection

The MAX38909 use external feedback resistors to set the output regulation voltage. The output voltage can be set from 0.6V to 5.0V. Set the bottom feedback resistor R1 to less than 100kΩ to minimize FB input bias current error. Calculate the value of the top feedback resistor R2 as follows:

$R2 = R1 \times (V_{OUT}/V_{FB} - 1)$

where V_{FB} is the feedback regulation voltage of 0.6V.

To set the output to 1.0V, for example, R2 should be:

$R2 = 15k\Omega \times (1.0V/0.6V - 1) = 10k\Omega$

R1 of 15kΩ is recommended to optimize noise performance.

Values of the resistor divider and its tolerance will have a direct impact to V_{OUT} accuracy. 1% resistors or better are recommended. Table 1 shows recommended values for the feedback resistors.

Table 1. Recommended Feedback Resistor Values

TARGETED OUTPUT VOLTAGE (V)	TOP FEEDBACK RESISTOR VALUES (kΩ)	BOTTOM FEEDBACK RESISTOR VALUES (kΩ)	CALCULATED OUTPUT VOLTAGE (V)
0.8	4.99	15.0	0.799
0.9	7.50	15.0	0.900
1.0	10.0	15.0	1.0
1.2	15.0	15.0	1.2
1.5	22.6	15.0	1.504
1.8	30.1	15.0	1.804
2.5	47.5	15.0	2.5
2.7	52.3	15.0	2.692
3.0	59.0	14.7	3.008
3.3	68.1	15.0	3.324
3.6	75.0	15.0	3.6
4.5	97.6	15.0	4.504
5.0	110.0	15.0	5.0

Applications Information

Input and Output Capacitors

The MAX38909 is designed to have stable operation using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and bypass pin. Multilayer ceramic capacitors (MLCC) with X7R dialectic are commonly used for these types of applications and are recommended due to their relatively stable capacitance across temperature. Nevertheless, amount of equivalent capacitance depends on operating DC voltage, AC voltage ripple, temperature, etc. Therefore, the capacitor data sheet needs to be properly examined.

The MAX38909 is designed and characterized for operation with X7R ceramic capacitors of 22µF or greater (10µF or greater of effective capacitance) both at the input and output. Place these capacitors as close as possible to the respective input and output pins to minimize trace parasitics.

A combination of multiple output capacitors in parallel boosts the high-frequency PSRR.

Thermal Design

To optimize the MAX38909 performance, special consideration is given to the device power dissipation and PCB thermal design. Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. It can be calculated by following equation:

Loss (W) = $(V_{IN} – V_{OUT}) \times I_{LOAD}$

The optimal power dissipation can be achieved by carefully choosing input voltage for a given output target rail voltage.

The main thermal conduction path for the device is through the exposed pad of the package. As a result, the thermal pad must be soldered to a copper pad area under the device. Thermal plated vias must be placed inside the thermal PCB pad to transfer heat to different GND layers in the system. The vias should be capped to minimize solder voids. The maximum power dissipation is determined by using thermal resistance from the device junction to ambient keeping the maximum junction temperature below +125°C. Thermal properties of the package are given in the *Package Information* section.

The first order power dissipation estimate for the 3.3V IN and 2.5V OUT with load current of 500mA condition is:

Loss (W) = $(V_{IN} – V_{OUT}) \times I_{LOAD}$ = (3.3V – 2.5V) x 0.5A = 0.4W

Assuming the MAX38909ATD+ is used, this power dissipation raises the junction temperature to:

$T_J = (PD \times \theta_{JA}) + 25°C$ = (0.4W x 41°C/W) + 25°C = 41.4°C

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	FEATURE
MAX38909ATD+	-40°C to +125°C	14 TDFN, 3mm x 3mm	2A LDO, enable input, externally adjustable output, low noise bypass
MAX38909ANL+	-40°C to +125°C	15 WLP, 5 x 3, 0.4mm pitch	2A LDO, enable input, externally adjustable output, low noise bypass

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/20	Release for market intro	—
1	11/20	Updated *Ordering Information* table	19