AN5165
Application note

Development of RF hardware using STM32WB microcontrollers

Introduction

STM32WB Series microcontrollers integrate a high quality RF transceiver for Bluetooth® Low Energy and 802.15.4 radio solution.

Special care is required for the layout of an RF board compared to a conventional circuit.

At high frequencies copper interconnections (traces) behave as functional circuit elements introducing disturbances that can degrade RF performance. Parasitic components created by traces and pads contribute significantly to the overall circuit behavior. Layout rules have to be carefully followed to mitigate these effects and achieve the requested performance.

This document describes the precautions to be taken to achieve the best performance from the MCU. The description is based on the QFN48 / QFN68 / UFBGA129 reference boards for 2-layer PCBs, and on the WLCSP100 reference board for the 4-layer PCB.

For some products of the STM32WB Series only QFN48 is available, check the product datasheet available on *www.st.com*.

These guidelines are generic, they need to be adapted to the specific application.

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1 RF basics

This section covers generic terms and definitions used in RF board design.

The following references can help the user.

1	Paul Horowitz and Winfield Hill	The art of electronics (3rd edition)	Cambridge University Press
2	Roger C. Palmer	An introduction to RF circuit design for communication systems (2nd edition)	Newnes
3	Christopher Bowick	RF circuit design (2nd edition)	Newnes
4	Joseph J. Carr and George W. Hippisley	Practical antenna handbook (5th edition)	McGraw-Hill Education
5	Smith chart (free SW)		http://www.fritz.dellsperger.net
6	Coplanar waveguide calculator (free SW)		http://wcalc.sourceforge.net

1.1 Terminology

1.1.1 Power

This unit, expressed in dBm, is the measure of the RF signal strenght: **dBm = 10 Log P**, where P is the power in mW. So it will be:

- 1 pW = -90 dBm
- 10 µW = -20 dBm
- 1 mW = 0 dBm
- 2 mW = 3 dBm
- 10 mW = 10 dBm

1.1.2 Gain

The gain (expressed in dB) is the ratio between the output and the input power of an RF device. Negative values correspond to an attenuation.

1.1.3 Loss

If there is impedance mismatch, incorrect transmission line design or incorrect PCB material selection between two stages of a circuit, signal power losses appear and not all the power is transmitted from one stage to the following one. There are also inherent losses, e.g. the dielectric loss, which depends upon the laminate and materials used to manufacture the board.

1.1.4 Reflection coefficient, voltage standing wave ratio and return loss

When a signal flows from a source to a load via a transmission line, if there is a mismatch between the characteristic impedance of the transmission line and the load a portion of the

signal will be reflected back to the source. The polarity and the magnitude of the reflected signal depend on whether the load impedance is higher or lower than the line impedance.

The reflection coefficient (Γ) is the measure of the amplitude of the reflected wave versus the amplitude of the incident wave, namely $\Gamma = (Z - Z_0) / (Z + Z_0) = (z - 1) / (z + 1)$.

The voltage standing wave ratio (VSWR) is the measure of the accuracy of the impedance matching at the point of connection. It is a function of the reflection coefficient and is expressed as $VSWR = (1 + |\Gamma|) / (1 - |\Gamma|)$. If VSWR is 1, there is no reflected power.

The return loss (RL) is a function of the reflection coefficient, but expressed in dB: $RL = 20 \log |\Gamma|$.

1.1.5 Harmonics

The harmonics are the integer unwanted multiples of input frequency (fundamental frequency).

1.1.6 Spurious

The spurious are the non-integer multiples of input frequency (unwanted frequencies).

1.1.7 Intermodulation

When two RF signal are mixed together, intermodulation products are the signals composed by an integer multiple of the sum and the difference between the two signals.

1.2 Impedance matching

To optimize the RF performance it is imperative to adapt the impedance matching from the antenna to the input of the chip, as well as that from the chip output to the antenna.

If this adaptation is poor, it will introduce losses in the RX/TX chain. These losses will immediately translate in lower sensitivity and in lower signal amplitude of the transmitted signal. These disadatpations, if high enough, will increase the level of TX harmonics.

As a consequence it is very important to spend efforts to adapt as best as possible the RF chain. In the Bluethooth® Low Energy bandwidth of the STM32WB, and more generally in RF frequencies, spurious elements (such as PCB track inductances and layer capacitors, trace length) have a significant impact on the impedance matching. To achieve the best TX/RX budget (optimum transfer of signal and energy) between the load and the STM32WB, a dedicated matching network is needed between the two blocks.

The maximum power is transferred when the internal resistance of the source equals the resistance of the load. When extended to a circuit with a frequency-dependent signal, to obtain maximum power transfer the load impedance must be the complex conjugate of the source impedance.

1.3 Smith chart

The Smith chart (*Figure 1*) is used to determine the matching network.

1.3.1 Normalized impedance

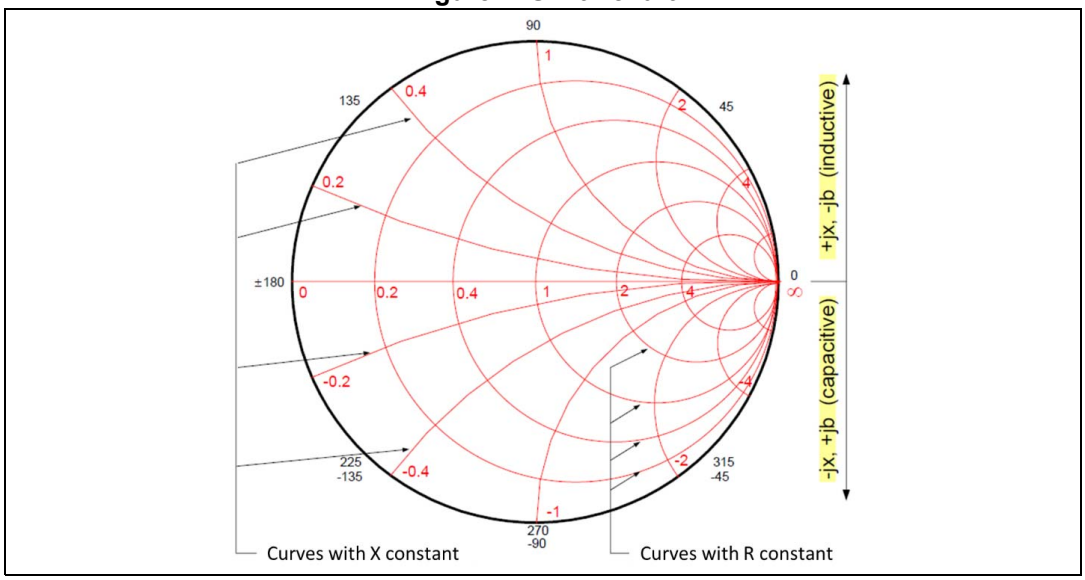
The normalized impedance z is a complex impedance (r is the real part and x the imaginary part): **$z = r + jx = Z / Z_0$** where Z_0 is the characteristic impedance and is often a constant (in our case Z_0 = 50 Ω).

For a capacitor $z = - j / (2 \pi * f * C * Z_0)$, for an inductor $z = j (2 \pi * f * L) / Z_0$.

1.3.2 Reading a Smith chart

The Smith chart is represented with the normalized impedance scale $z = Z / Z_0$.

Figure 1. Smith chart



If Z_0 = 50 Ω, when there is matching ($Z = Z_0$) the normalized impedance at 50 Ω is 1 and it is the center of the Smith chart. The goal in the search of a matching network is to converge towards this point.

The horizontal axis of the Smith chart represents pure resistors: at the left side, z = 0 (short circuit) and at the right side, z = ∞.

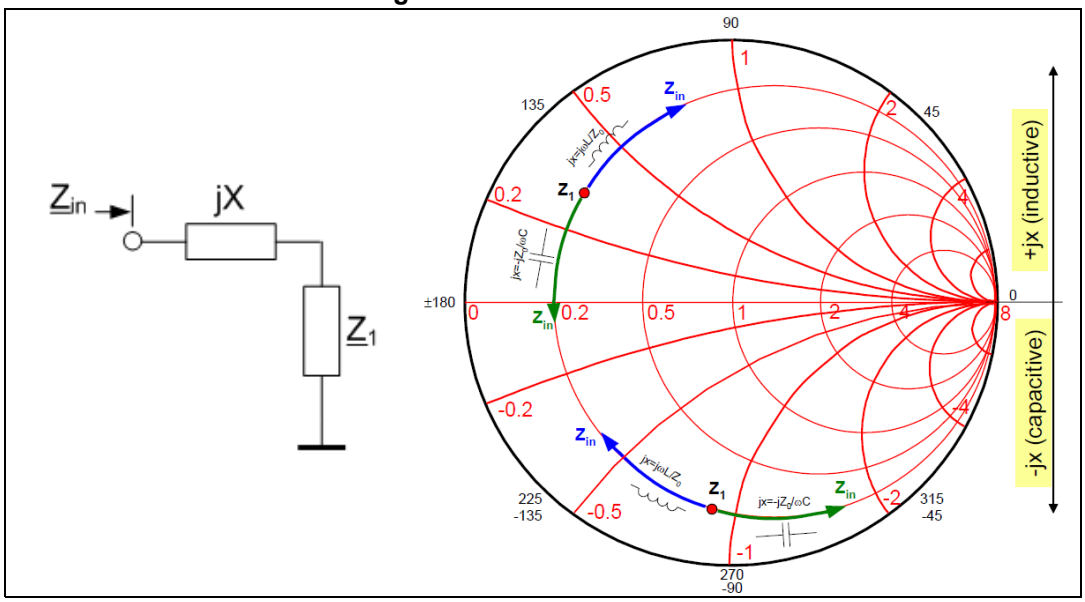
The region located above the X axis represents impedances with inductive reactance (positive imaginary part of the complex impedance) or capacitive susceptance (positive imaginary part of the complex admittance).

The region below the X axis represents impedances with capacitive reactance (negative imaginary part of the complex impedance) or inductive susceptance (negative imaginary part of the complex admittance).

Serial inductor or capacitor

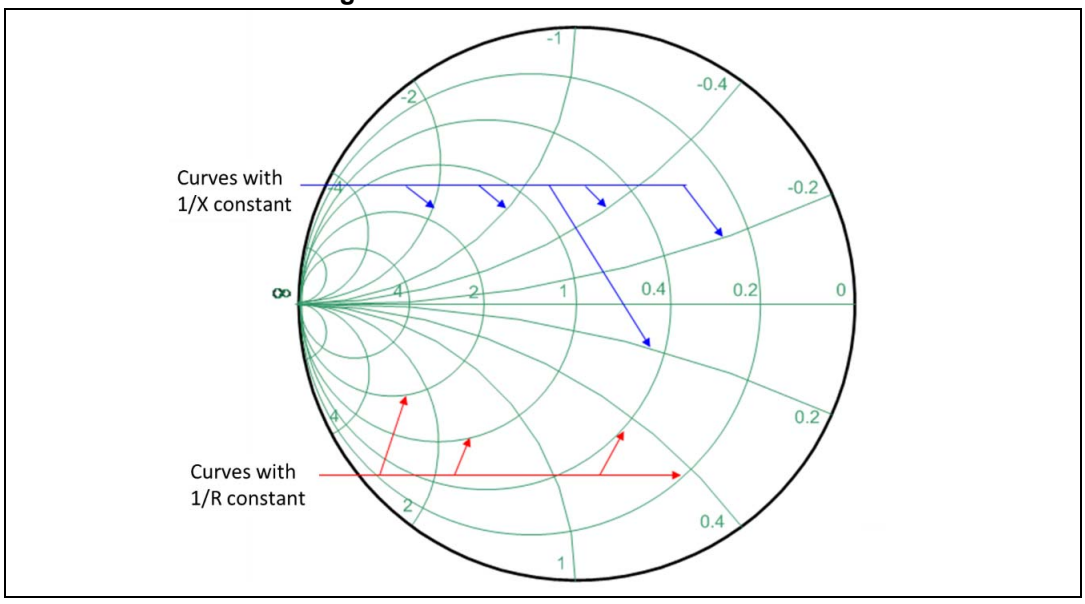
If an inductor or a capacitor is in series with the load impedance Z_1 the resulting impedance Z_{in} moves as shown in *Figure 2*.

Figure 2. Series connection



As for the Smith chart in normalized impedance (z) scale, the Smith chart can be represented in normalized admittance (y = 1/z) scale as shown in *Figure 3*.

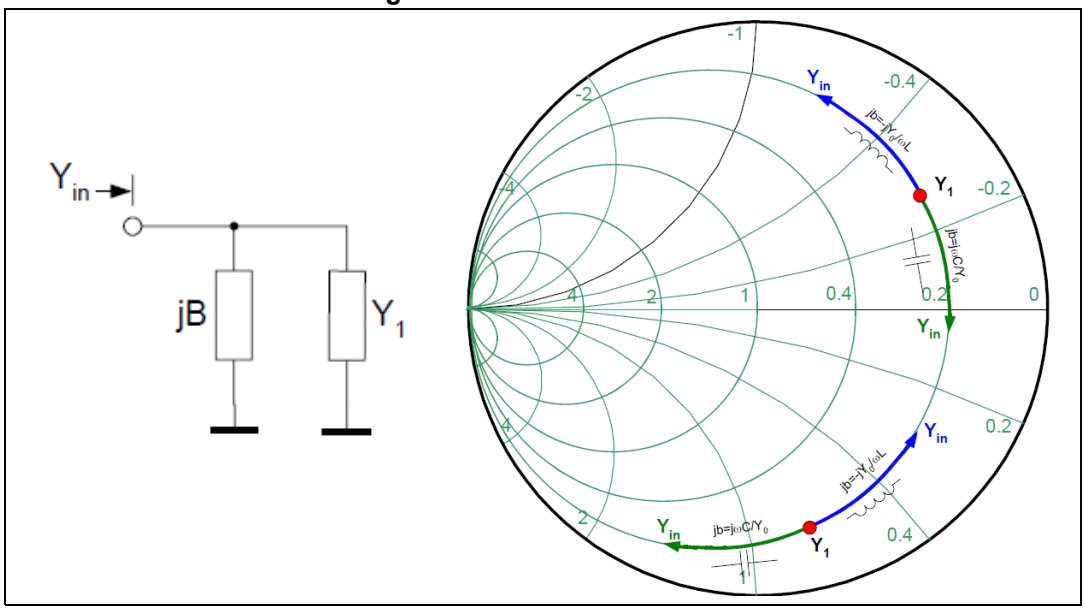
Figure 3. Smith chart for admittance



Parallel inductor or capacitor

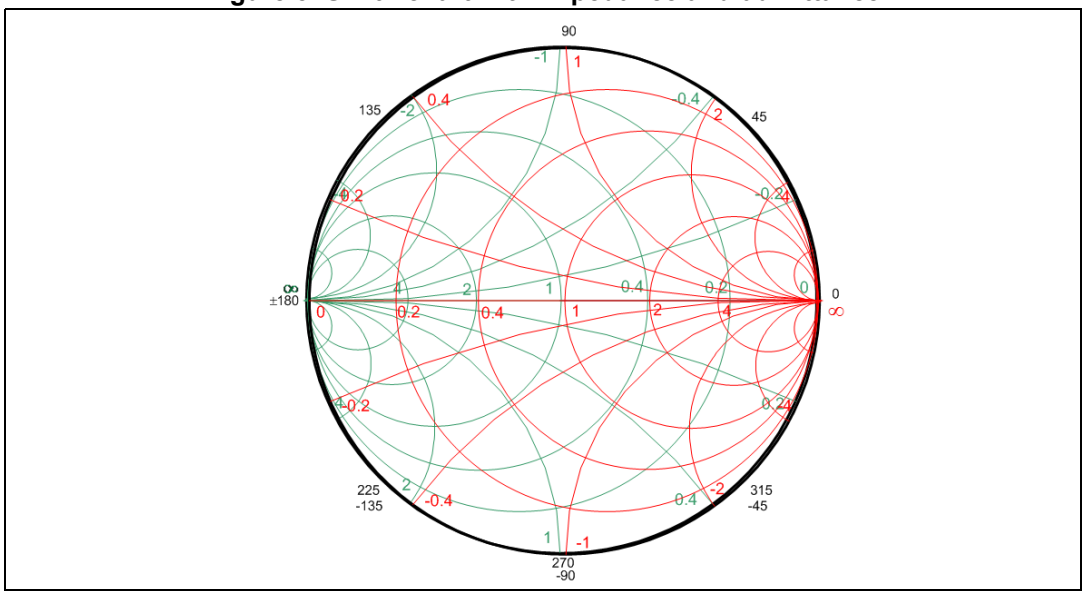
If an inductor or a capacitor is in parallel with the load admittance Y_1 the resulting impedance Y_{in} moves as shown in *Figure 4*.

Figure 4. Parallel connection



In *Figure 5* the Smith chart in impedance and admittance planes.

Figure 5. Smith chart with impedance and admittance



The circles with constant VSWR are an additional information can be retrieved from the Smith chart even when they are not represented. These circles have the same center, and as values the intersections between the circle and the right side of the horizontal axis from the center (see *Figure 6*).

Figure 6. Smith chart with VSWR circles

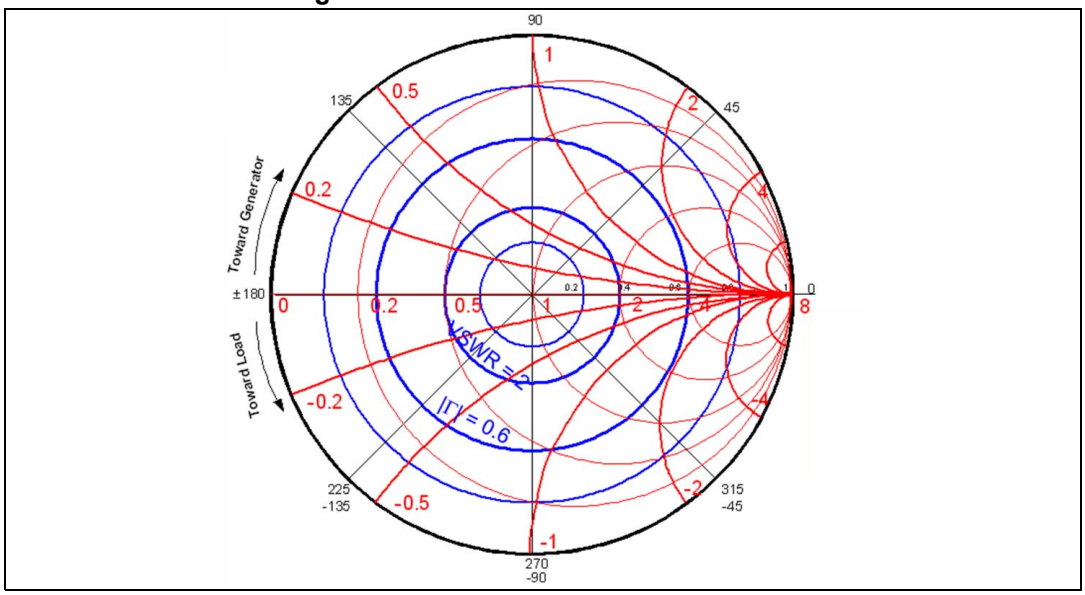
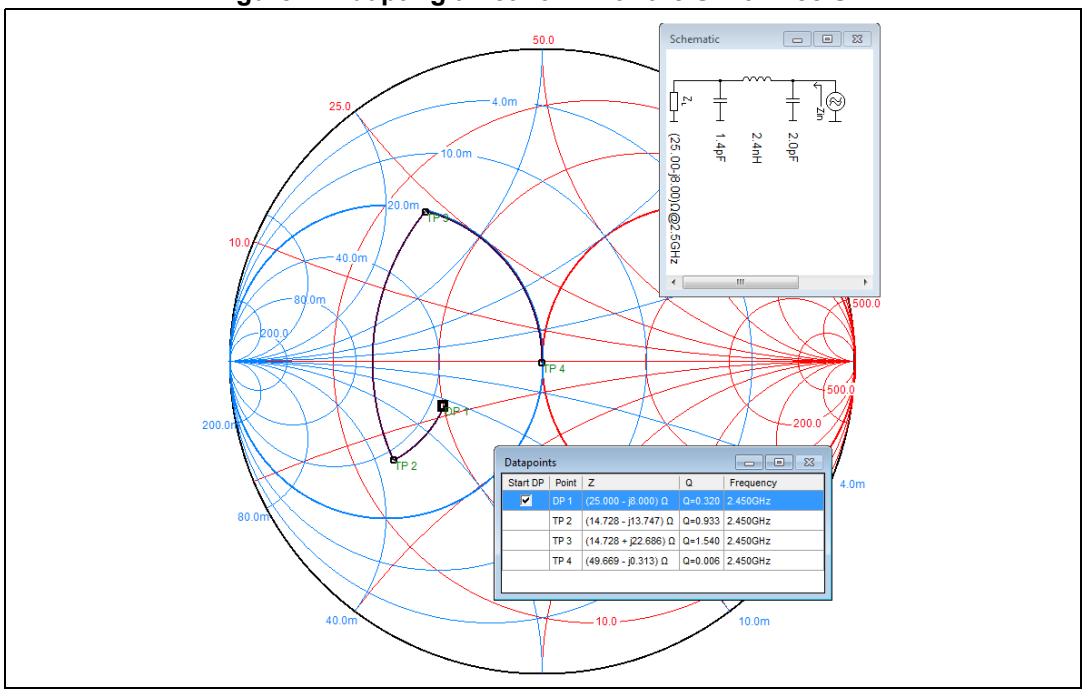


Figure 7 is an example of the free software “Smith”: starting from Z_L = (25.00 – j*8.00) Ω, represented on the Smith chart by DP1, the goal is to obtain Z_{in} = 50 Ω. By adding (in series or in parallel) inductors or capacitors, the impedance converges towards the center of the graph.

Figure 7. Adapting a network with the Smith free SW



2 Reference board schematics

The STM32WB Series microcontrollers are based on Arm®(a) cores.

The schematics in *Figure 8*, *Figure 9* and *Figure 10* represent, respectively, the 2-layer reference boards for UFQFPN48, VFQFPN68 and UFBGA129 packages. *Figure 11* represents the 4-layer reference board for WLCSP100. The RF output is only from SMA. All the layout guidelines described in the next paragraphs for two layers PCB are based on these boards.

Table 1. External components

Component(s)	Description
C1, C2	Decoupling capacitors for V_{DDRF}
C3, C4	Matching capacitors
C5, C6, C7	Decoupling capacitors for V_{DD}
C8	Decoupling capacitor for V_{BAT}
C9	Decoupling capacitor for V_{DDUSB}
C10	Decoupling capacitor for V_{DDA}
C12	Decoupling capacitor for SMPS
C11, C13	DC-DC converter filtering capacitors
C14, C15	X2 capacitors
C16	Decoupling capacitor for NRST pin
D1	Diode protection for NRST pin
FLT1	Integrated Low-Pass Filter
L1	Matching inductor
L2, L3	DC-DC converter inductor
L4	Filtering inductor for V_{DDA}
R1	Pull-up resistor for NRST
R2	Boot selector resistor
U1	STM32WBxx
X1	High frequency crystal
X2	Low frequency crystal

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

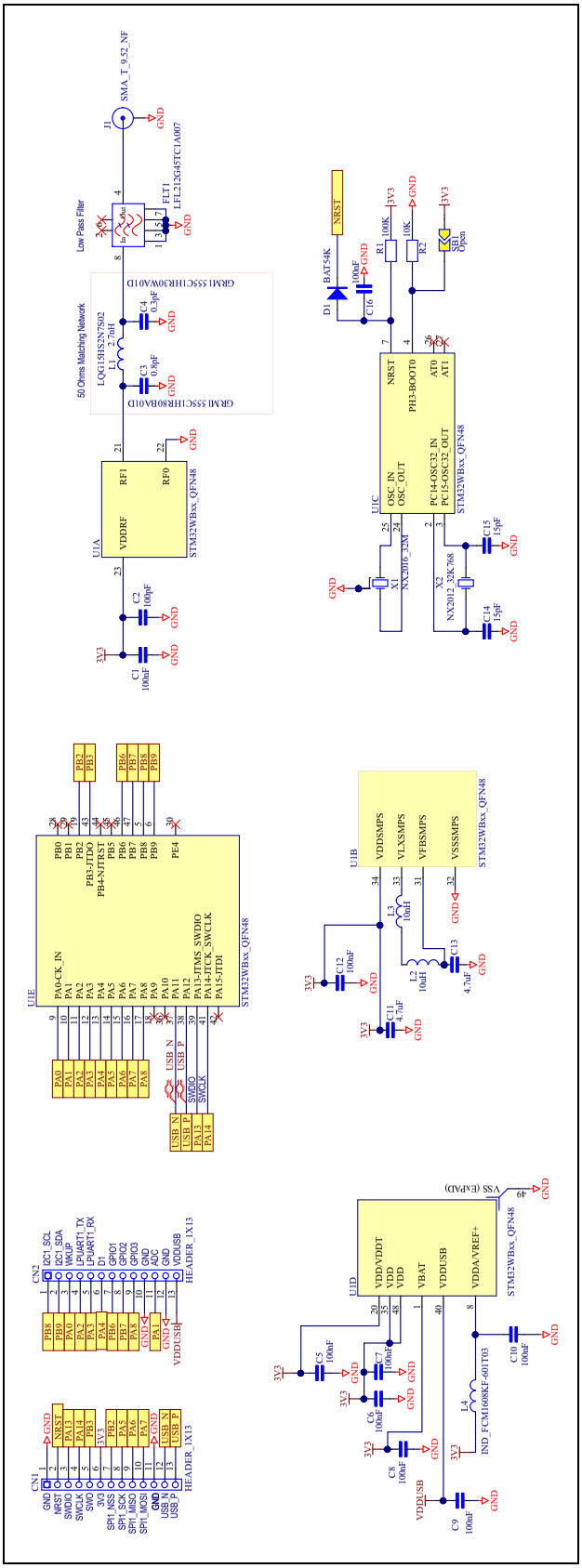


Figure 8. UFQFPN48 reference board

Figure 9. VFQFPN68 reference board

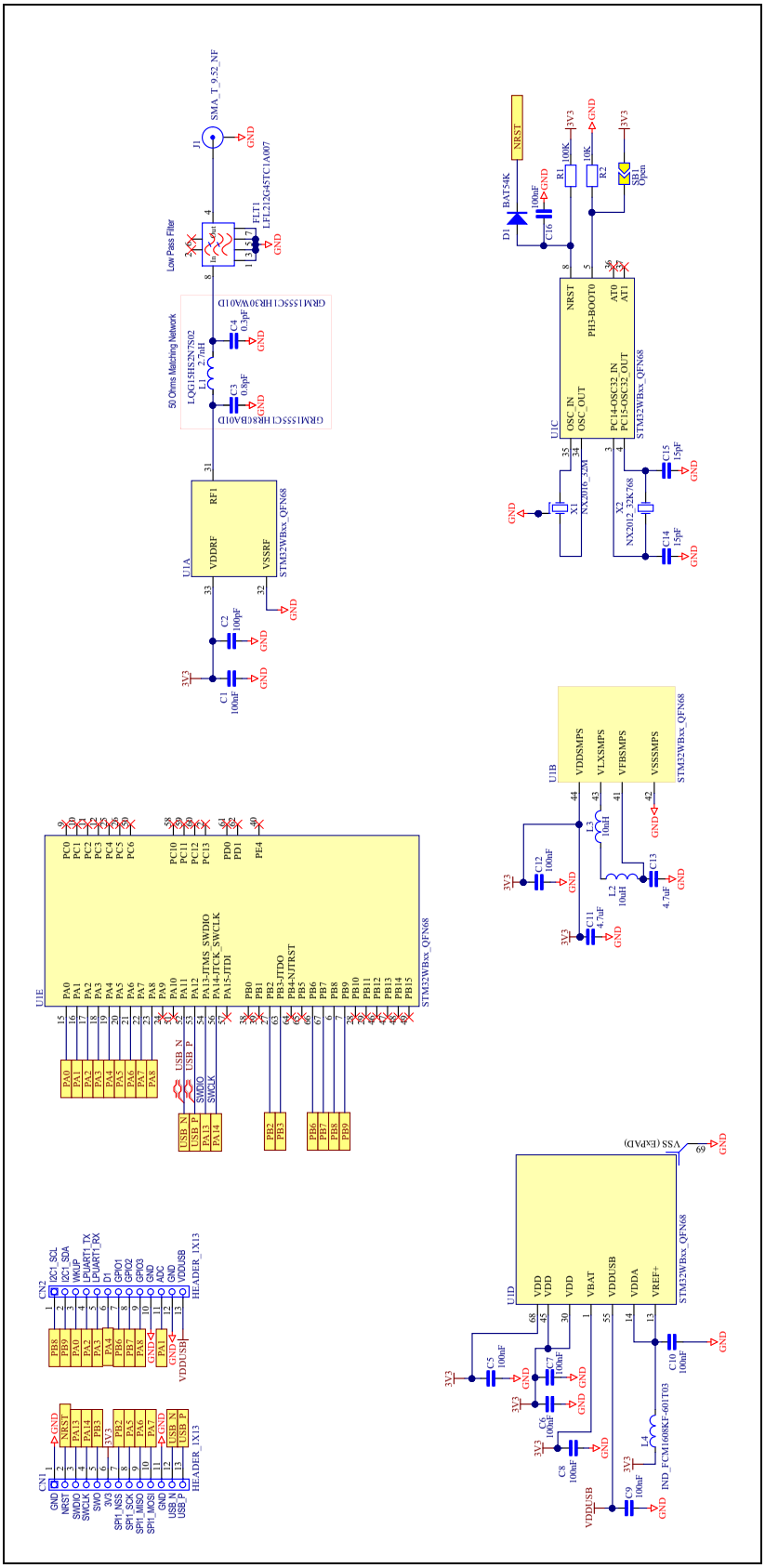
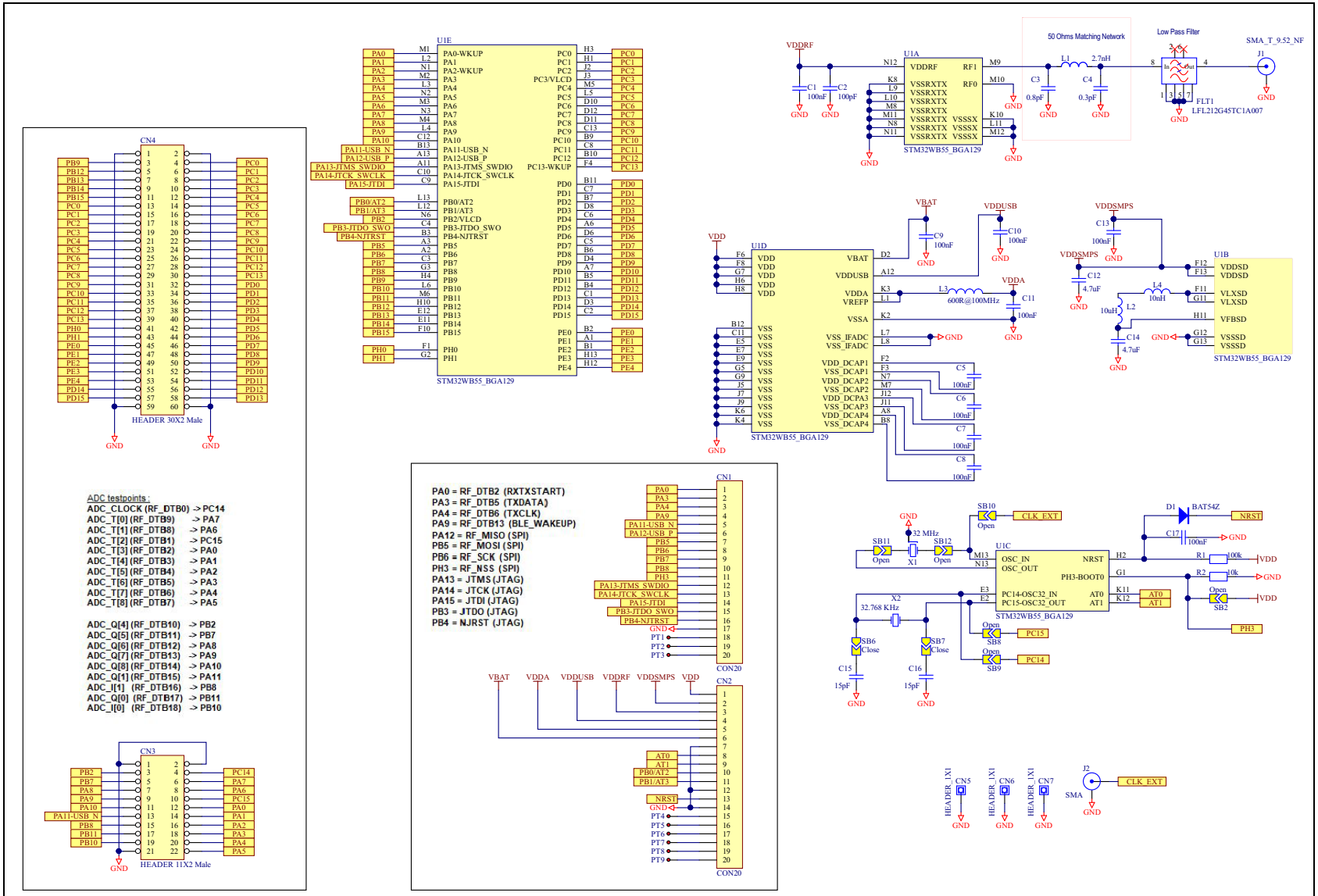


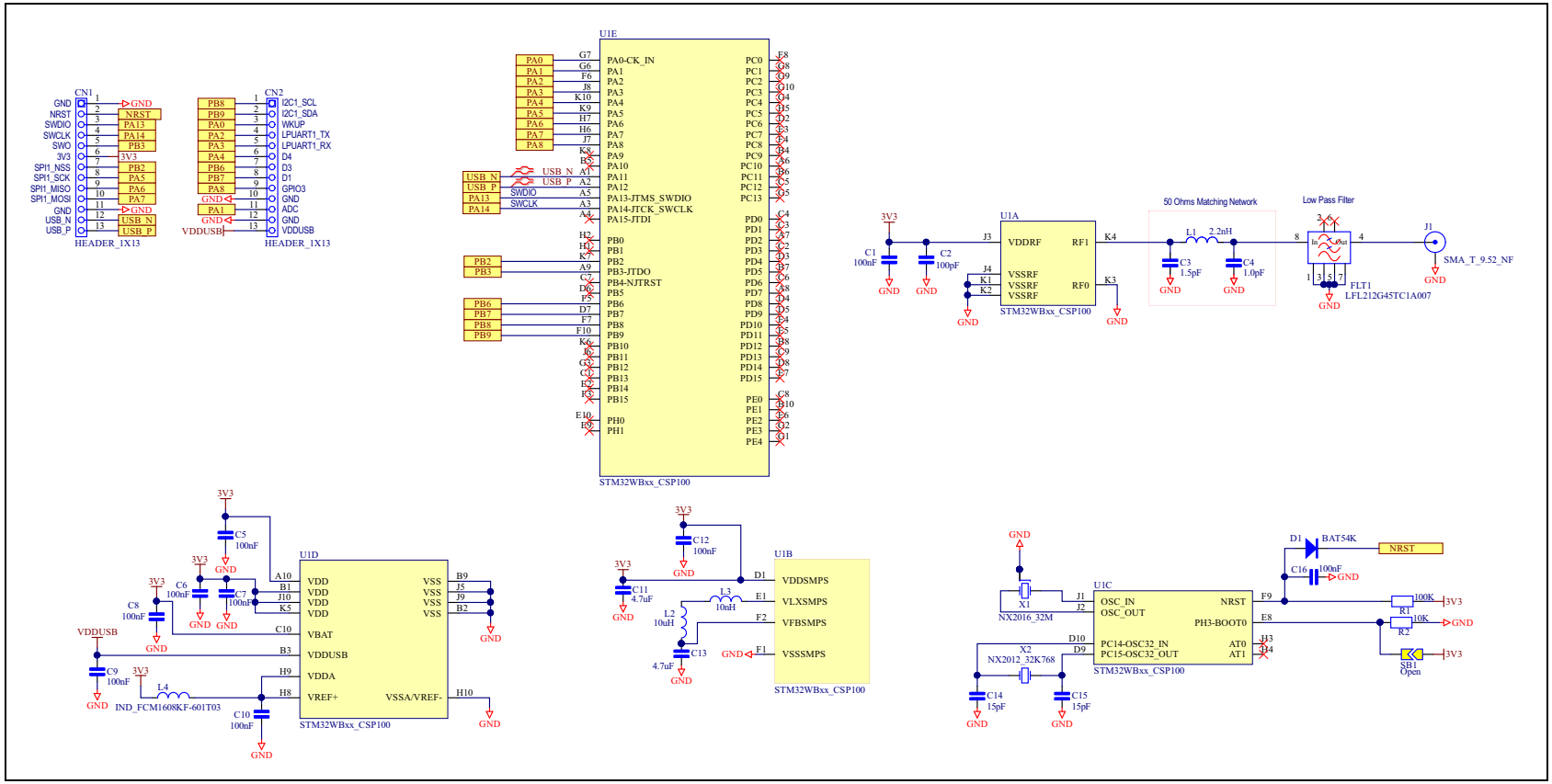
Figure 10. UFBGA129 reference board



Connecteurs sur la carte fille (TOP LAYER)

Connecteurs vers la carte mère (BOTTOM LAYER)

Figure 11. WLCSP100 reference board



3 Components choice

In the Bluetooth® Low-Energy bandwidth and more generally at high frequencies, the choice of the external components is critical because they directly influence the performance of the application.

3.1 Capacitor

A capacitor is a passive electrical component used to store energy in an electrical field. They are made with different construction techniques, materials (such as double-layer, polyester, polypropylene) and sizes. For RF design, it is recommended to use ceramic capacitors on surface mount version.

The equivalent circuit of a capacitor is represented in *Figure 12*. The resistor R_p represents its leakage current, while R_s is the equivalent serial resistor (ESR) and represents all ohmic losses of the capacitor. The inductor L_s is the equivalent serial inductance (ESL) and its value is function of the SRF (self-resonant frequency). From *Figure 13* it can be appreciated that the impedance of the capacitor is capacitive at low frequencies, at the SRF is resistive, and inductive at higher frequencies.

Figure 12. Capacitor equivalent circuit

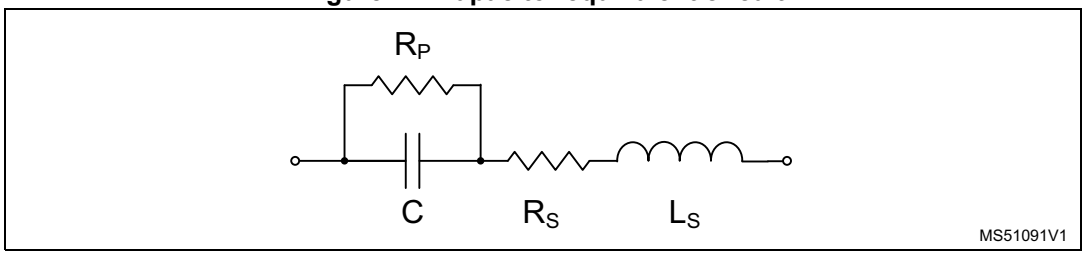
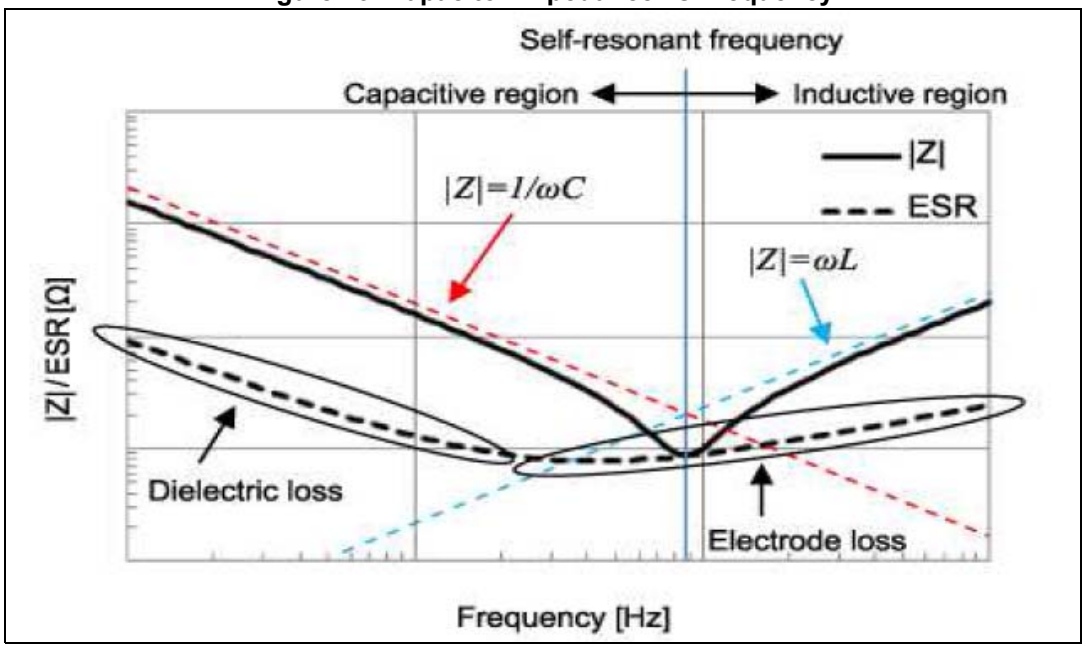


Figure 13. Capacitor impedance vs. frequency



For RF matching, multilayer ceramic capacitors offer linear temperature coefficients, low losses and stable electrical properties over time, voltage and frequency. SMD (Surface Mount Device) is used with a 0402 package, which is a good compromise between performance and handling.

For RF decoupling, the capacitance value must be chosen so that the frequency to be decoupled is close to or just above the self-resonant frequency of the capacitor.

For DC-DC converter, as the quality factor of a capacitor is inversely proportional to its ESR, a capacitor with low insertion loss and a good quality factor is recommended. The capacitor requires either an X7R or X5R dielectric.

Table 2. Capacitor temperature ranges

Minimum temperature		Maximum temperature		Variation over the temperature range	
Code	Temperature	Code	Temperature	Code	Variation (%)
X	-55 °C (-67 °F)	4	+65 °C (+149 °F)	P	±10
		5	+85 °C (+185 °F)	R	±15
Y	-30 °C (-22 °F)	6	+105 °C (+221 °F)	S	±22
		7	+125 °C (+257 °F)	T	+22 / -33
Z	+10 °C (+50 °F)	8	+150 °C (+302 °F)	U	+22 / -56
		9	+200 °C (+392 °F)	V	+22 / -82

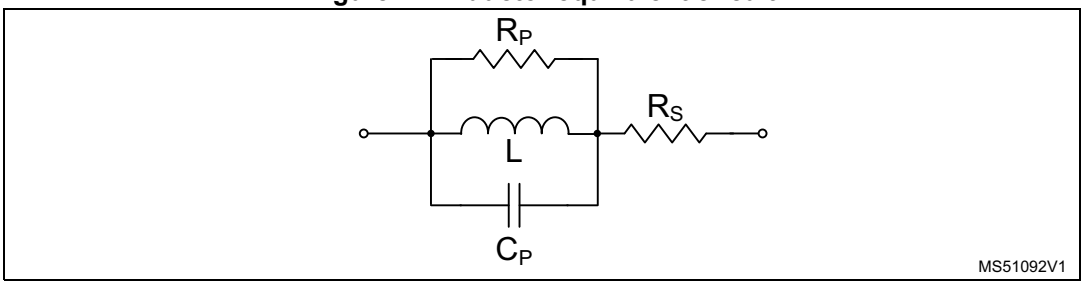
3.2 Inductor

An inductor is a passive electrical component used to store energy in its magnetic field. Inductors differ from each other for construction techniques and materials used to manufacture.

For RF design, where a high Q (Quality factor = Im[Z] / Re[Z]) is required to reduce insertion loss, it is generally recommended to use air core inductors. Those inductors do not use a magnetic core made of ferromagnetic material, but are wound on plastic, ceramic, or another nonmagnetic material. SMD is also used with a 0402 package.

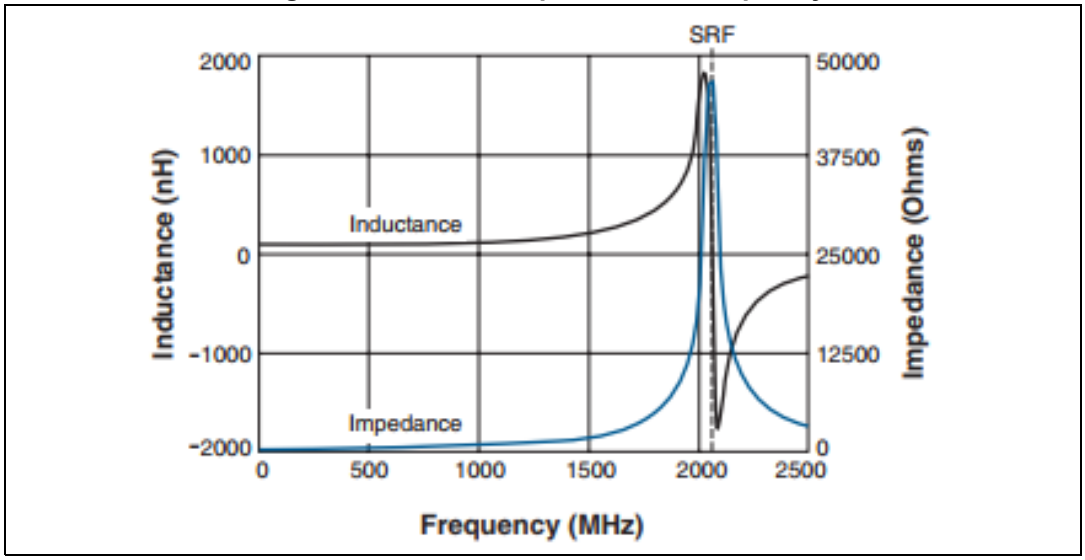
The equivalent circuit of an inductor is shown in *Figure 14*. The resistor R_s represents the losses due to the winding wire and terminations, its value increases with temperature. The resistor R_p represents the magnetic core losses, it varies with frequency, temperature and current. The capacitor C_p is associated with the windings.

Figure 14. Inductor equivalent circuit



As shown in *Figure 15*, at SRF the impedance and inductance are at their maximum. At lower / higher frequencies impedance and inductance increase / decrease with frequency.

Figure 15. Inductor impedance vs. frequency



For RF matching and decoupling, a good compromise between application cost and RF performance is to use an inductor with medium Q.

For DC-DC converter, the nominal value is 10 µH. The inductor value affects the peak-to-peak ripple current, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current.

It is important to use the components shown in the schematics to obtain the best RF performance with the given PCB layout of the reference boards.

3.3 SMPS

Some STM32WBxx microcontrollers (check the product datasheet available on *www.st.com*) embed an SMPS (switched mode power supply) that can be used to improve power efficiency when V_{DD} is high enough.

In order not to disturb the RF performances, this SMPS has its switching frequency synchronous with the RF main clock source HSE. The allowed frequency for the SMPS are 4 or 8 MHz. Note that during RF startup phases from low power modes, the HSI will be used instead of HSE, to allow a faster wakeup time than waiting from the HSE stabilization before starting the SMPS and the Digital logic.

Two specifics features have been added to this step down SMPS in association with all the low power modes supported by the STM32WB microcontrollers:

To operate properly the SMPS needs two inductors and two capacitors, whose value depend upon the targeted performance, and upon the PCB area and total height allowed in the mechanical design.

For best power performances, 4 MHz should be selected, leading to a 10 µH inductor associated with a 4.7 µF bulk capacitance. For smaller footprint, and especially to use very

low profile inductor, the 8 MHz can be selected, making it possible to use a 2.2 µH inductor associated with a 4.7 µF bulk capacitance.

For all packages it is advised to add an extra 10 nH inductor in series with the 10 or 2.2 µH one, to filter the RF harmonic that can degrade the receiver performance.

Another 4.7 µF capacitor must be used to decouple the V_{DDSMPS} supply. All of these external components must have the lowest possible ESR values. Note that V_{DDSMPS} must be connected to V_{DD}, and that voltage rising and falling must satisfy the conditions described in the STM32WB data sheet.

3.4 External crystal

Two oscillators with external crystals are available on the STM32WB microcontrollers.

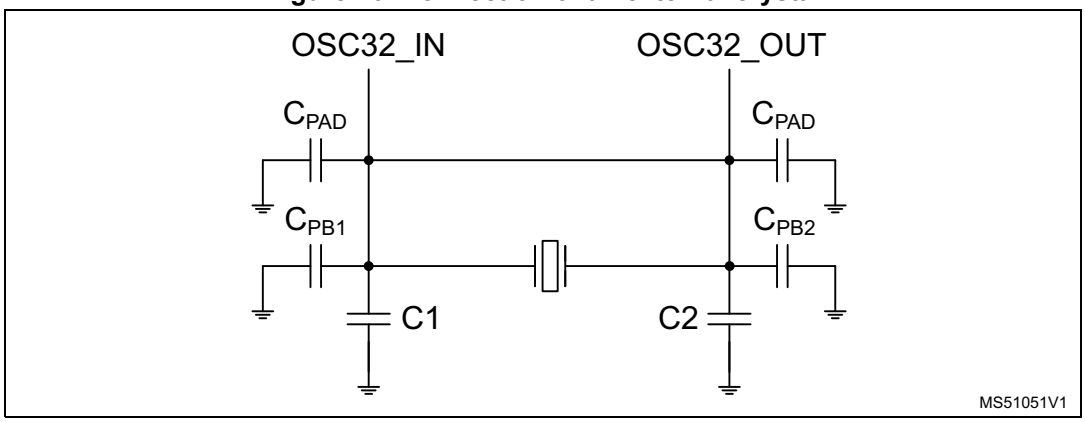
The HSE (High Speed External) with 32 MHz frequency is used by the RF subsystem. The crystal X1 has to be placed as close as possible to the oscillator pins OSC_IN and OSC_OUT to minimize output distortion and start-up stabilization time. The load capacitances are integrated on chip and can be tuned according to the selected crystal via an internal register. By default, the load capacitances are 8 pF for the NX2016 from NDK used on the boards.

The LSE (Low Speed External) with 32.768 kHz frequency is used for the RTC subsystem. C_1 and C_2 values must be tuned to meet to the recommended load capacitance C_0 of the selected crystal. Low power consumption and fast start-up time are achieved with a low C_0 value. On the contrary, a higher C_0 leads to a better frequency stability.

With reference to *Figure 16*, the total load capacitance C_0 seen by the crystal is $C_0 = [(C1 + C_{PAD} + C_{PB1}) * (C2 + C_{PAD} + C_{PB2})] / (C1 + C_{PAD} + C_{PB1} + C2 + C_{PAD} + C_{PB2})$, where:

- C_{PAD} accounts for the parasitic capacitance of the STM32WB pads, of the SMD components C_1 and C_2, and of the crystal itself.
- C_{PB1} and C_{PB2} represent the PCB routing parasitic capacitances. They must be minimized by placing X2, C1 and C2 close to the chip, thus improving the robustness against noise injection.
- C1 and C2 must be connected to ground by a separate via.

Figure 16. Connection of an external crystal



4 PCB stack and technology

PCB traces at RF frequencies have to be designed carefully because their length is a fraction of the signal wavelength. Furthermore, the impedance of a PCB trace at RF frequencies depends on the thickness of the trace, its height above the ground plane, and the dielectric constant and loss tangent of the PCB dielectric material. Another important parameter is the PCB stack up, described in this paragraph.

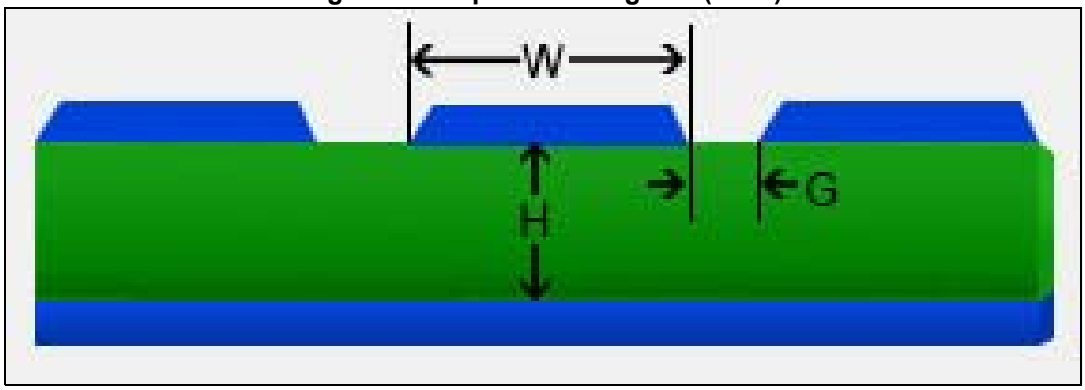
RF boards are usually designed with at least two or four layers to obtain the best performance.

4.1 RF transmission lines

The transmission lines on a PCB can be implemented on external layers (microstrips and coplanar waveguides), or buried in internal layers (striplines).

The coplanar waveguide (CPW) transmission line is composed (see *Figure 17*) of a central signal line of width W between two ground planes, separated from them by a gap G. The central line and ground planes are on the surface of a dielectric substrate of a thickness H.

Figure 17. Coplanar waveguide (CPW)



A version of CPW named GCPW or CPWG exists, with a ground plane opposite to the dielectric.

4.2 PCB substrate choice

There are different types of PCB substrate, even if built with the same basic material (glass), some of them have controlled parameters that are more suitable for RF product. The PCB substrate used in RF designs is FR-4 (flame resistant 4). This material is known to retain its high mechanical values and electrical insulating qualities in both dry and humid conditions, at the expenses of dielectric constant stability over frequency and loss.

4.3 2-layer PCB

With the 2-layer PCB (see *Figure 18*), the RF signals and routing are on the top layer while the bottom layer is used for grounding under the RF zones, and for routing in others parts. The ground plane must be continuous under the RF zones, otherwise the return path current can increase and degrade the RF performance.

Figure 18. 2-layer PCB

The 2-layer PCB provides a cheaper solution and can provide performance equivalent to those of the 4-layer PCB, but requires careful signal routing and component placement.

The 2-layer PCB definition of the reference boards for the UFQFPN48, VFQFPN68 and UFBGA129 packages is shown in *Figure 19* and the values are summarized in *Table 3*.

Figure 19. 2-layer PCB - Reference boards for UFQFPN48, VFQFPN68 and UFBGA129

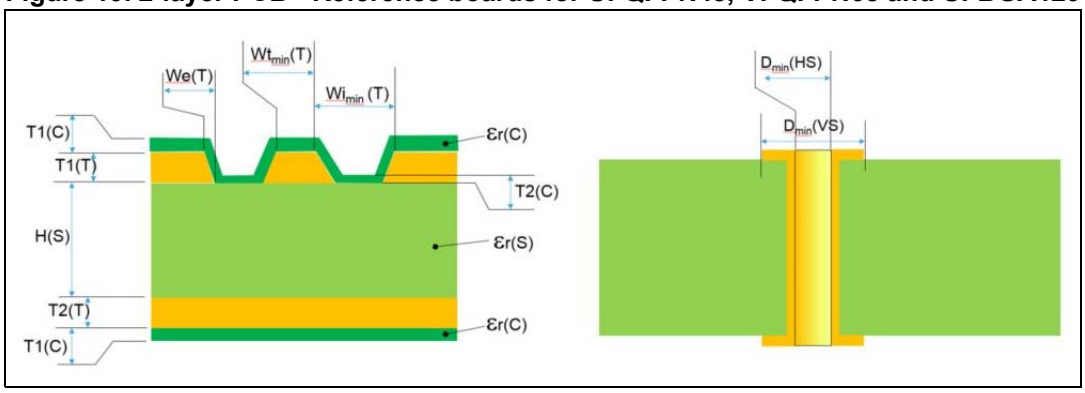


Table 3. 2-layer PCB - Reference values

Parameter	Symbol	Value	Tolerance
Coating thickness above copper (soldermask)	T1(C)	10 to 18 µm	± 5 µm
Coating thickness above substrate (soldermask)	T2(C)	≥ 10 µm	± 5 µm
Dielectric coating (soldermask)	ε_r(C)	3.4	± 0.1
Trace thickness L1 (Cu + plating)	T1(T)	29.3 µm	< 6 µm
Substrate height L1/L2	H1(S)	1.47 mm	± 10%
Dielectric substrate L1/L2	ε_{r1}(C)	4.2	± 0.1
Trace thickness L2 (Cu + plating)	T2(T)	29.3 µm	< 6 µm
Width error of trace	We(T)	12.7 µm	> 8 µm
Minimum trace width	Wt_{min}(T)	0.05 mm	± 20%

Table 3. 2-layer PCB - Reference values (continued)

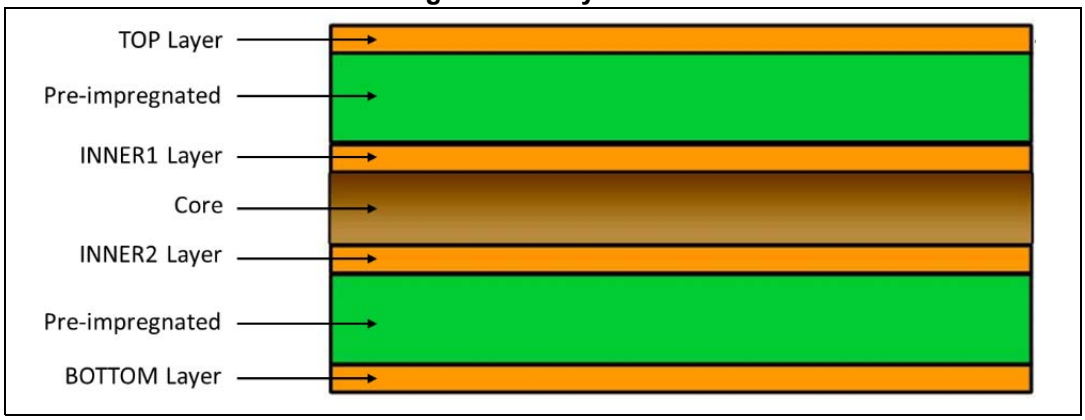
Parameter	Symbol	Value	Tolerance
Minimum isolation width	$Wt_{min}(T)$	0.01 mm	± 20%
Minimum hole diameter	$D_{min}(HS)$	0.2 mm	± 0.05 mm
Minimum via diameter	$D_{min}(VS)$	0.3 mm	± 0.05 mm

4.4 4-layer PCB

With the 4-layer PCB shown in *Figure 20*, it is recommended to have the following distribution:

- TOP layer: RF signal and routing on the top layer
- INNER1 layer: routing the others parts
- INNER2 layer: power and low frequency routing, ground reference under RF zone(s)
- BOTTOM layer: low frequency routing

Figure 20. 4-layer PCB



The 4-layer PCB solution is more complicated and expensive. The laser-filled and the buried vias have to be used to connect the tracks to the internal balls.

The 4-layer PCB definition of the reference board for the WLCSP100 is shown in *Figure 21* and the values are summarized in *Table 3*.

Figure 21. 4-layer PCB - Reference board for WLCSP100

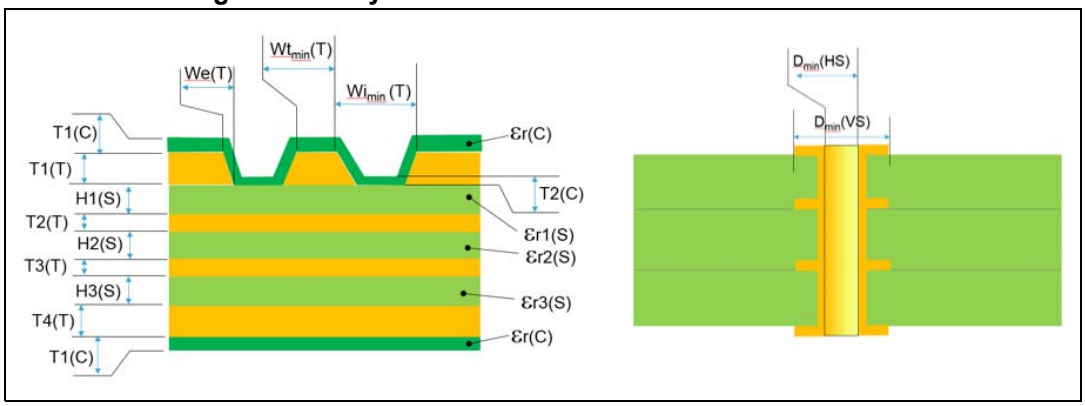


Table 4. 4-layer PCB - Reference values

Parameter	Symbol	Value	Tolerance
Coating thickness above copper (soldermask)	T1(C)	10 to 18 µm	± 5 µm
Coating thickness above substrate (soldermask)	T2(C)	≥ 10 µm	± 5 µm
Dielectric coating (soldermask)	ε_r(C)	3.4	± 0.1
Trace thickness L1 (Cu + plating)	T1(T)	29.3 µm	< 6 µm
Substrate height L1/L2	H1(S)	1.25 mm	± 10%
Dielectric substrate L1/L2	ε_{r1}(C)	4.2	± 0.1
Trace thickness L2 (Cu + plating)	T2(T)	30 µm	< 6 µm
Substrate height L2/L3	H1(S)	1.14 mm	± 10%
Dielectric substrate L2/L3	ε_{r2}(C)	4.2	± 0.1
Trace thickness L3 (Cu + plating)	T2(T)	30 µm	< 6 µm
Substrate height L3/L4	H1(S)	1.25 mm	± 10%
Dielectric substrate L3/L4	ε_{r3}(C)	4.2	± 0.1
Trace thickness L4 (Cu + plating)	T2(T)	29.3 µm	< 6 µm
Width error of trace	We(T)	12.7 µm	> 8 µm
Minimum trace width	Wt_{min}(T)	0.05 mm	± 20%
Minimum isolation width	Wt_{min}(T)	0.01 mm	± 20%
Minimum hole diameter	D_{min}(HS)	0.2 mm	± 0.05 mm
Minimum via diameter	D_{min}(VS)	0.3 mm	± 0.05 mm

5 Layout recommendations

5.1 2-layer PCB

Figure 22. PCB layout for UFQFPN48 (left to right: all, top and bottom layers)

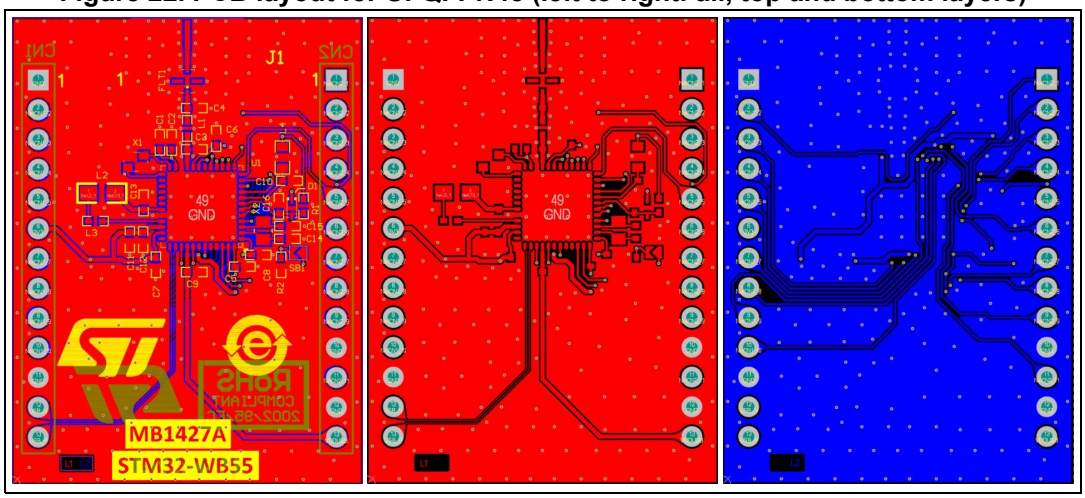


Figure 23. PCB layout for VFQFPN68 (left to right: all, top and bottom layers)

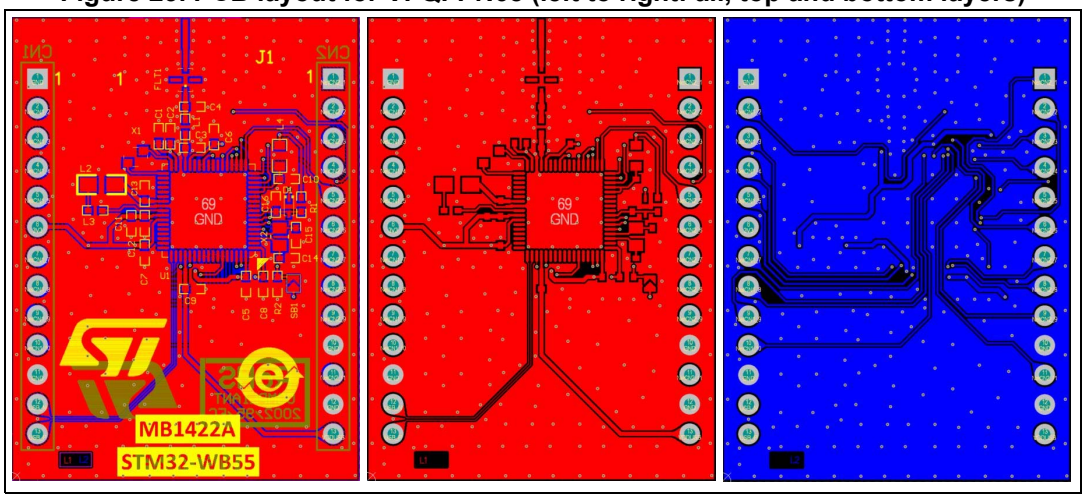
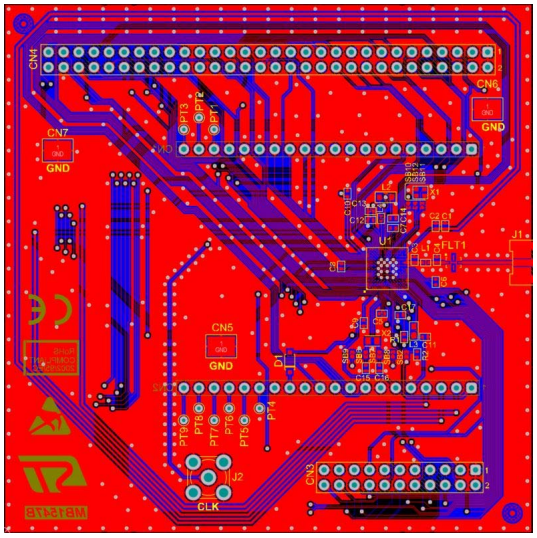
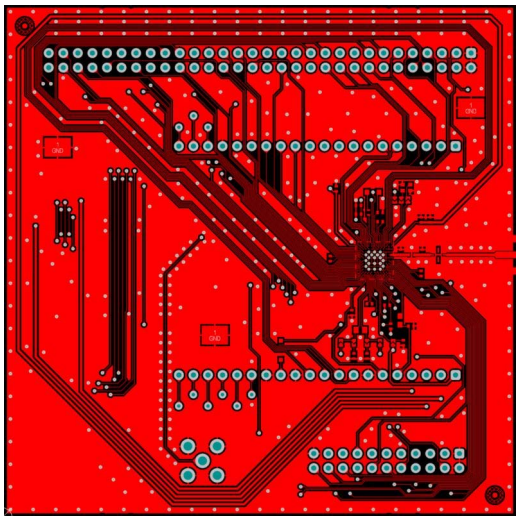


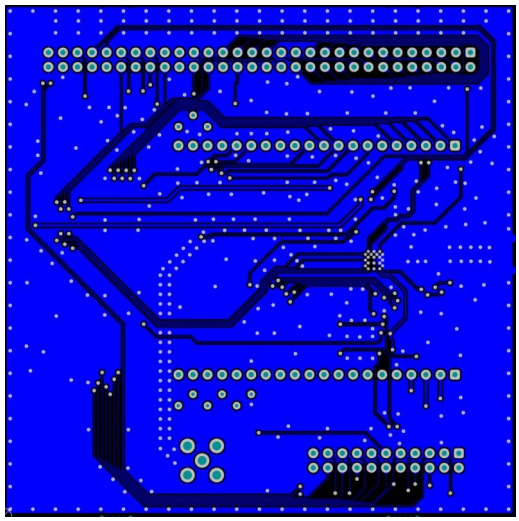
Figure 24. PCB layout for UFBGA129



All layers



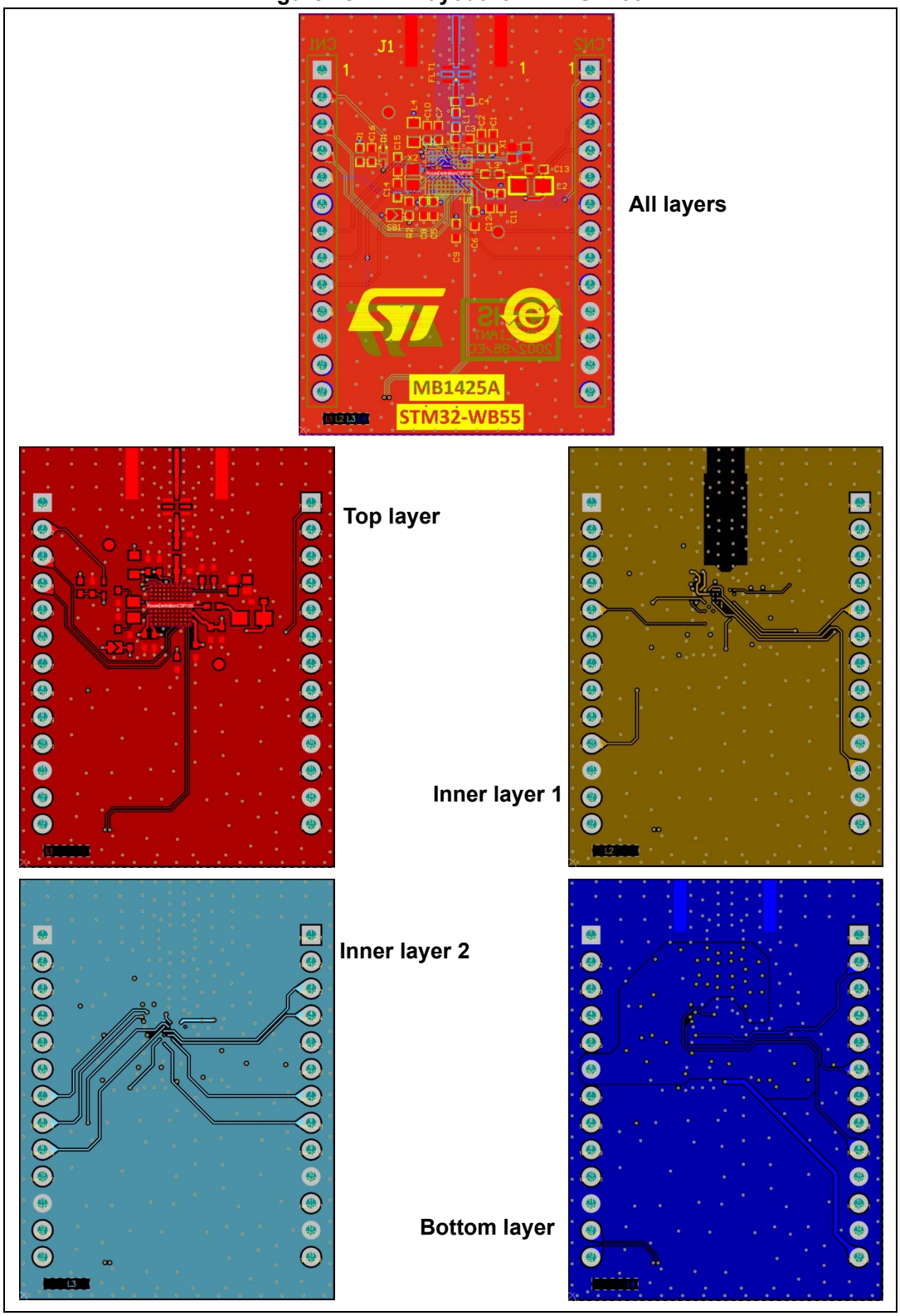
Top layer



Bottom layer

5.2 4-layer PCB

Figure 25. PCB layout for WLCSP100



5.3 Critical parts

The three critical parts in the layout are the RF, the SMPS and the LSE.

5.3.1 RF

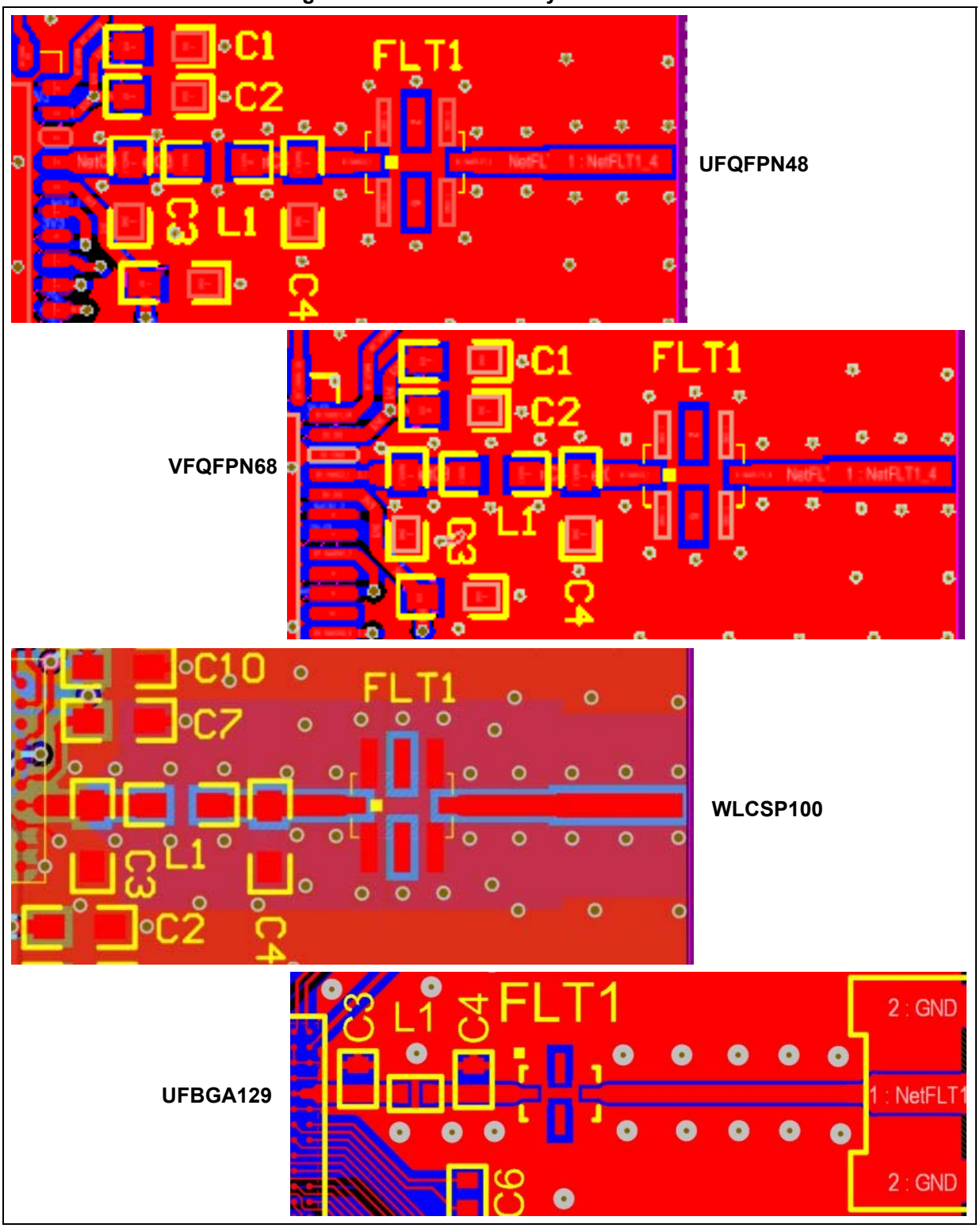
To obtain the best RF performance (in particular the maximum transmission power, the optimum reception sensitivity and a sufficient spurious and harmonic rejection), a matching network is required between the RF1 output pin and the RF low-pass filter.

This network is composed by a discrete LC PI filter followed by an integrated low-pass filter. C3 and L1 have the role of adapting the RF pin impedance of the STM32WB to 50 Ω, the impedance that must be seen by the SMA. C4 and the integrated low-pass filter FLT1 are used to reject the harmonic frequencies. The values of C3, C4 and L1 depend on the reference board PCB definition, detailed in *Section 2: Reference board schematics*.

The low-pass filter FLT1 used has a mark to distinguish the direction. Respect the direction indicated on the PCB (the filter structure is not perfectly symmetric, the properties change with the mounting direction).

It is also recommended to place the matching network as near as possible to the RF output and to avoid long track between each component of this matching network. The track between the output of the low-pass filter FLT1 and the SMA connector can have a variable length, depending upon the application, provided that its impedance is always 50 Ω.

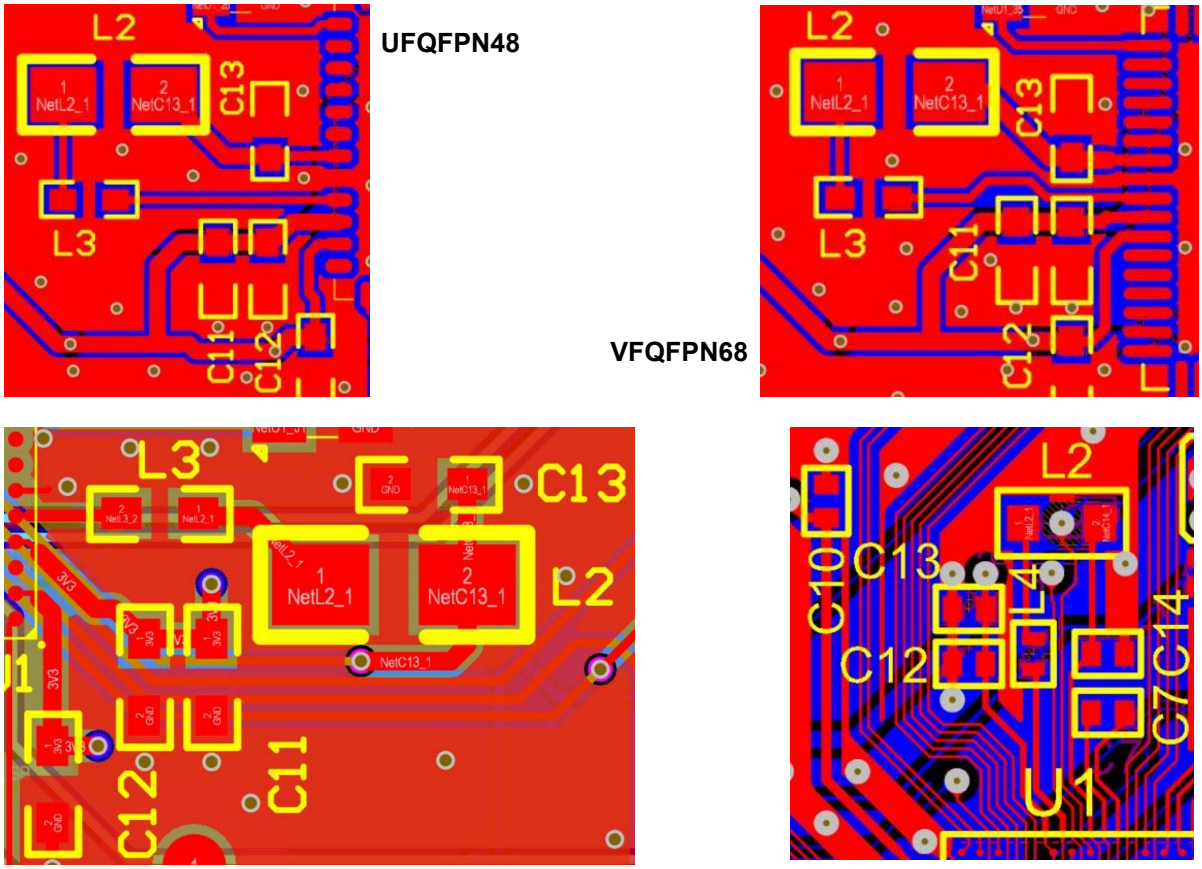
Figure 26. Detail of PCB layout for the RF



5.3.2 SMPS

In addition to the recommendations given in *Section 3.3: SMPS*, to avoid important current loop when the STM32WB is in SMPS mode, it is recommended to place C11, C12 and C13 as close as possible to their respective pins on STM32WB. Do not forget to connect the solder pad to ground to have a strong current return path.

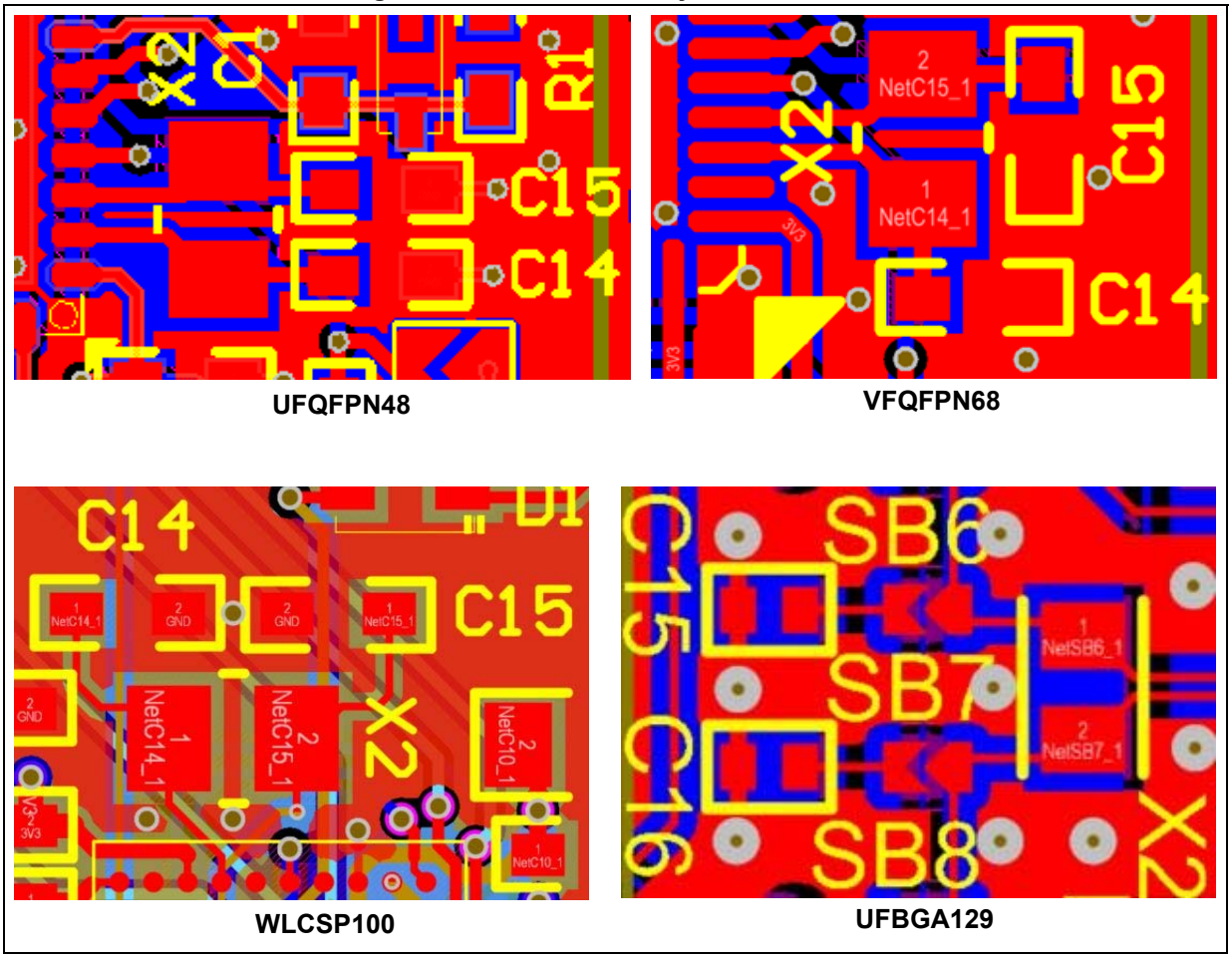
Figure 27. Detail of PCB layout for the SMPS



5.3.3 LSE

As indicated in *Section 3.4: External crystal*, place X2, C14 and C15 as close as possible to their respective pins.

Figure 28. Detail of PCB layout for the LSE



6 Reference boards with IPD

The goal of the IPD (integrated passive device) is to replace the discrete matching network plus the integrated low-pass filter keeping equivalent TX/RX performance. *Figure 29* shows the differences between the two approaches, using as example the QFN48 package.

Figure 29. Different matching networks (discrete components on the left, IPD on the right)

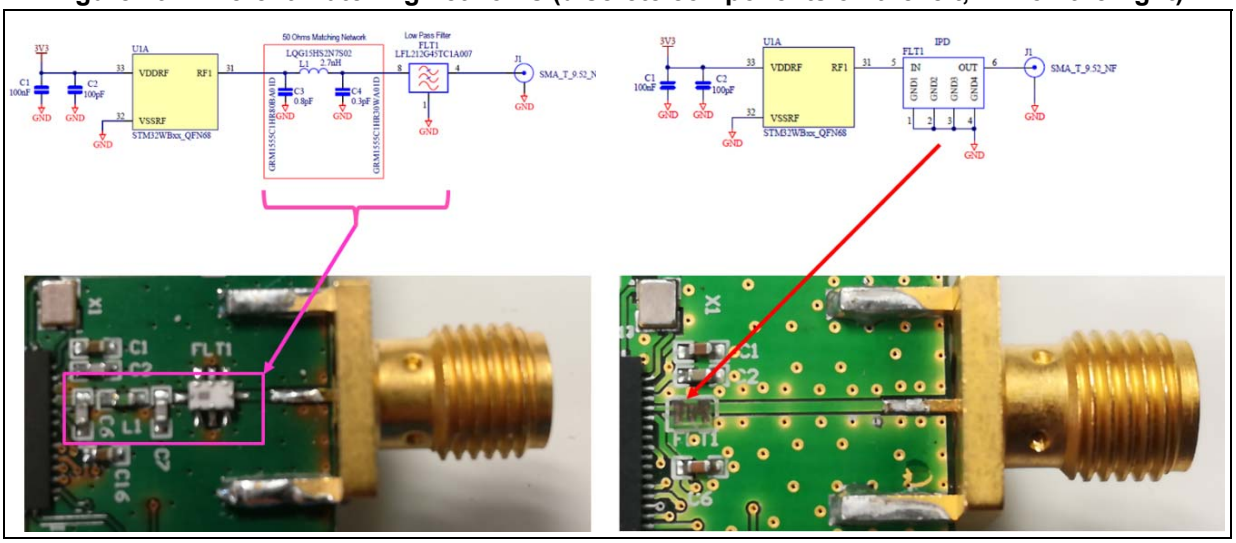


Table 5. References

Package	IPD reference	Document
QFN48	MLPF-WB55-01E3	DS12804[1], *2.4 GHz low pass filter matched to STM32WB55Cx/Rx*
QFN68		
UFBGA129		
WLCSP100	MLPF-WB55-02E3	DS13176[1], *2.4 GHz low pass filter matched to STM32WB55Vx*

1. Available on *www.st.com*.

Transmission and insertion loss performance are shown, respectively, on the left and on the right side of *Figure 30* (MLPF-WB55-01E3) and of *Figure 31* (MLPF-WB55-02E3).

Figure 30. RF performance of the MLPF-WB55-01E3

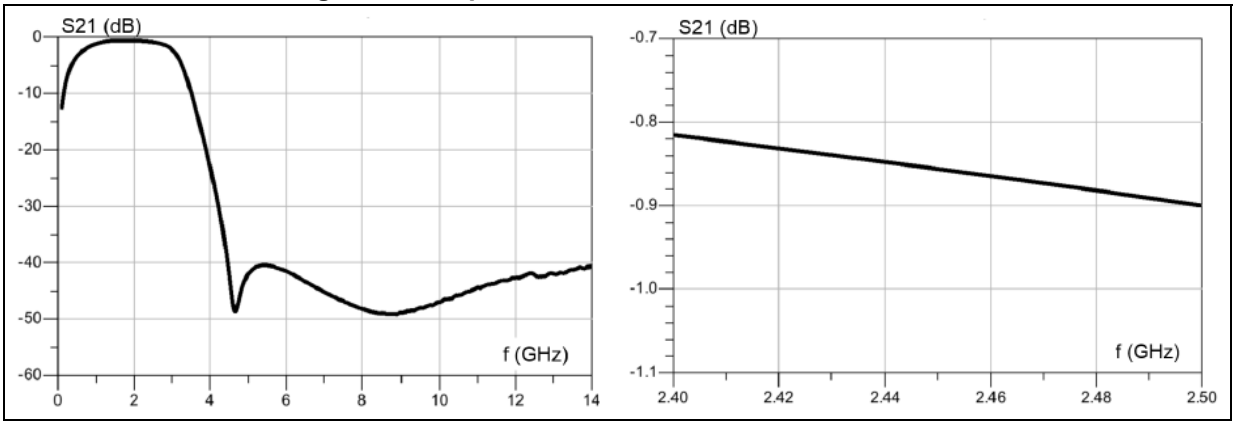
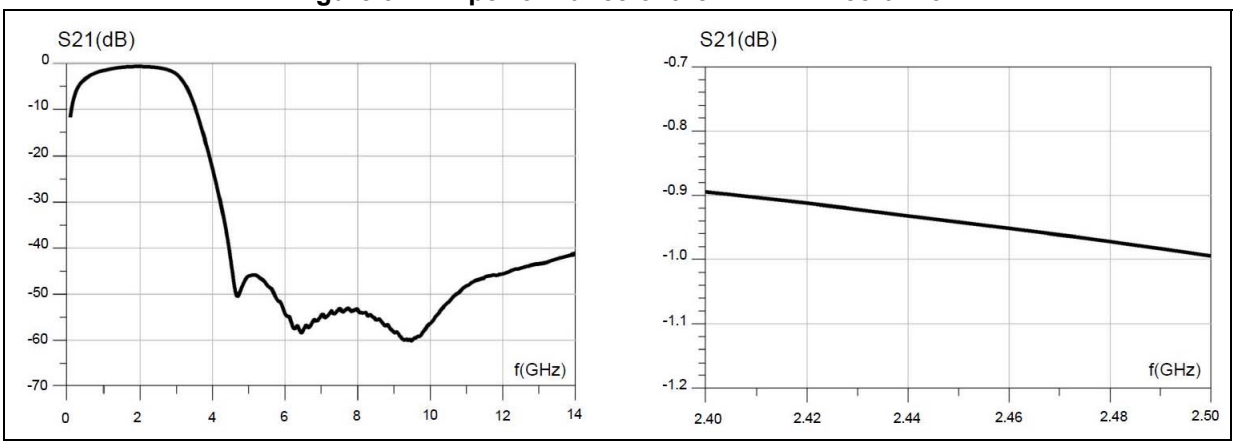
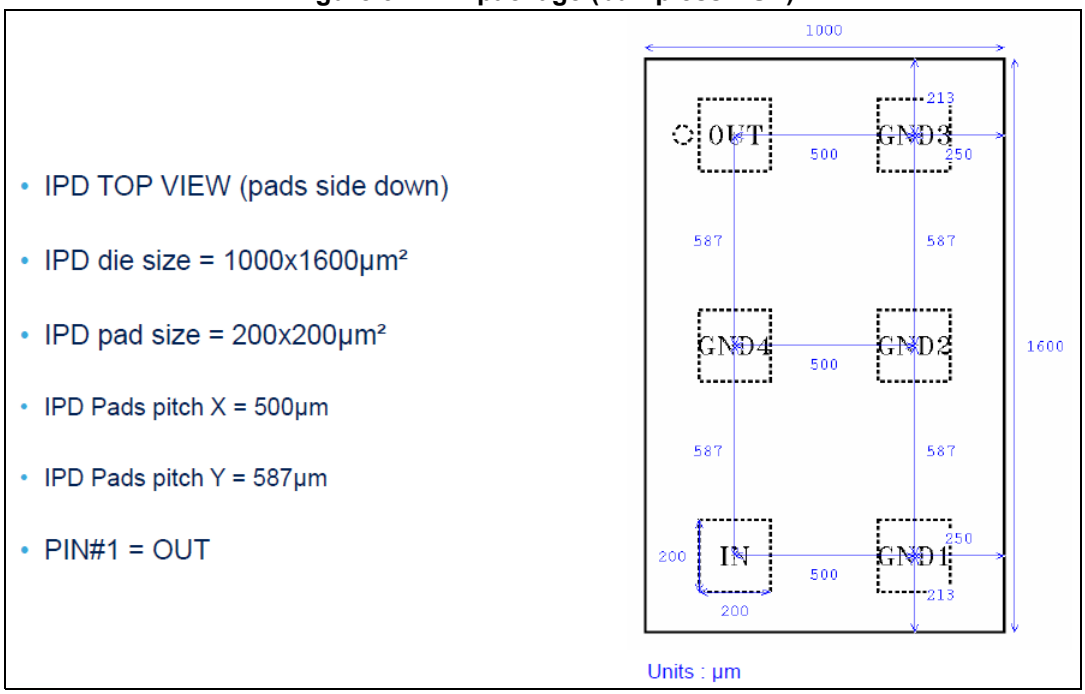


Figure 31. RF performance of the MLPF-WB55-02E3



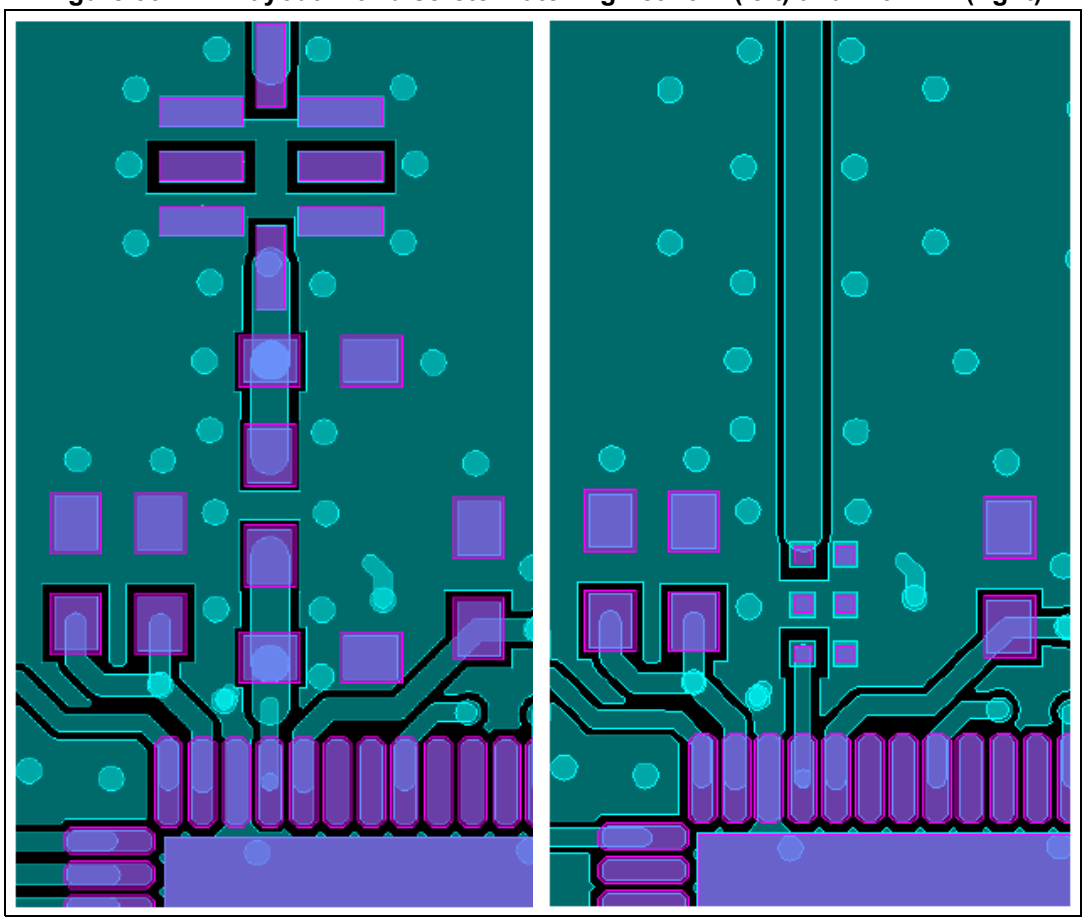
The bottom view of the IPD package is shown in *Figure 32*.

Figure 32. IPD package (bumpless CSP)



The PCB can be greatly simplified, as shown in *Figure 33*.

Figure 33. PCB layout with discrete matching network (left) and with IPD (right)



Note that the length of the track between the output of the IPD and the RF output can be further reduced to decrease the dimensions of the PCB. This improves RF performance by reducing losses due to the length of this track.

As a conclusion, the IPD reference MLPF-WB55-01E3 can replace the RF output network of the STM32WB for the QFN packages (an antenna filter is still needed) for a 2-layer PCB. The PCB size and the bill of materials will be reduced, while guaranteeing equivalent RF performance compared with the discrete RF output network. Another advantage of the IPD solution is the performance stability on volume production (lower parameter dispersion compared with the discrete components).

7 Conclusion

The STM32WB Series microcontrollers integrate a high performance RF front end.

To achieve the best TX and RX performance, several aspects have to be addressed during the PCB design:

- choice of the PCB technology (number of layers, substrate technology)
- computation of the antenna matching and filtering network
- floor plan and critical RF component placement and routing
- placement of the SMPS and LSE components (if used)

This application note provides useful guidelines to help the user to reach the performance specified in the datasheets.

8 Revision history

Table 6. Document revision history

Date	Revision	Changes
14-Sep-2018	1	Initial release.
18-Jan-2019	2	Added *Section 6: Reference boards with IPD*.
28-Jan-2019	3	Changed document classification, from ST restricted to public.
24-Sep-2019	4	Updated *Introduction* and *Section 3.3: SMPS*.
25-Oct-2019	5	Introduced WLCSP100 package, hence updated *Introduction*, *Section 2: Reference board schematics* and *Section 3.3: SMPS*. Updated *Table 1: External components*. Updated *Figure 8: UFQFPN48 reference board*, *Figure 9: VFQFPN68 reference board*, *Figure 19: 2-layer PCB - Reference boards for UFQFPN48, VFQFPN68 and UFBGA129*, *Figure 21: 4-layer PCB - Reference board for WLCSP100*, *Figure 22: PCB layout for UFQFPN48 (left to right: all, top and bottom layers)*, *Figure 23: PCB layout for VFQFPN68 (left to right: all, top and bottom layers)*, *Figure 25: PCB layout for WLCSP100*, *Figure 26: Detail of PCB layout for the RF*, *Figure 27: Detail of PCB layout for the SMPS* and *Figure 28: Detail of PCB layout for the LSE*. Added *Section 5.1: 2-layer PCB* and *Section 5.2: 4-layer PCB*. Removed MB1355C board and related former *Section 3: Nucleo board (MB1355C) schematics* and *Section 6: 4-layer PCB Nucleo board MB1355C*.
25-Jan-2020	6	Introduced UFBGA129 package, hence updated *Introduction*, *Section 4.3: 2-layer PCB* and *Section 6: Reference boards with IPD*. Updated *Figure 8: UFQFPN48 reference board*, *Figure 9: VFQFPN68 reference board*, *Figure 11: WLCSP100 reference board*, *Figure 26: Detail of PCB layout for the RF*, *Figure 27: Detail of PCB layout for the SMPS* and *Figure 28: Detail of PCB layout for the LSE*. Updated caption of *Figure 19* and of *Figure 21*. Added *Figure 10: UFBGA129 reference board*, *Figure 24: PCB layout for UFBGA129* and *Figure 31: RF performance of the MLPF-WB55-02E3*. Added *Table 5: References*.

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