AN3265

UPD301A USB Power Delivery Operation

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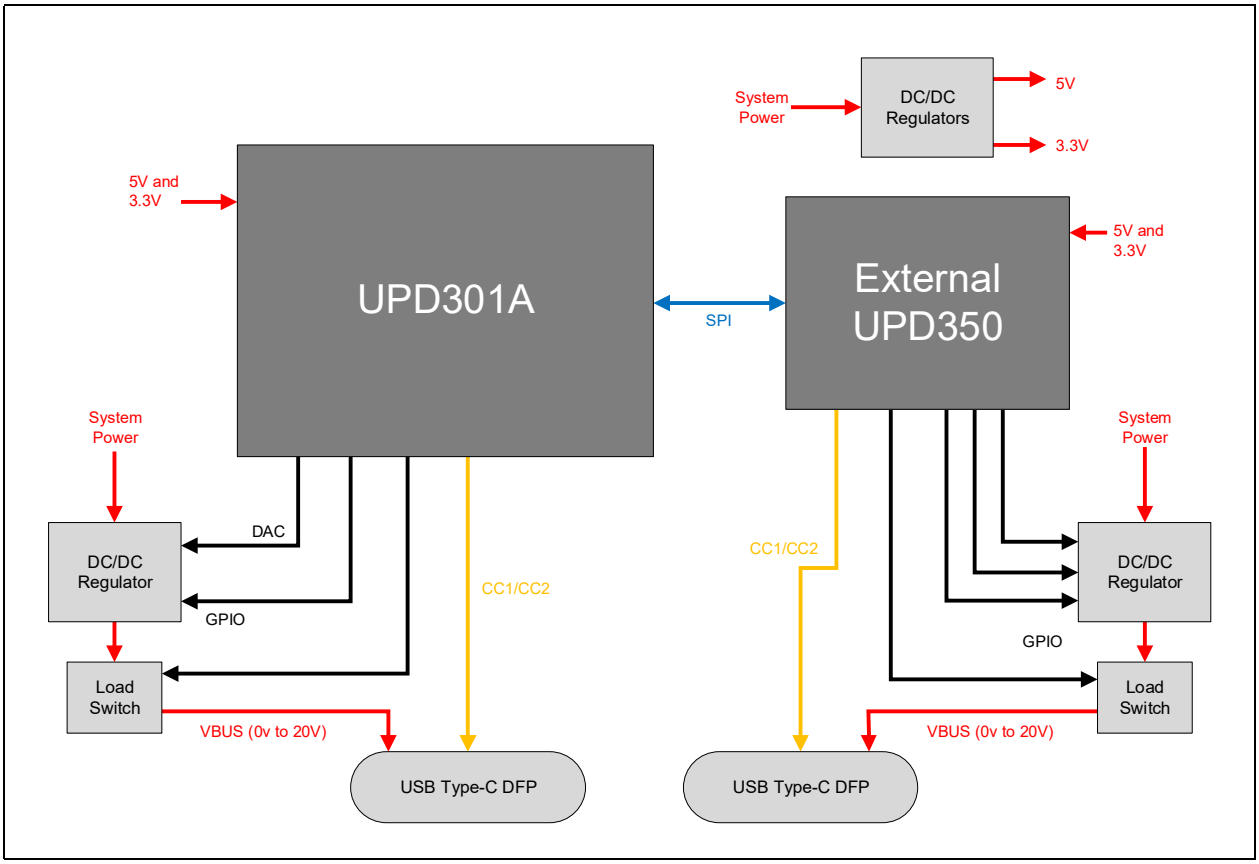
1.0 INTRODUCTION

The UPD301A is a single-chip USB Power Delivery (PD) solution for stand-alone source-only applications. USB Power Delivery functionality can be expanded to a 2-port source-only application when one UPD301A is used in conjunction with a UPD350 USB Power Delivery port controller. The UPD301A is preprogrammed with PD firmware to support the standard PD power profiles.

1.1 Features

- Up to two USB Type-C®, PD Power Source-Only Downstream Facing Ports (DFP)
- Supports system designs capable of up to 100W per PD port
- Fixed PDO voltages: 5V, 9V, 15V, and 20V
- USB Power Delivery 3.0 compliant MAC

FIGURE 1-1: SIMPLIFIED BLOCK DIAGRAM OF TWO PD PORT IMPLEMENTATION



1.2 Sections

This document includes the following topics:

- Section 1.0, "Introduction"
- Section 2.0, "Power Delivery Operation"
- Section 3.0, "System-Level Requirements and Design Guidelines"
- Section 4.0, "System Block Diagrams"
- Section 5.0, "VBUS Power Requirements"

1.3 References

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *UPD301A Data Sheet*
- *System Management Bus Specification, Version 1.0*
- *USB Power Delivery Specification Rev. 3.0, Version 1.2, June 21, 2018 and ECNs* (Note 1 and Note 2)
- *USB Type-C™ Cable and Connector Specification Revision 1.4, March 29, 2019* (Note 1 and Note 2)

Note 1: It is recommended that the latest versions of the above documents be downloaded and reviewed in addition to this document. If any information within this document conflicts with the information presented in the specifications below, the information contained in the USB-IF specification document supersedes.

2: System and firmware requirements may be impacted by future USB specification revisions.

2.0 POWER DELIVERY OPERATION

2.1 Supported PD Features

- Source-Only Power Operation
- Fixed Supply Power Data Objects (PDOs)
  - 5V up to 5A
  - 9V up to 5A
  - 15V up to 5A
  - 20V up to 5A
- Unsupported features:
  - Power and Data Role Swaps not supported
  - Alternate Modes not supported
  - Programmable Power Supply

2.2 PD Operation Summary

A USB Type-C connector is a high-speed, high-power-capable symmetrical connector with 24 total pins. USB Power Delivery v2.0/v3.0 is a complementary feature, but it is not explicitly required for USB Type-C. A Type-C port without Power Delivery is limited to:

- 5V VBUS only
- Up to 3A
- Data Downstream Facing Port (DFP) must always be a power source.
- Data Upstream Facing Port (UFP) must always be a power sink.

Note:	In a basic Type-C implementation, power and data roles can be toggled before initial attach through the toggling DRP mechanism, or immediately after initial attach through the Try.SRC/Try.SNK mechanism. After an initial connection has been resolved, power and data role cannot be changed at any time during a connection. A power source can never be a data UFP, and a power sink can never be a data DFP in a basic Type-C system.

Adding USB Power Delivery to a Type-C port enables the following main features (many advanced features are omitted from this list):

- VBUS Voltages greater than 5V
- Amperage greater than 3A
- Data Role Swap at any time during connection
- Power Role Swap at any time during connection
- Alternate Mode Operation

2.2.1 GENERAL OPERATION

When disconnected, a Type-C connector must ensure VBUS is within the specified range for 0V. VBUS is only applied when a device is attached, and a short debounce timer has expired. All Type-C connections begin at 5V, and then may negotiate to a high voltage, amperage, or both through USB Power Delivery messaging.

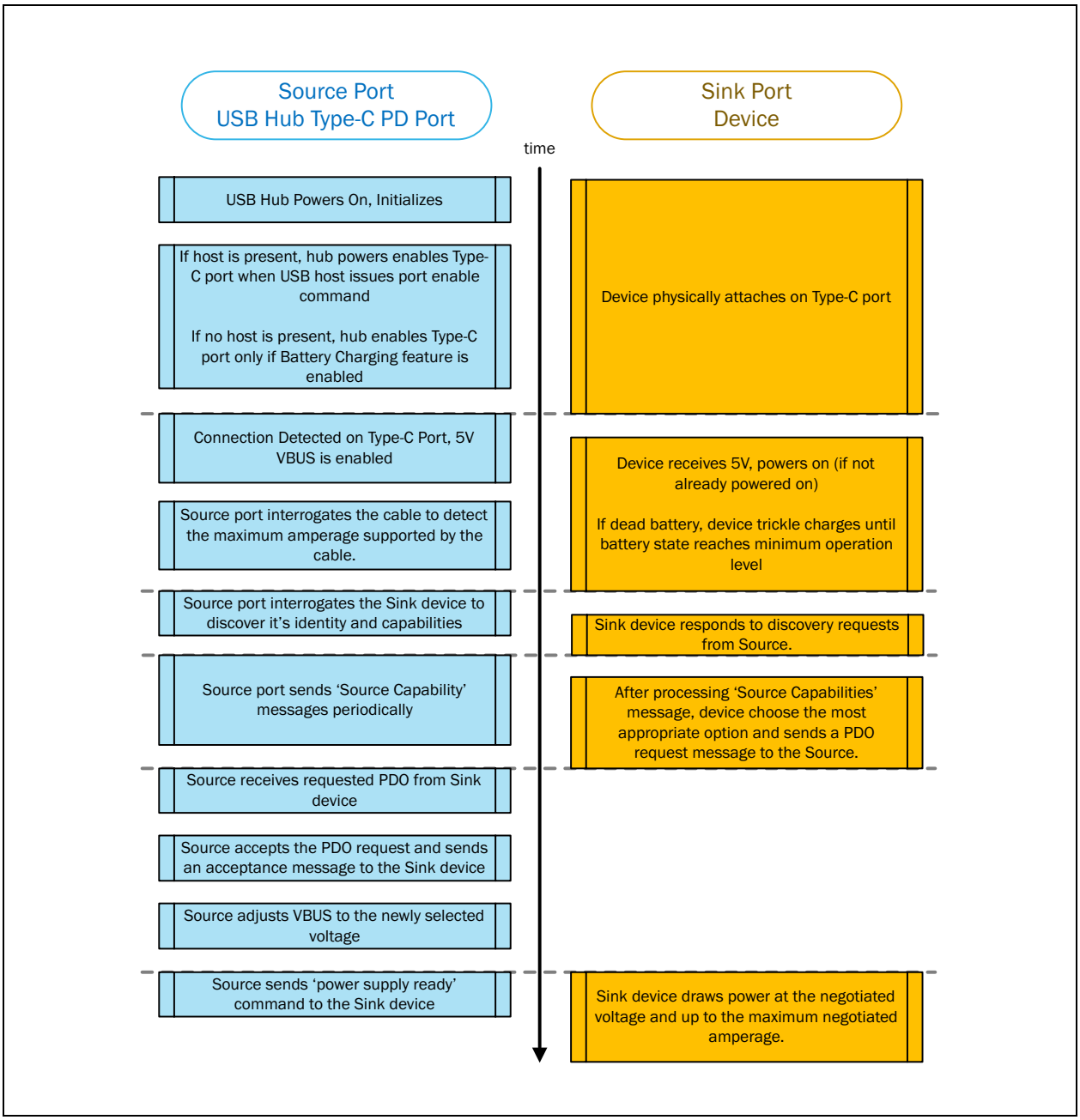
UPD301A operates as a fixed PD Source-Only DFP. It is always the USB Power Delivery Bus master and is responsible for initiating most communication.

After a connection is detected, the UPD301A first performs a cable capability discovery. A cable supporting current greater than 3A must have embedded power delivery controllers and must respond to USB PD protocol.

Once the UPD301A has discovered the current capability of the cable, it begins to advertise its Source Capabilities to the attached device. A device that supports PD must choose only one voltage option, and it may request any amperage up to the maximum amperage advertised by the power source. A device that does not support PD will not respond, and the connection will remain at 5V.

An example of a typical connection sequence of events from source and sink perspective is shown in Figure 2-1.

FIGURE 2-1: TYPICAL POWER DELIVERY SOURCE-ONLY CONNECTION SEQUENCE



A device may choose to re-negotiate power and select a new power option at any time.

A device is responsible for drawing current up to, but never above, the amperage requested. It is not the responsibility of the power source to dynamically limit current. Only a fixed, short circuit level overcurrent protection threshold is required of the power source.

A power source can also never force a device to draw current near the levels the device has requested. For example, if a device requests 3A current but only draws a small amount (in other words, less than 500 mA), there is nothing a power source can do to force the device to take additional power, or to give the power back so that it can be added back to the overall system budget.

All requests for power or data role swaps from the attached device are rejected.

UPD301A will not communicate any alternate mode capabilities.

If at any time the attached device issues a Hard Reset or Soft Reset command, the UPD301A will respond by removing VBUS (discharging to 0V) and then restarting the connection as if it were a new connection.

All fault conditions are handled by immediately removing VBUS (discharging to 0V), resetting the DC/DC controller and load switch, and then communicating the fault to the USB host. The connection may be restarted if the USB host clears the fault condition and re-enables the port through standard USB port control protocol.

2.3 PDO Calculation

The USB Power Delivery specification defines Power Data Objects (PDOs) as mechanism to communicate the source or sink power capability of a port. Each PDO communicates a source or sink capability, and the information carried within the PDO varies depending on the type of PDO (Fixed, Battery, Variable, or Augmented). Simply put, the objective of the PDO is to describe a specific operating voltage or voltage range and a maximum current. The specification allows for a maximum of seven total PDOs per port.

UPD301A supports up to four fixed PDOs with the standard USB Power Delivery PDP voltages of 5V, 9V, 15V, and 20V. The Power Delivery Profile (PDP) of each port is defined by a strap resistor. Each port has a pin on the UPD301A, PDP_SELx, which must be strapped with a resistor outlined in Table 2-1 to select the PDP.

TABLE 2-1: PDP_SELX RESISTOR ENCODING

PDP_SELx Resistor Value	PDP	PDO 1	PDO 2	PDO 3	PDO 4
200kΩ Pull-Down	7.5W	5V @ 1.5A	—	—	—
200kΩ Pull-Up	15W	5V @ 3A	—	—	—
4.7kΩ Pull-Down	27W	5V @ 3A	9V @ 3A	—	—
4.7kΩ Pull-Up	45W	5V @ 3A	9V @ 3A	15V @ 3A	—
10Ω Pull-Down	60W	5V @ 3A	9V @ 3A	15V @ 3A	20V @ 3A
10Ω Pull-Up	100W	5V @ 5A	9V @ 5A	15V @ 5A	20V @ 5A

2.4 Type-C Cable Power Capabilities

The maximum amount of current that is allowed to be advertised in the Source Capabilities PDOs is also limited by the power capability of the Type-C cable that is inserted. If a 3A cable is detected, then no advertised PDO may offer a current level above 3A. If a 5A cable is detected, then the maximum calculated current level (up to 5A maximum) may be advertised.

3.0 SYSTEM-LEVEL REQUIREMENTS AND DESIGN GUIDELINES

3.1 Single Port DC/DC Control and UPD301A Pin Assignments

The DC/DC regulator for a single port solution must be controlled using the DAC output from the UPD301A.

3.1.1 DAC DC/DC CONTROL

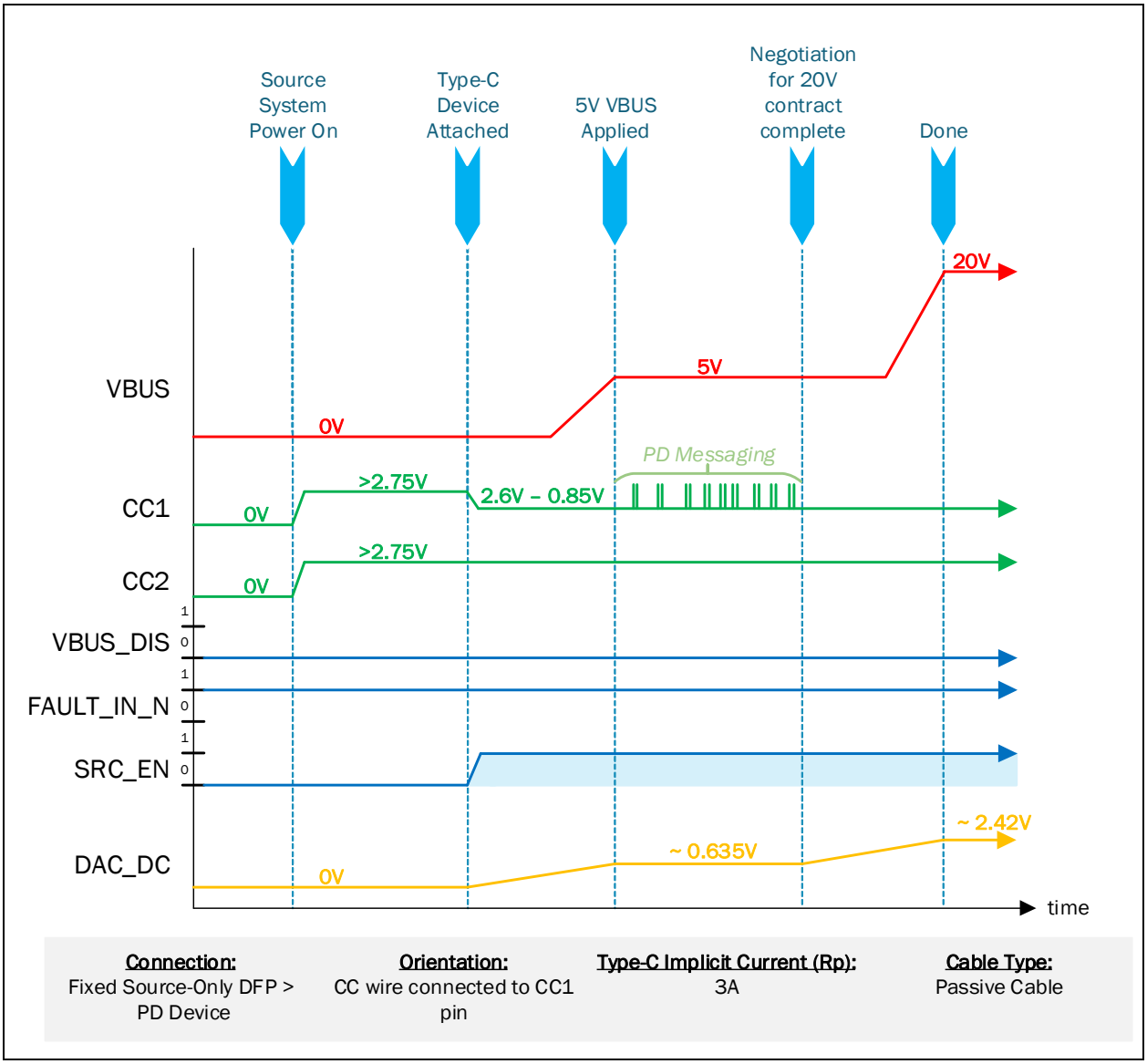
The default pin assignments and behaviors for the UPD301A are described in Table 3-1.

TABLE 3-1: UPD350 GPIO ASSIGNMENTS, GPIO CONTROL MODE

Pin	Name	Direction	Mode	Description
1	ORIENTATION_N	Output	Active High	Optionally used to control an external USB3 MUX for data applications.
12	DAC_DC	Analog Output	N/A	Used to control the output voltage of the DC/DC regulator. Can be connected directly to an ADC pin on the DC/DC or can be used in combination with an op amp to change the voltage of the feedback loop for the DC/DC.
17	PDP_SEL0	Input	—	Strap input used to select power delivery profile as defined in Table 2-1.
26	SRC_EN	Output	Active High	Asserts when voltage to VBUS is enabled. Connects to a load switch device such as a power FET or load switch IC.
38	VBUS_DIS	Output	Active High	Control for discharging VBUS (connecting VBUS to GND). Asserts whenever VBUS voltage must transition from a high voltage to a lower voltage state and when VBUS is disabled.
39	FAULT_IN_N	Input	Active Low	Fault input for detecting overcurrent fault, or undervoltage or overvoltage fault from an external sensing device.

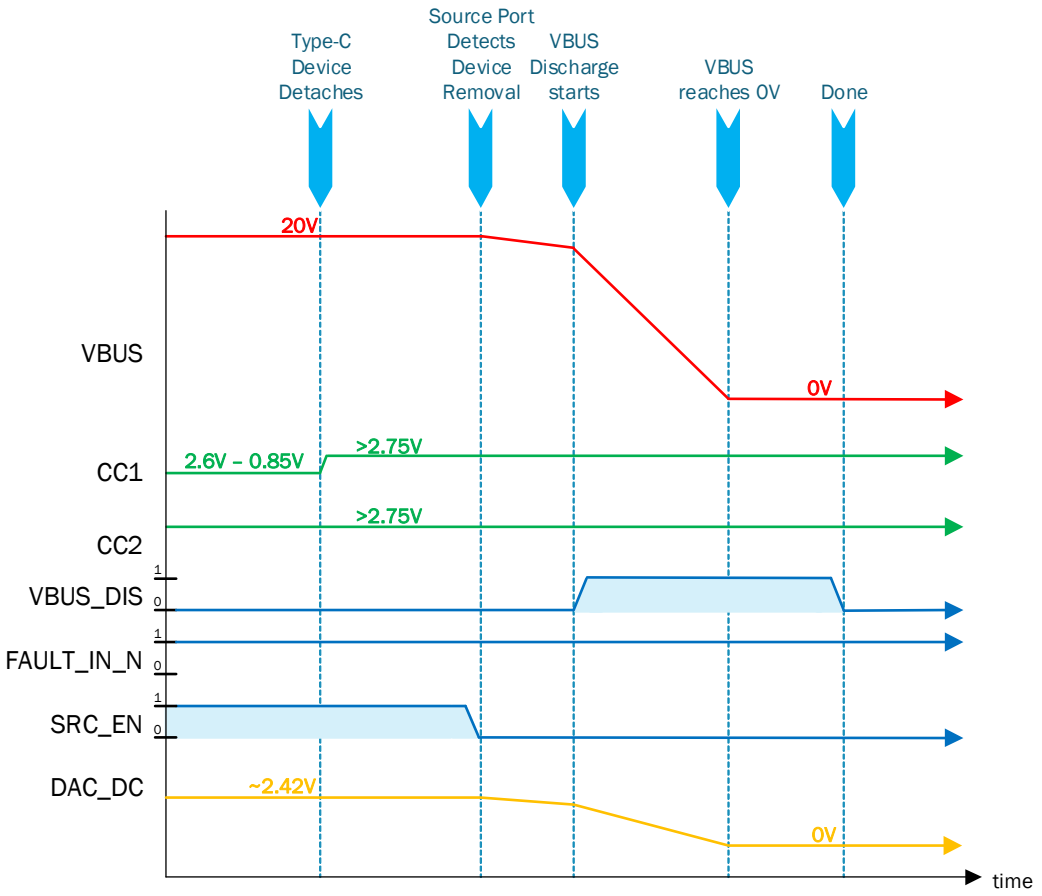
The pin behavior for a typical initialization and device connection sequence of events is shown in Figure 3-1.

FIGURE 3-1: UPD301A PIN BEHAVIOR DURING TYPICAL CONNECTION SEQUENCE



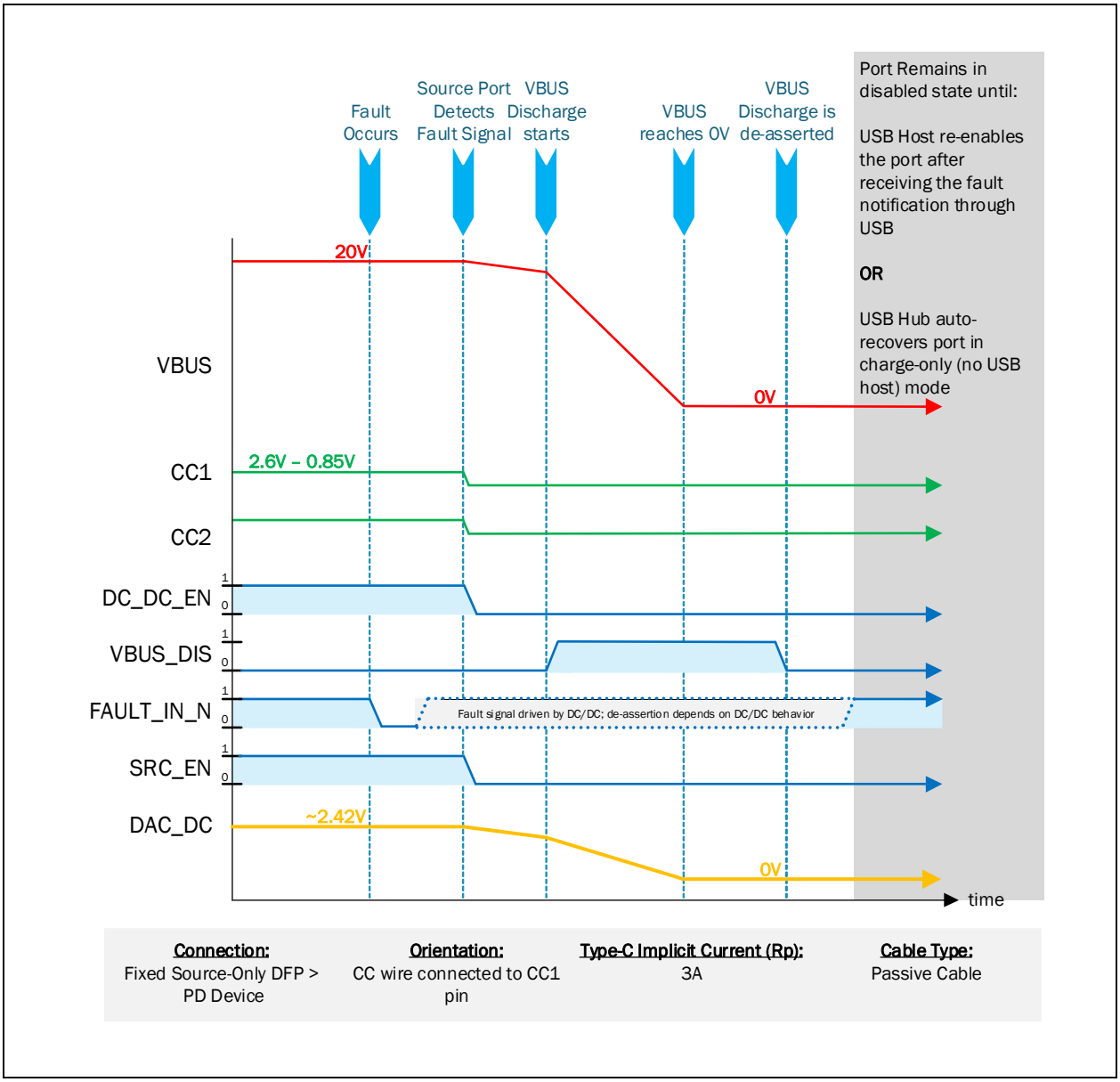
The pin behavior for a typical device disconnection is shown in Figure 3-2.

FIGURE 3-2: UPD301A PIN BEHAVIOR DURING TYPICAL DISCONNECTION SEQUENCE



The pin behavior under a typical fault condition is described in Figure 3-3.

FIGURE 3-3: UPD301A PIN BEHAVIOR DURING TYPICAL FAULT EVENT



3.2 Optional Port 2 GPIO-Based DC/DC Control

The default pin assignments and behaviors for the external UPD350 are described in Table 3-2. There is also a pin on the UPD301A that selects the PDP of the second port.

TABLE 3-2: UPD301A PIN ASSIGNMENT FOR OPTIONAL PORT 2

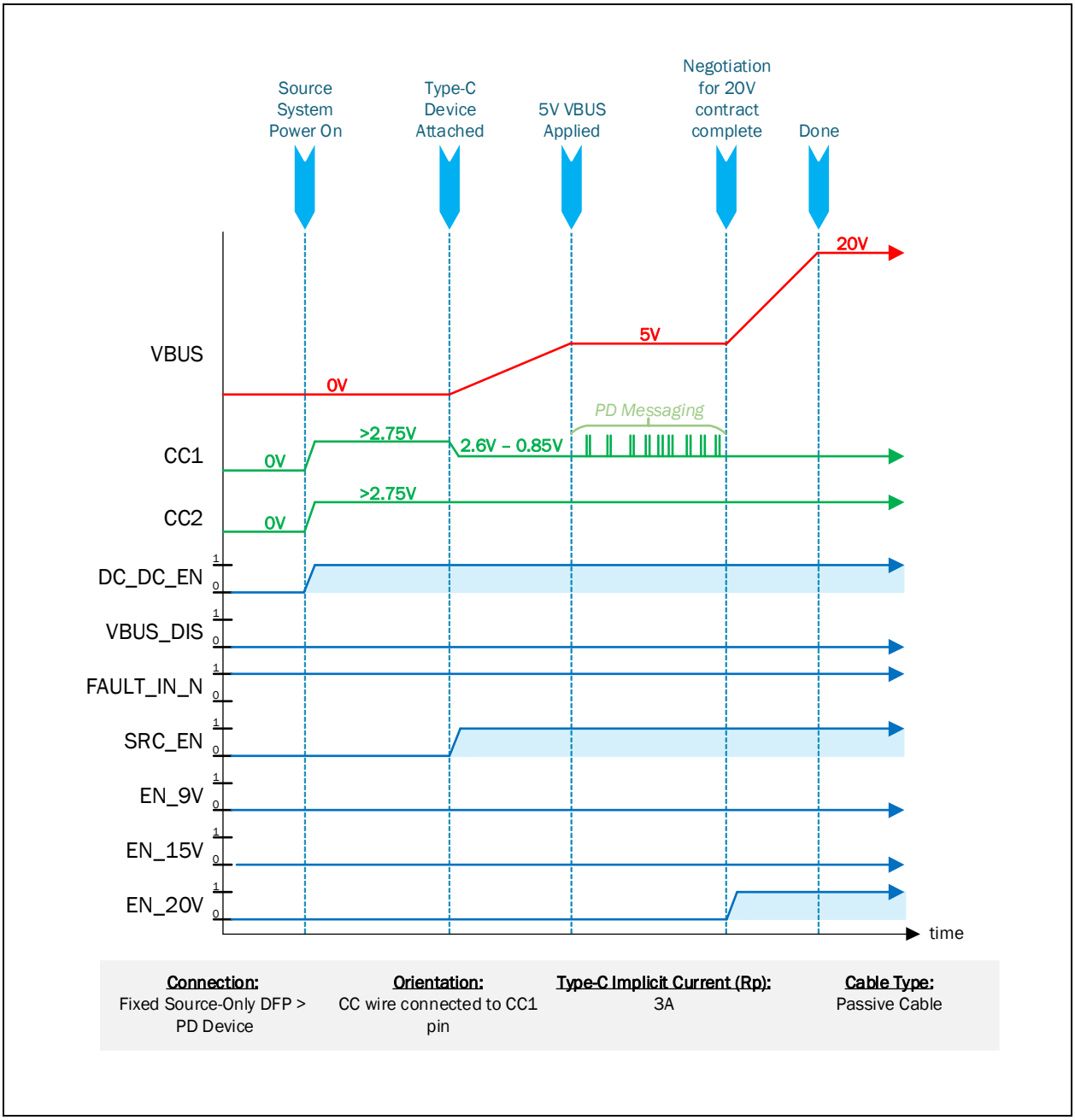
Pin	Name	Direction	Mode	Description
18	PDP_SEL1	Input	—	Strap input used to select power delivery profile as defined in Table 2-1.

TABLE 3-3: UPD350 GPIO ASSIGNMENTS, GPIO CONTROL FOR OPTIONAL PORT 2

GPIO	Pin	Name	Direction	Mode	Description
GPIO0	16	N/A	N/A	N/A	SPI_CLK
GPIO1	17	N/A	N/A	N/A	SPI_SS1
GPIO2	18	ORIENTATION_N	Output	Active High	Optionally used to control an external USB3 MUX for data applications.
GPIO3	19	SRC_EN	Output	Active High	Asserts when voltage to VBUS is enabled. Connects to a load switch device such as a power FET or load switch IC.
GPIO4	23	VBUS_DIS	Output	Active High	Control for discharging VBUS (connecting VBUS to GND). Asserts whenever VBUS voltage must transition from a high voltage to a lower voltage state and when VBUS is disabled.
GPIO5	24	FAULT_IN_N	Input	Active Low	Fault input for detecting overcurrent fault, or undervoltage or overvoltage fault from external sensing device.
GPIO6	25	DC_DC_EN	Output	Active High	Asserts any time the PD port is enabled and in active or idle state (even if Type-C is in unattached state). This enables and powers the DC/DC and must be asserted before any I^2C configuration or initialization to the DC/DC can be performed. Can be used to toggle enable or reset of a DC/DC to recover from an error condition.
GPIO7	26	EN_9V(VSEL2)	Output	Active High	Voltage Selector pins. Used to control the output voltage of the DC/DC regulator. In a typical application, these pins are used to switch in different resistors into the feedback loop to vary the output voltage. By default, a 1-pin-per-voltage implementation is implemented. VSEL[2:0]: “000” = 5V (No pins asserted) “001” = 15V (Only EN_15V asserted) “010” = 20V (Only EN_20V asserted) “100” = 9V (Only EN_9V asserted)
GPIO8	27	EN_15V_SRC(VSEL0)			
GPIO9	28	EN_20V_SRC(VSEL1)			

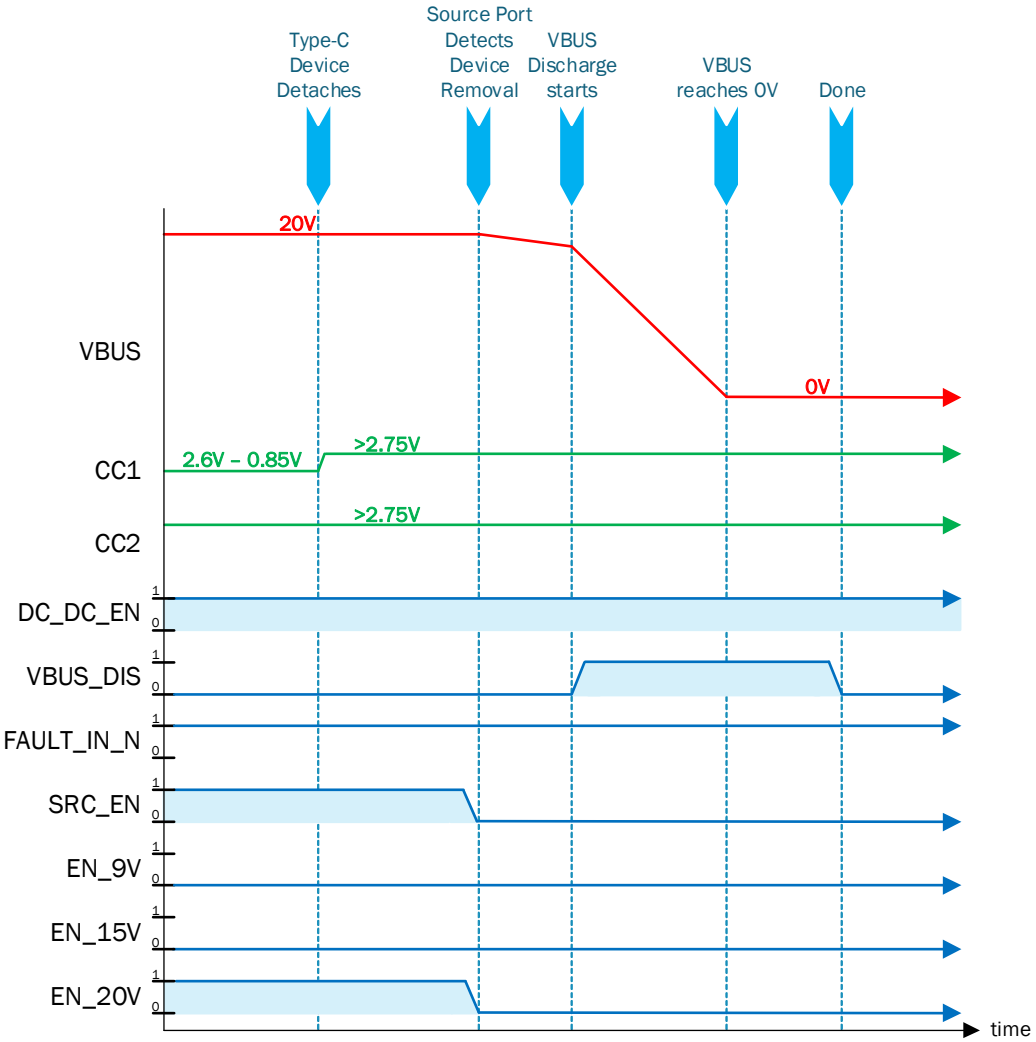
The pin behavior for a typical initialization and device connection sequence of events is shown in Figure 3-4.

FIGURE 3-4: UPD350 GPIO BEHAVIOR DURING TYPICAL CONNECTION



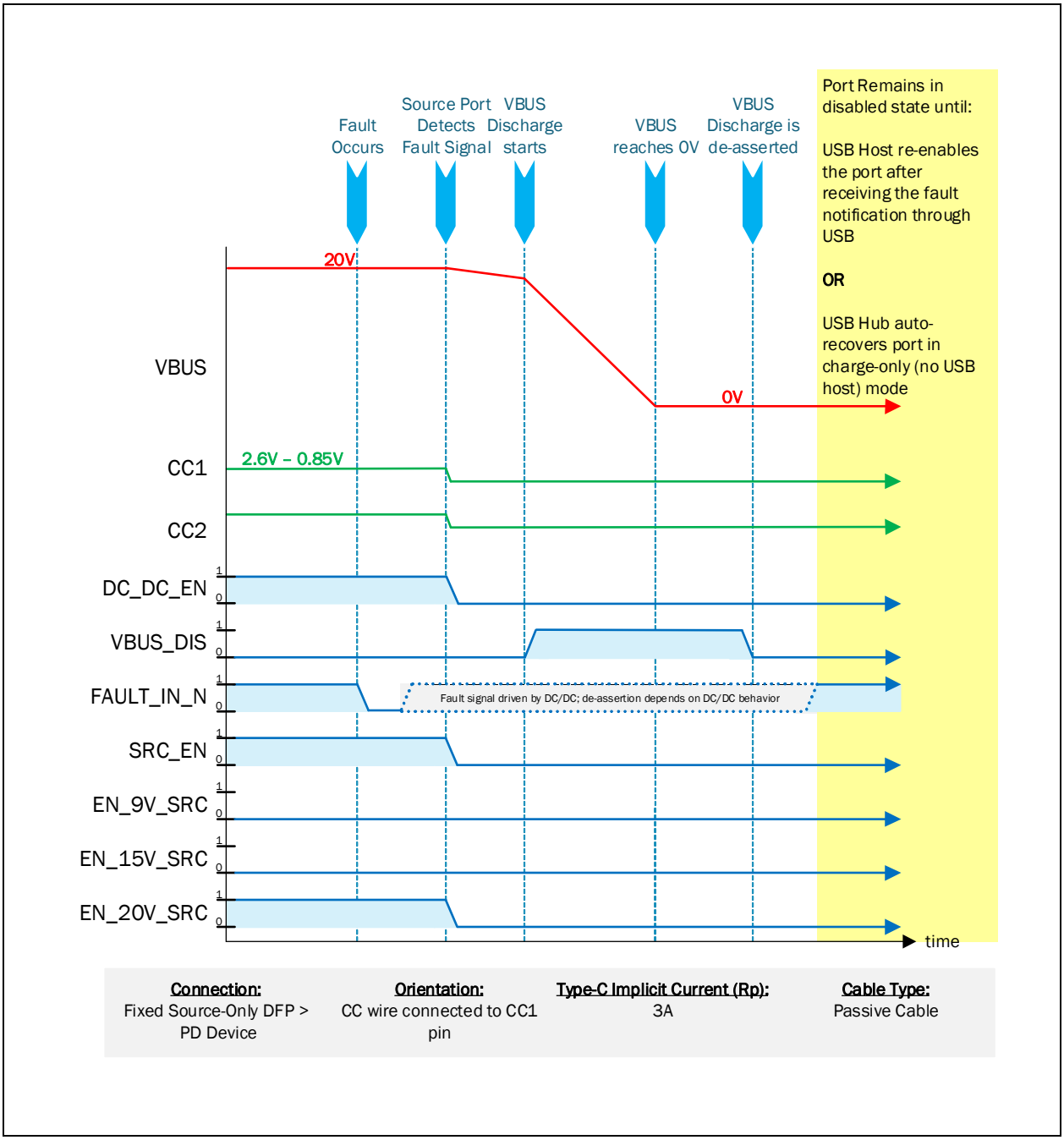
The pin behavior for a typical device disconnection is shown in Figure 3-5.

FIGURE 3-5: UPD350 GPIO BEHAVIOR DURING TYPICAL DISCONNECTION



The pin behavior under a typical fault condition is described in Figure 3-6.

FIGURE 3-6: UPD350 GPIO BEHAVIOR DURING TYPICAL FAULT EVENT



4.0 SYSTEM BLOCK DIAGRAMS

4.1 System-Level Diagrams

System-level diagrams for all supported system implementations are shown in Figure 4-1 and Figure 4-2.

FIGURE 4-1: UPD301A PORT POWER CONTROL: 1 PD PORTS, DAC CONTROL

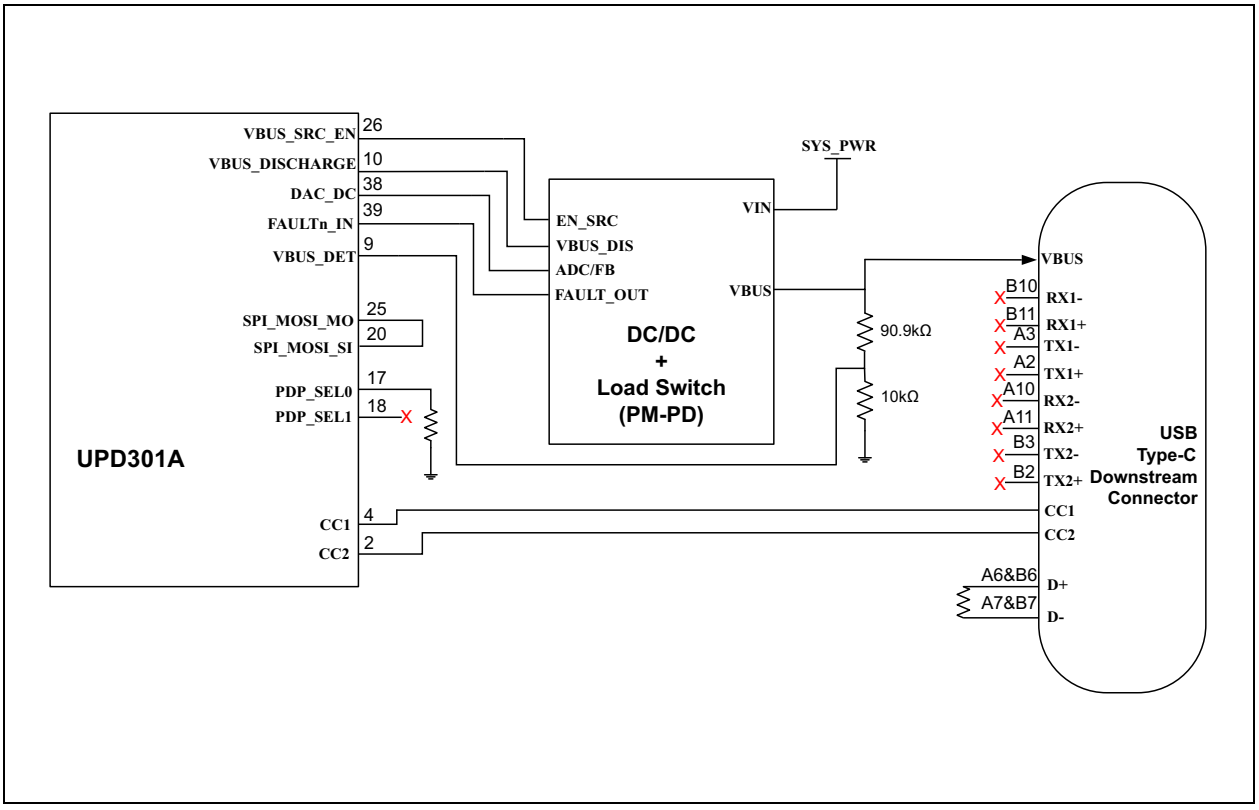
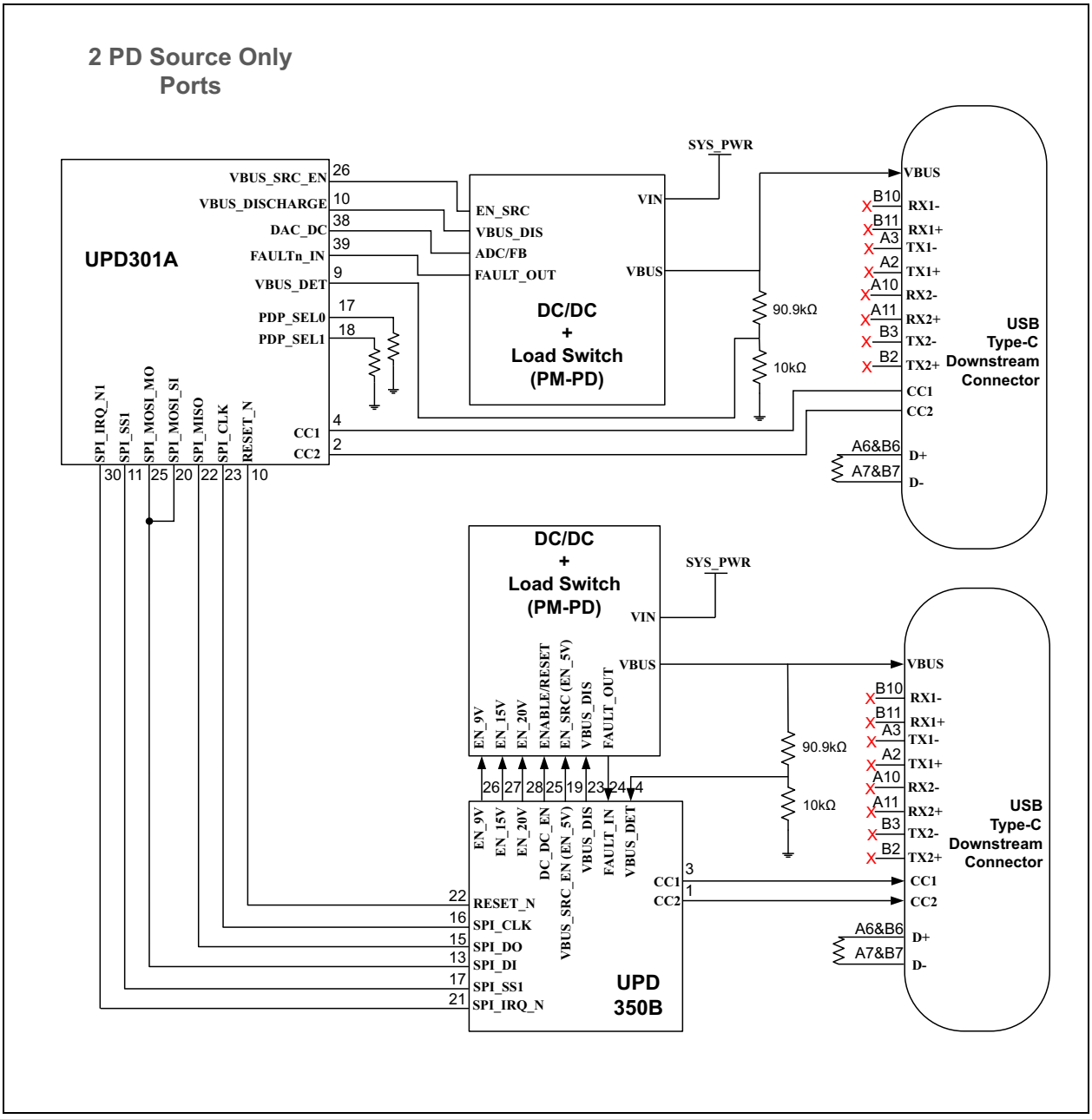


FIGURE 4-2: UPD301A PORT POWER CONTROL: 2 PD PORT, DAC/GPIO MODE



5.0 VBUS POWER REQUIREMENTS

Note: The following information is designed to aid in the understanding of the high-level requirements for VBUS power from a USB Type-C and USB Power Delivery specification standpoint. This information may be used to select an appropriate DC/DC solution for your application. After selecting a DC/DC solution for your design, it is highly recommended to acquire and refer to the documentation, including any Type-C specific application notes or reference designs, from the solution vendor.

5.1 Typical DC/DC System Examples

The power regulation for VBUS can take many forms. Four solutions (two for port 1 and another two for port 2) are shown in the following examples to show a full range of common solutions. The examples do not represent every possible solution. Individual solutions may mix and match the various components within these diagrams (or use different components altogether).

Figure 5-1 is an example of a traditional, all-analog Buck/Boost DC/DC controlled via a DAC inputting into an op amp that is tying directly into the feedback loop of the DC/DC to control the voltage. This type of design requires deep knowledge of power regulation circuitry in order to design a system that meets all of the compliance specification requirements.

FIGURE 5-1: PORT 1 ANALOG BUCK/BOOST DC/DC WITH DISCRETE FET SWITCHING USING DAC CONTROL

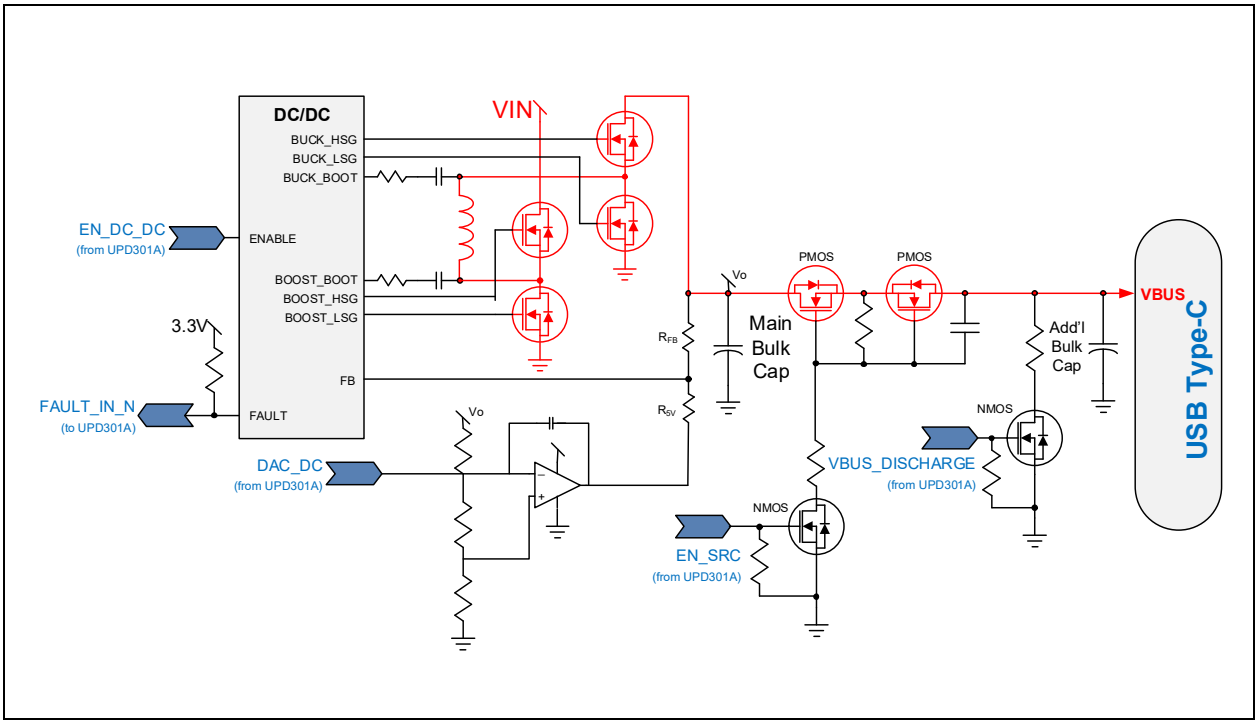


Figure 5-2 is an example of a digitally controlled buck/boost DC/DC converter with integrated switching FETs. These types of solutions are typically purpose-built for USB Type-C applications, so very little additional control beyond the DAC/ADC connection may be required. Figure 5-2 shows an example of a system where all voltage regulation, fault handling, and discharging are handled by a purpose-built IC.

FIGURE 5-2: PORT 1 INTEGRATED DAC CONTROLLED DC/DC WITH LOAD SWITCH

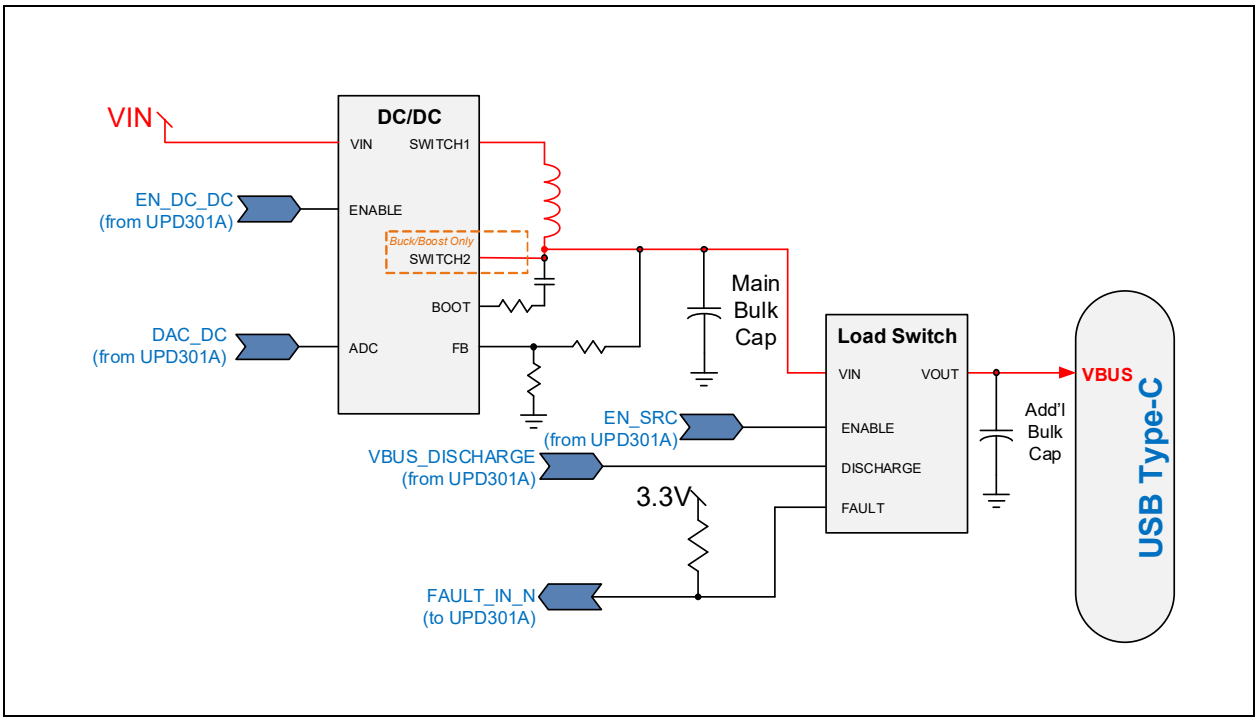


Figure 5-3 is another example of a traditional, all-analog Buck/Boost DC/DC. For port 2, it is controlled via GPIOs tying directly into the feedback loop of the DC/DC to control the voltage. This type of design also requires deep knowledge of power regulation circuitry in order to design a system that meets all of the compliance specification requirements.

FIGURE 5-3: PORT 2 ANALOG BUCK/BOOST DC/DC WITH DISCRETE FET SWITCHING USING GPIO CONTROL

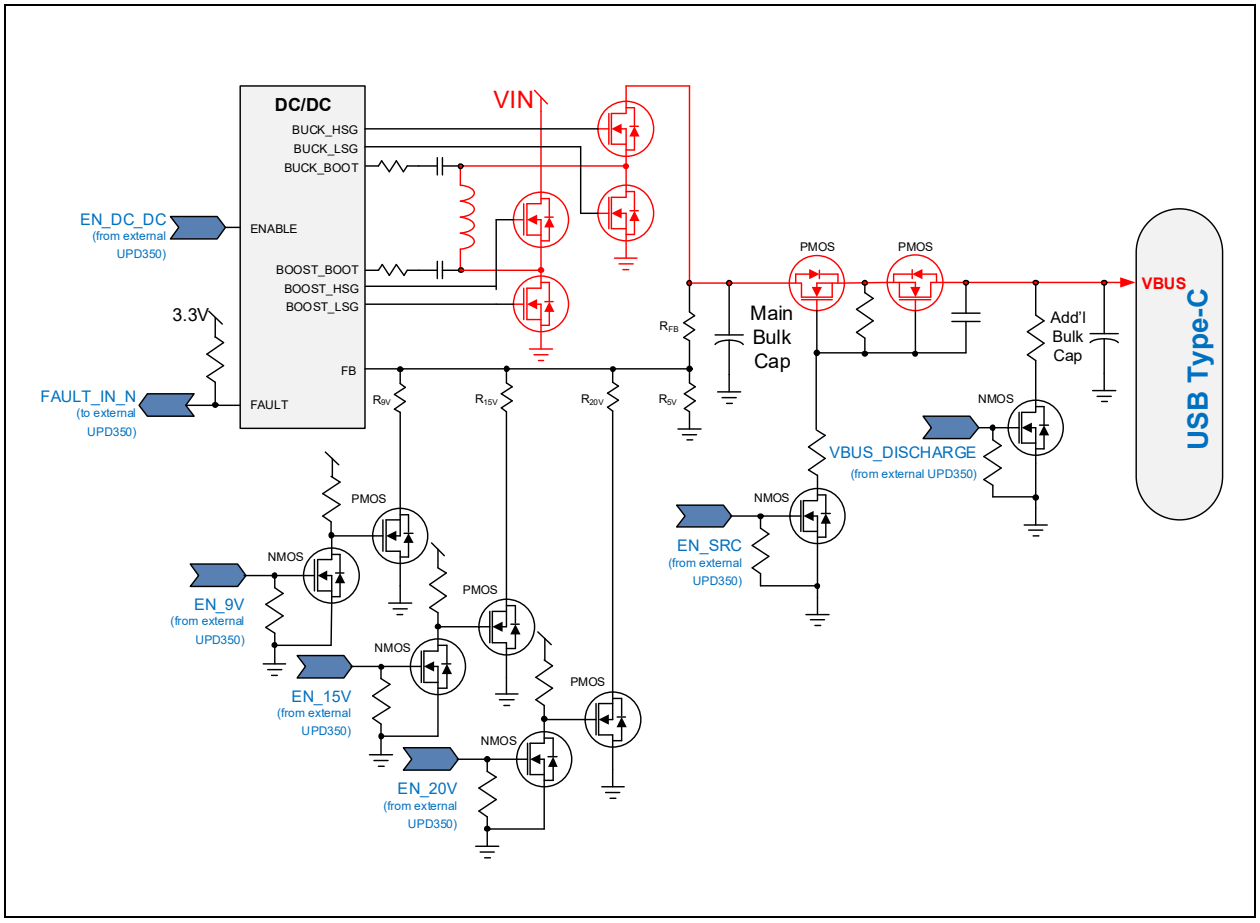
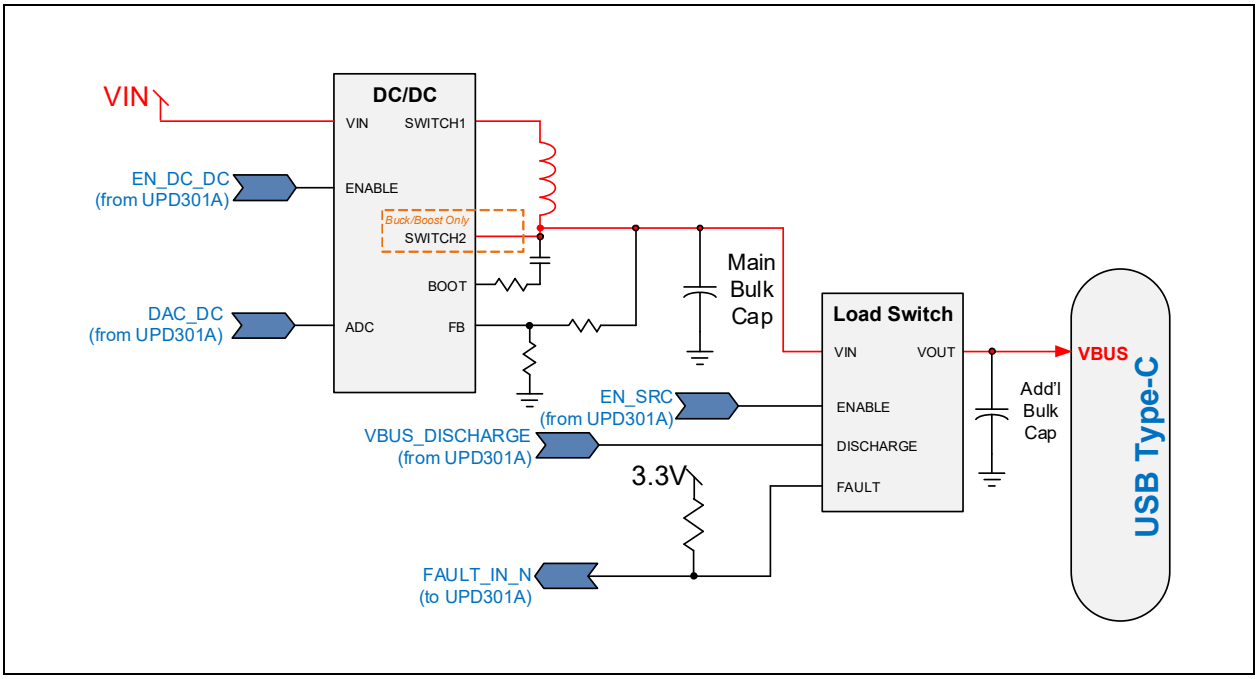


Figure 5-4 is another example of a digitally controlled buck/boost DC/DC converter with integrated switching FETs. Figure 5-4 illustrates an example of a system where all voltage regulation, fault handling, and discharging are handled by a purpose-built IC, and the DC/DC is controlled directly via GPIOs.

FIGURE 5-4: PORT 2 INTEGRATED GPIO CONTROLLED DC/DC WITH LOAD SWITCH



5.2 Voltage Regulation

The DC/DC must be able to supply steady voltages within a specified range for the set voltage. The required voltage range is changed slightly according to different conditions.

- ***vSafe5V***: Special voltage range defined for 5V regulation only. This is the nominal, static load voltage range requirement.
- ***vSrcNew***: Special voltage range defined for any voltage outside of 0V and 5V regulation. This is the nominal, static load voltage range requirement.
- ***vSrcPeak***: Special voltage range in peak current operation that is allowed when overload conditions occur.
- ***vSrcValid***: Additional range by which a source voltage is allowable during a transient load step. The VBUS voltage must always remain within this voltage window.

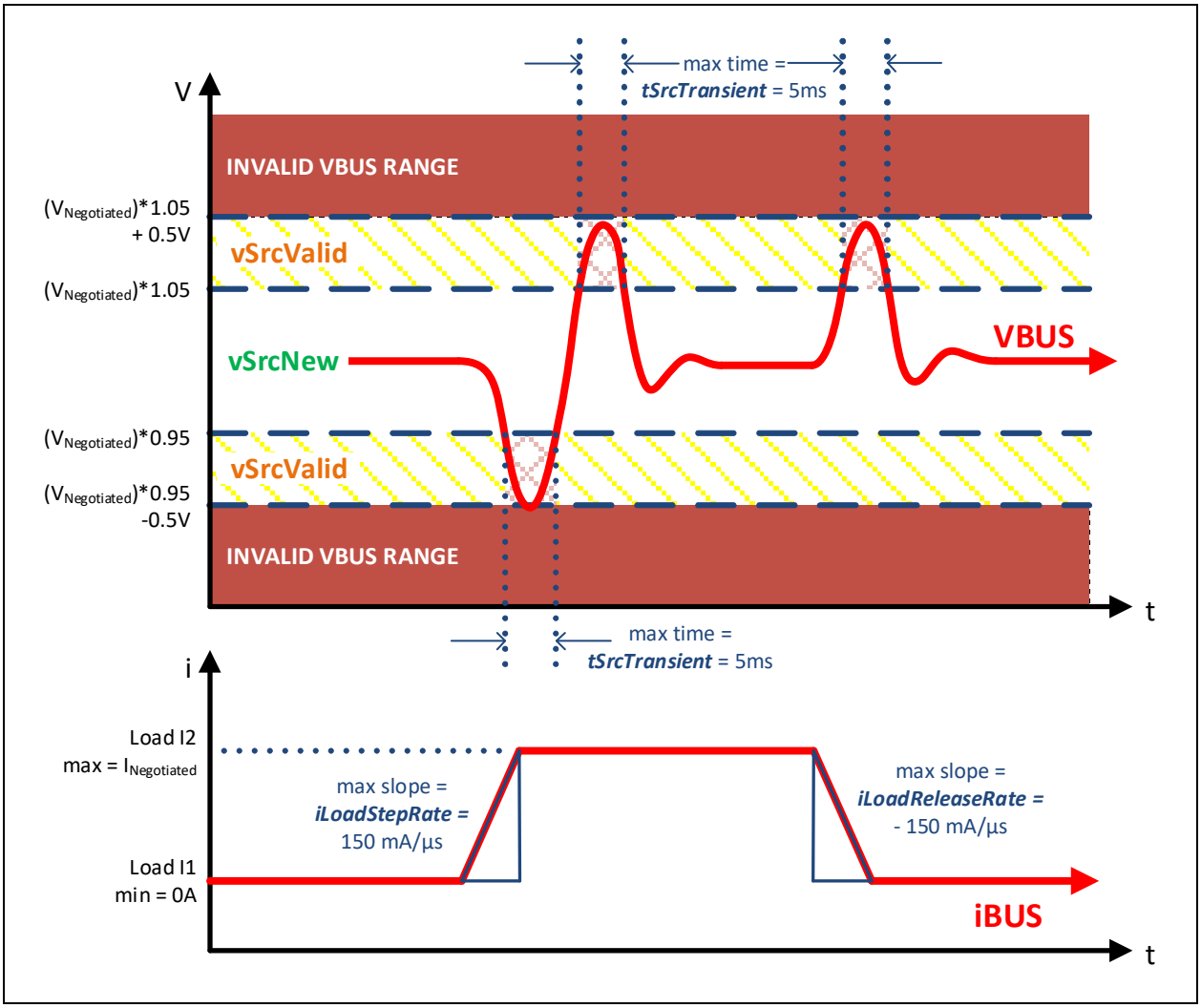
The actual voltages these specifications describe per *USB Power Delivery Specification Rev. 3.0, Version 1.2, June 21, 2018 and ECNs* are shown in Table 5-1.

TABLE 5-1: VBUS VOLTAGE REGULATOR REQUIREMENTS

Negotiated Voltage	Nominal Acceptable Range (at Source Connector)		Valid Range	
5V	Maximum	5.5V	Maximum	6.0V
	Minimum	4.75V	Minimum	4.25V
9V	Maximum	9.45V	Maximum	9.95V
	Minimum	8.55V	Minimum	8.05V
15V	Maximum	15.75V	Maximum	16.25V
	Minimum	14.25V	Minimum	13.75V
20V	Maximum	21.00V	Maximum	21.50V
	Minimum	19.00V	Minimum	18.50V

Upon attachment, load may step up or step down its load at a rate of ***iLoadStepRate*** or ***iLoadReleaseRate***, causing a very rapid load step from as little as 0A to as high as the maximum negotiated amperage or vice versa. The DC/DC regulator must be able to maintain voltage within the ***vSrcValid*** range even during load transients. The maximum amount of time that the source voltage max operates outside of the ***vSrcNew*** range (while still in ***vSrcValid*** range) is defined as ***tSrcTransient***.

FIGURE 5-5: STATIC VOLTAGE RANGES



5.3 Current Capability

The DC/DC must be capable of supplying a sustained load at the maximum current capability advertised through PD messaging.

It is recommended that some margin be included in the design. A general recommendation is to allow somewhere between 5% to 10% of additional current margin to allow for manufacturing variability and to ensure interoperability with devices that are operating near the edge of allowable operation.

It is also recommended that the selected DC/DC controller to have some amount of transient immunity to allow devices that very quickly enable a load when sinking power to operate without interruption.

5.4 VBUS Capacitance

The selected DC/DC regulator shall define its own output capacitance requirements, and the bulk capacitance and transient response of the DC/DC regulator must be sufficient to meet the drop/droop requirements of the PD specification.

The minimum VBUS capacitance for a PD source port is defined in the Type-C specification as ***cSrcBulk***, but this value is much lower than any DC/DC typically requires for stable operation.

5.4.1 5V TURN-ON TIMING

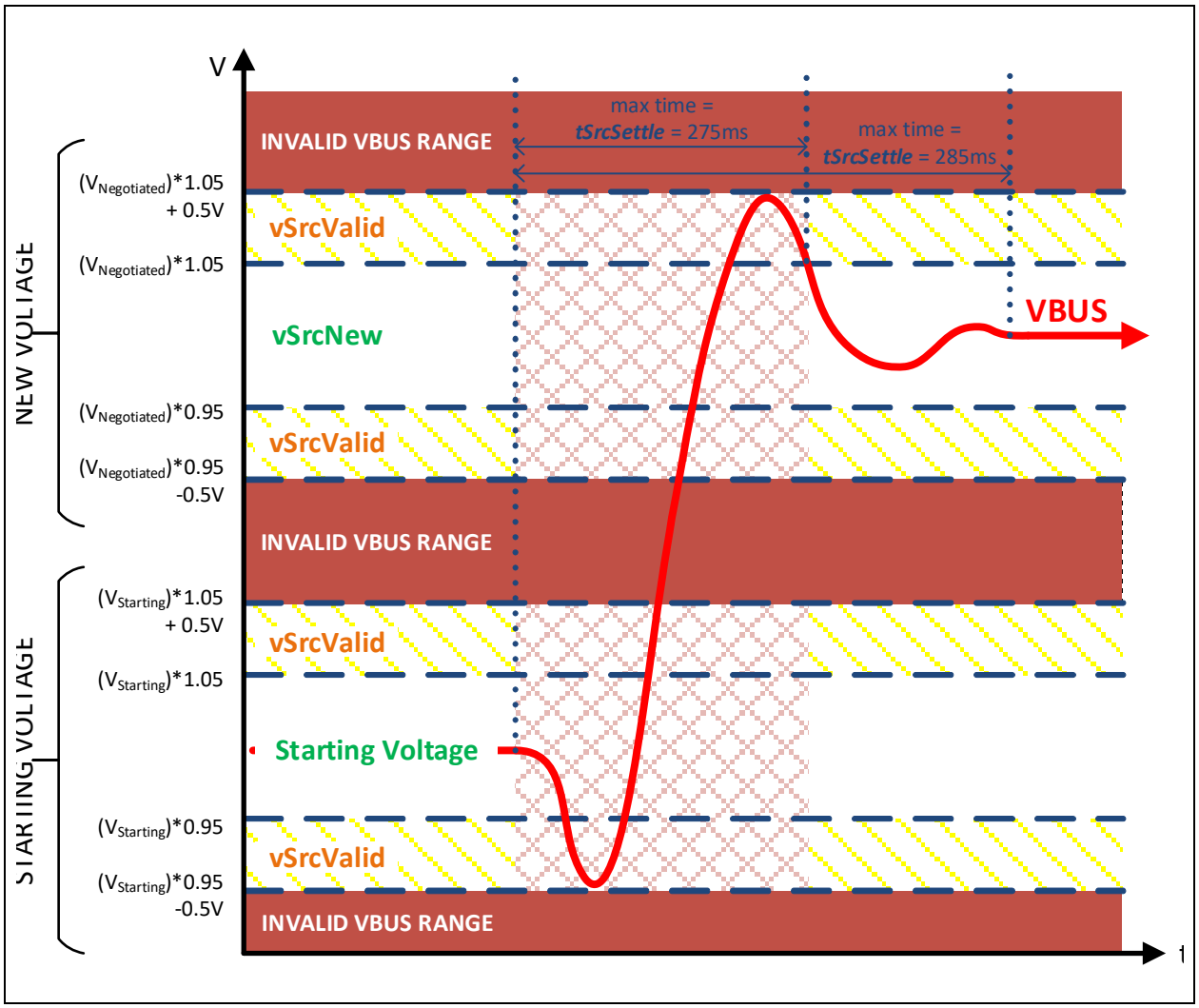
A USB Type-C connector is a 'cold socket', which means that the basic 5V VBUS voltage that every connection begins with is only applied after a valid Type-C attach is detected by the PD controller.

The DC/DC must be able to transition from the VBUS Off state (***vSafe0V***) to VBUS 5V state (***vSafe5V***) within ***tSafe5V***.

5.4.2 LOW-TO-HIGH VOLTAGE TRANSITIONS

When a new higher voltage is negotiated with a sink device, the DC/DC regulator must be able to monotonically transition to within the new voltages ***vSrcValid*** range within ***tSrcSettle***, without dipping below the original voltage's lower ***vSrcValid*** limit. By ***tSrcReady***, the voltage must be stable and within the ***vSrcNew*** voltage range.

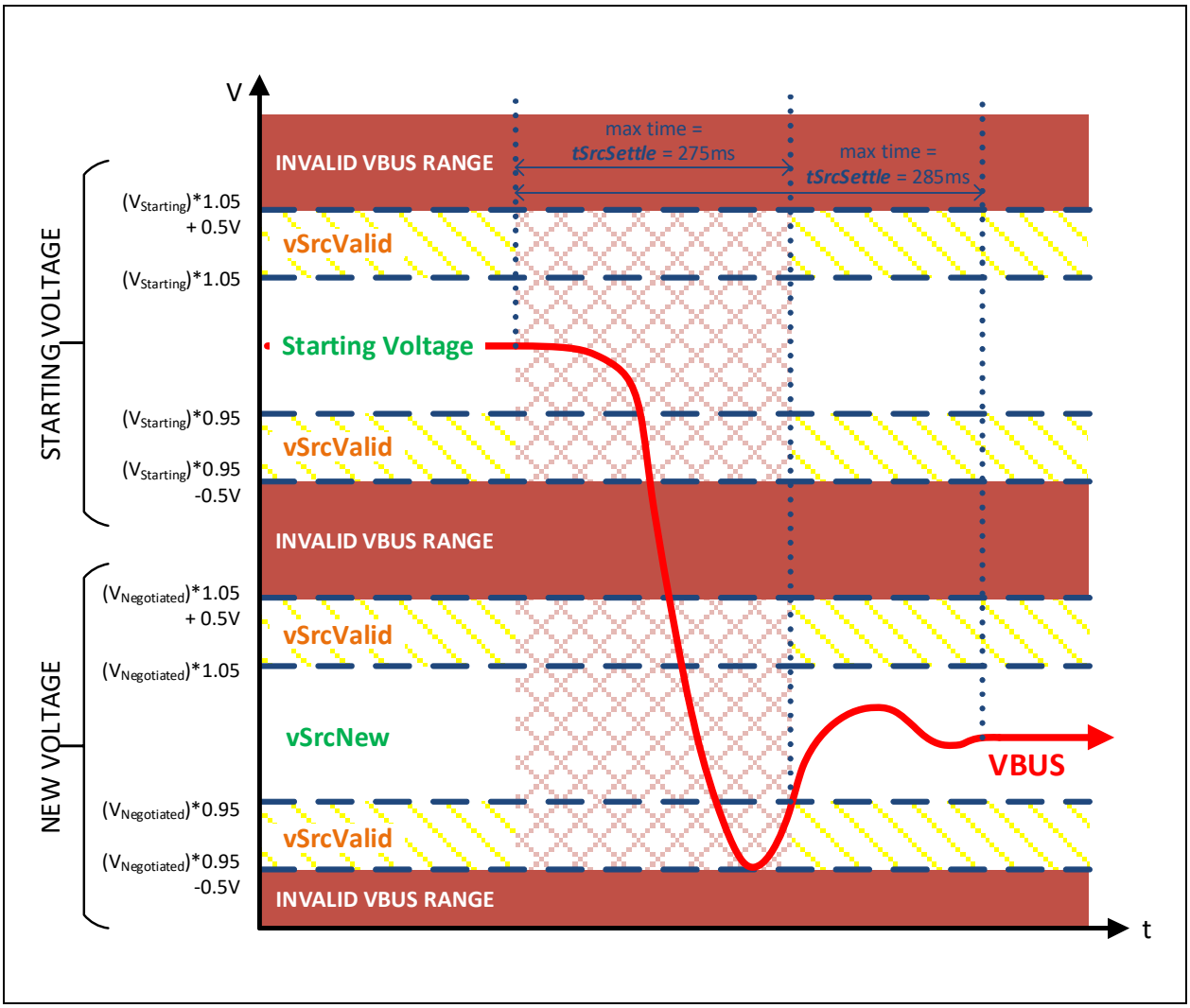
FIGURE 5-6: LOW-TO-HIGH VOLTAGE TRANSITIONS



5.4.3 HIGH-TO-LOW VOLTAGE TRANSITIONS

When a new lower voltage is negotiated with a sink device, the DC/DC regulator must be able to monotonically transition to within the new voltages ***vSrcValid*** range within ***tSrcSettle***. By ***tSrcReady***, the voltage must be stable and within the ***vSrcNew*** voltage range.

FIGURE 5-7: HIGH-TO-LOW VOLTAGE TRANSITIONS



5.4.4 OVERVOLTAGE AND UNDERVOLTAGE FAULT HANDLING

The UPD301A has a VBUS voltage monitoring pin (VBUS_DET) that verifies that the intended voltage is always supplied. The Power Delivery firmware automatically handles fault conditions in an overvoltage or undervoltage condition. By default, the UPD301A qualifies an overvoltage as +10% above the negotiated set voltage, and an undervoltage as -10% below the negotiated set voltage. These thresholds are adjustable in the firmware.

The DC/DC controller may optionally provide another layer of protection by monitoring for overvoltage and undervoltage conditions and signaling a fault condition to the UPD301A or external UPD350 through the FAULT_IN_N pin.

Note:	The VBUS_DET pin must always be connected, even if the DC/DC regulator is also handling overvoltage or undervoltage protection.

5.4.5 OVERCURRENT FAULT HANDLING

The DC/DC, load switch, or the combination of the two must be capable of protecting the source system from overcurrent scenarios. The point by which overcurrent protection initiates is not explicitly defined or tested. The USB compliance tests simply verify that overcurrent exists at some point above the advertised amount and that the protection circuitry adequately protects the power source from damage under hard short-to-ground conditions. The general recommendation is to set a static overcurrent threshold that initiates at the maximum advertised current level +10%.

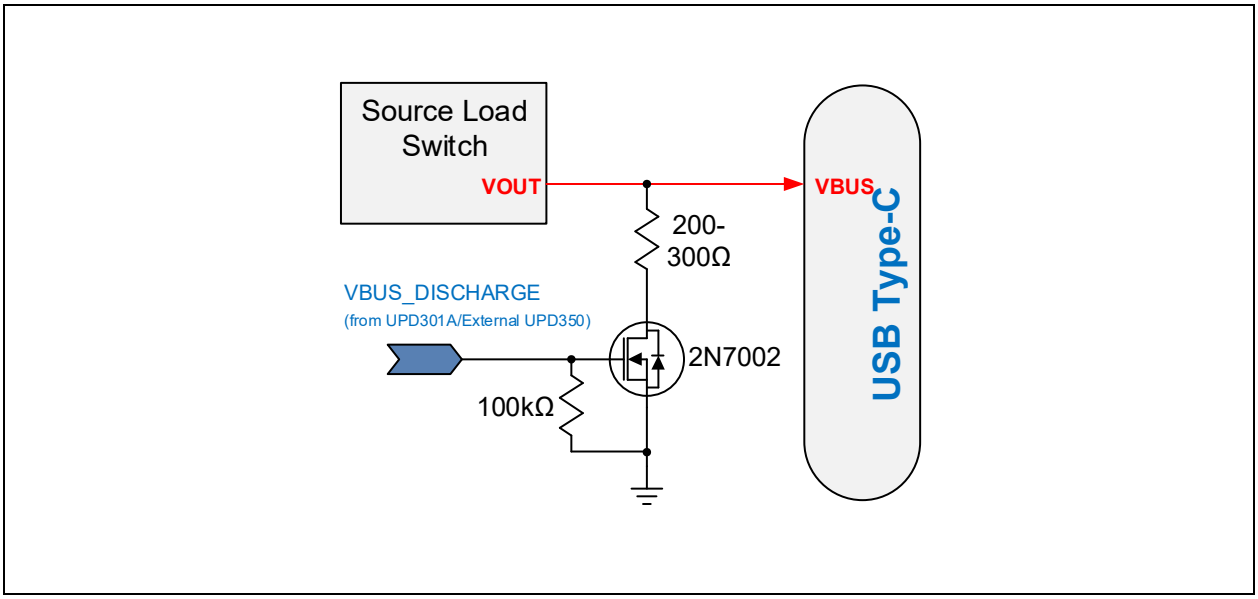
Note:	The current firmware implementation does not support variable overcurrent threshold adjustment based upon the actual negotiated contract, though such an implementation is possible and may be supported in a future firmware release.

5.4.6 VBUS DISCHARGE TO 0V

When transitioning from high voltage to low voltage or to no voltage, a discharge circuit is required to overcome the large bulk capacitance located on VBUS and ensure that the voltage transition is completed on time.

A recommended discrete circuit is shown in Figure 5-8:

FIGURE 5-8: DISCRETE VBUS DISCHARGE CIRCUIT



The system design may implement alternative solutions, such as a discharge circuit within an integrated load switch device or through a DC/DC controlled discharge FET, as long as the solution meets the requirements in Table 5-2.

TABLE 5-2: VBUS DISCHARGE CIRCUIT GENERAL REQUIREMENTS

Number	Requirement	Notes
1	The system or circuit can be controlled from an active-high GPIO of the UPD301A or external UPD350 device.	3.3V logic level with 8 mA drive strength
2	The system or circuit can handle the instantaneous current associated with the discharging of the full VBUS bulk capacitance charged up to the maximum supported VBUS voltage.	Assuming VBUS is charged to 20V, and there is a 300Ω discharge path, 66 mA of peak current (I = V/R) can be expected. Hence, a discharge FET that can handle 66 mA with margin should be selected.
3	The system can discharge VBUS from the maximum voltage to: • 5V (***vSafe5V***) with the time alloted (***tSafe5V)*** • 0V (***vSafe0V***) within the time allotted (***tSafe0V)***	Assuming general 5*R*C discharge rule of thumb, VBUS discharge time can be approximated. Keep in mind that the following resistance or capacitance should be added together to calculate the worse-case VBUS capacitive loading: • ***cSrcBulk:*** VBUS bulk capacitance of the source • ***cSnkBulkPd***: VBUS bulked capacitance for an attached sink device. • Cable resistance: The worst-case resistance for VBUS path of a Type-C cable assembly, including connectors and contact resistance, is: - 0.166Ω - 3A cable - 0.01Ω - 5A cable **Note:** Calculated assuming that the maximum IR drop is equal to 500 mV.

5.5 USB Specification Parameters

For ease of reference, the following USB specification parameters are copied within this document from the *USB Power Delivery Specification Rev. 3.0, Version 1.2, June 21, 2018 and ECNs* release package. It is recommended to cross reference these values with the latest Power Delivery specification, as they are subject to change with subsequent engineering change notices (ECNs).

TABLE 5-3: KEY USB SPECIFICATION PARAMETERS PER PD SPEC REV 3.0, VERSION 1.2

Parameter	Description	Value
cSrcBulk	Source bulk capacitance when a port is powered from a dedicated supply	Min: 10 µF
cSnkBulkPd	Bulk capacitance on VBUS a sink is allowed after a successful negotiation	Min: 1 µF Max: 100 µF
iLoadReleaseRate	Maximum load decrease rate	Max: -150 mA/µs
iLoadStepRate	Maximum load increase rate	Max: 150 mA/µs
tSafe5V	Time to reach ***vSafe5V*** max	Max: 275 ms
tSafe0V	Time to reach ***vSafe0V*** max	Max: 650 ms
tSrcReady	Time to when source is ready to provide power after newly voltage request is accepted by the source	Max: 285 ms
tSrcSettle	Time to when source voltage is within ***vSrcNew*** voltage range after the newly voltage request is accepted by the source	Max: 275 ms
tSrcTransient	Maximum amount of time the source voltage may be outside of ***vSafe5V*** or ***vSrcNew*** during a transient event. The voltage may never be outside of ***vSrcValid*** during this time.	Max: 5 ms
vSafe5V	Safe operating voltage at 5V	Min: 4.75V Max: 5.5V
vSafe0V	Safe operating voltage at “zero volts”	Max: 0.8V
vSrcNew	Allowable voltage range for VBUS under normal static load conditions	Max: Negotiated voltage*1.05 Min: Negotiated voltage*0.95
vSrcPeak	Allowable voltage range for VBUS under peak current conditions	Max: Negotiated voltage*1.05 Min: Negotiated voltage*0.90
vSrcValid	Absolute maximum or minimum range for VBUS voltage under transient load conditions	Max: vSrcNew max voltage + 0.5 Min: vSrcNew min voltage – 0.5
vSrcSlewNeg	Maximum source voltage slew rate during a VBUS high-to-low transition	Max: -30 mV/µs
vSrcSlewPos	Maximum source voltage slew rate during a VBUS high-to-low transition	Max: 30 mV/µs

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003265A (03-31-20)	Initial release	

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