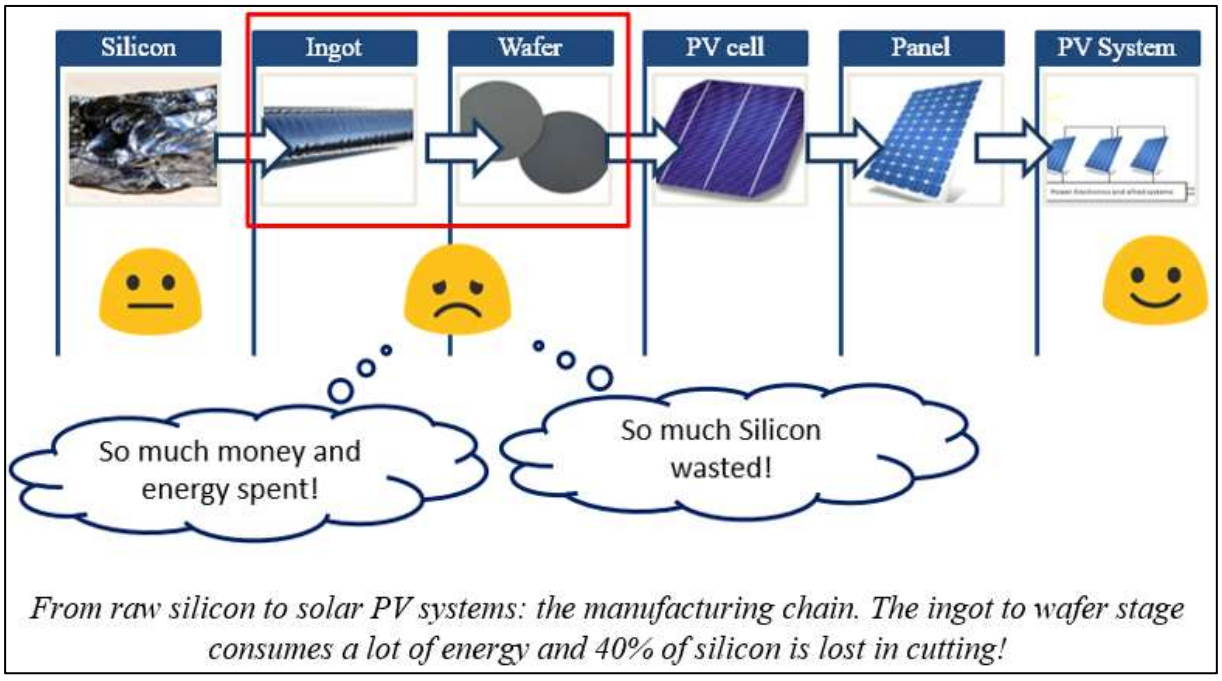
Making low-cost solar panels

If solar energy is free, why we do not just install solar panels everywhere? How can we reduce cost of *making* Photo-Voltaic (PV) systems (i.e. the systems which convert solar energy into electricity)? Is it possible to spend less money and less energy for fabrication of the PV systems? We are searching ways so that PV systems will cost much lesser than it is today and they can be made in India as well.

Let's see some numbers first. Presently, a lot of energy is spent in making even a small unit of a PV system. Suppose we want to manufacture a PV system that will generate 1 unit of energy, then how long should it operate before we recover the cost associated with that 1 unit of energy – right now, it is 2 to 3 years! This period is called ***payback period***. About 90% of the world's PV systems are made from silicon-solar-cells. But do you know that, in manufacturing one solar cell, a huge portion (40%) of silicon is wasted in manufacturing itself! Thus, to make solar energy more feasible, we need to find ways so that we can manufacture PV systems by spending lesser energy and by saving silicon which is wasted in the process. With this view, we, at IIT Bombay, started looking at the problem few years ago.



From raw silicon to solar PV systems: the manufacturing chain. The ingot to wafer stage consumes a lot of energy and 40% of silicon is lost in cutting!

To see how exactly we did it, first, we have to understand how the PV systems are manufactured. The first step is to extract silicon from ores. Big cylinders (roughly 20 cm in diameter), called as the *ingots*, are formed from this raw silicon. The ingots are sliced into 180 microns thick wafers. This is approximately equal to the thickness of just 2 human-hairs! *Note*

that, the thinner the wafers; the more will be the efficiency of the solar cell. The actual solar cells are formed from the wafers after some complex chemical and electrical processes. Several such cells are connected together to form solar panels. Put some allied electronics around it, and then our PV system is ready to use! The figure above shows the chain of manufacturing the PV system from raw silicon.

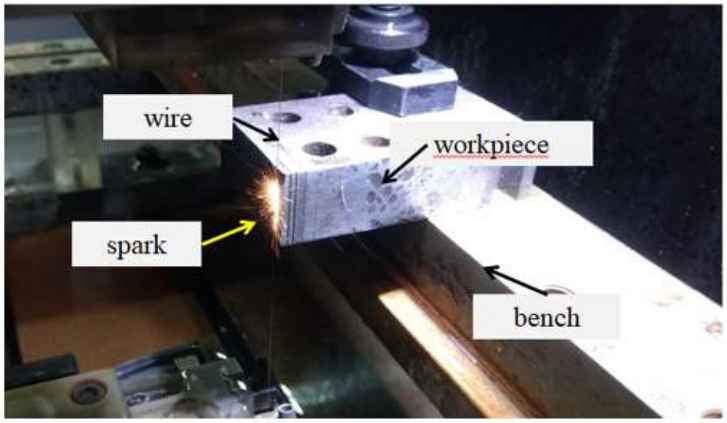
Our efforts are aimed at the ingot-to-wafer stage. This stage consumes 37% of total energy required in the manufacturing chain. Conventionally, *abrasive*- wire-cutting is used to cut wafers from ingots. In this method, a metal wire acts as a cutting tool. The word ***abrasive*** means the wire rubs against silicon ingot to cut it – just like we use a saw to cut wooden planks, or a knife to slice a bread-loaf! Now, these methods are lossy – suppose we slice 1 meter long ingot, 40 cm of it is lost while cutting itself! These are called as ***kerf losses***.

Prof S S Joshi along with Dr Dongre, Kamlesh Joshi and others, from Department of Mechanical Engineering, IIT Bombay, have already shown that, if we use Wire Electric Discharge Machining (**WEDM**) to cut the wafers, the **kerf losses can be reduced** from **40%** to **15%**. Plus, wafers thinner than the present wafers (~**120 microns**) can be cut, which means that we can achieve a **significant improvement in the efficiency** of the solar cells.

So all said and done, what is now stopping us from implementing this technology on a large scale? Well, there are two problems: (a) the established abrasive cutting methods can produce thousands of wafers per day, whereas the production rate of WEDM is much less (b) although the existing WEDM can cut wafers from silicon ingots, it does not do it *optimally*. That is because, it is *designed* for cutting metals and silicon is a semiconductor (which means that its electrical properties are different from those of metals). For example, the electrical conductivity of metals is 10,000 times that of silicon. Therefore, to compete with the established practices, we need to adapt the existing WEDM technology for cutting semiconductors. Our team (I along with my advisors, Prof S V Kulkarni and Prof H J Bahirat) is doing research in the ***adaption of WEDM for silicon***.

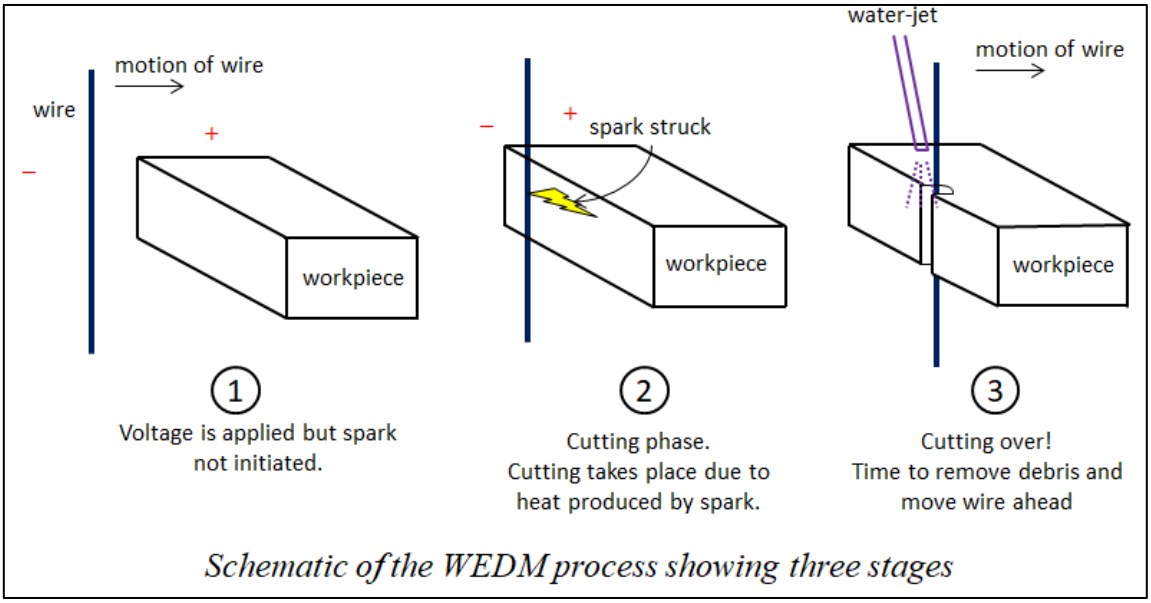
First, let's see what WEDM is. The meaning is hidden in the name itself: here, the *machining* (cutting) takes place due to an *electric discharge* or spark, which is struck between the *wire* and the workpiece! An electric supply is connected across them, with the wire connected to the negative terminal and ingot (workpiece) connected to the positive terminal. Water is continuously flushed in the gap between the two. The wire is brought very close (10-100 microns) to the ingot and a supply voltage is then turned ON. If the voltage exceeds

certain vale, known as the breakdown voltage, a *spark* is struck (See the photo below). The temperature of the spark is around 10,000 ^{o}C. This is more than the temperature at the surface of the Sun!



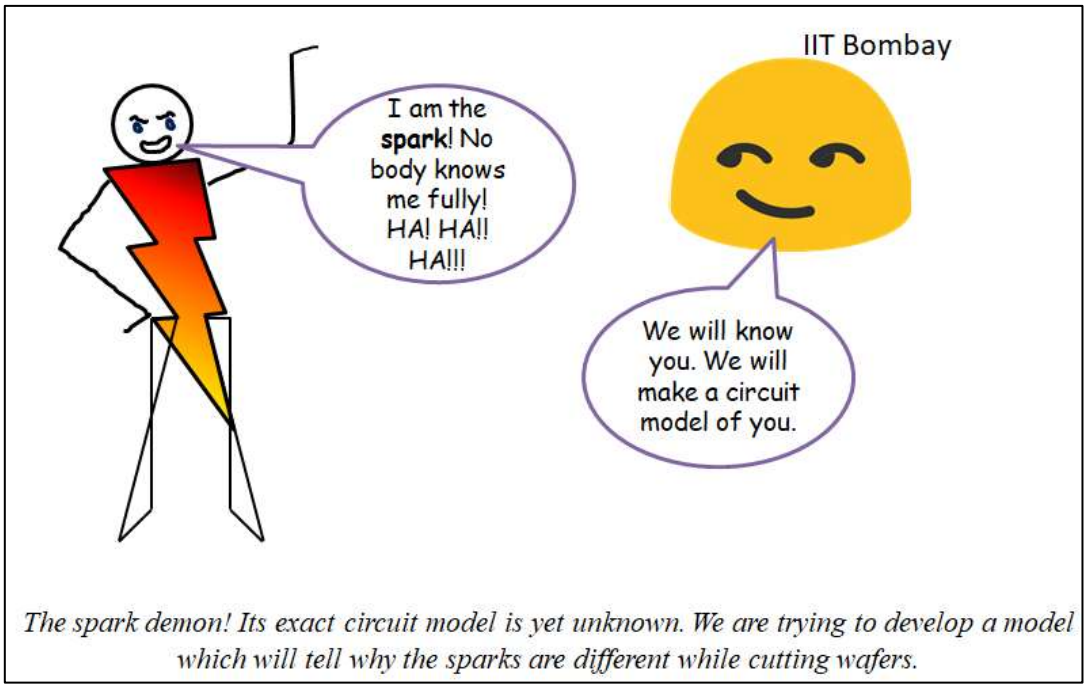
WEDM: photo of actual setup: The wire just as thick as a hair! Also the gap between the wire and workpiece is also equal to a hair. Hence, it cannot be seen here!

The region of the ingot around the wire then melts. Note that, the wire never actually touches the workpiece, which means that this is a *non-contact* process! After a short duration, the voltage is turned OFF. If we do not turn it OFF, there will be a short circuit. This OFF time serves two other purposes: (a) debris of the cut material are flushed away by water, (b) the wire is moved closer to the ingot to make it ready for the next cutting cycle. The cycle is completed within a very small fraction of a second (typically in 100–200 microseconds). Following image illustrates the three stages.



Schematic of the WEDM process showing three stages

To verify its feasibility in fabricating silicon wafers, we first did several experiments of cutting silicon and steel pieces of the same dimensions. Spark-voltages and spark-currents were recorded while cutting. It was observed that, the sparks are *different* for the two materials. The exact nature of these sparks is not known till date. Then, we tried to characterize the difference by means of developing an accurate ***circuit model***. The model will help us explain the behaviour of silicon in WEDM and how it is distinct from those of the metals. Besides, it can also take us to a step ahead in understanding the sparks in general, e.g. in case of lightning or short circuits. Our circuit model is *novel* because it is an elaborate and a complex (non-linear) model. This model will be useful for (a) design of a customized WEDM (b) understanding of sparks between the metal wire and semiconductor piece and (c) modelling sparks in other processes.

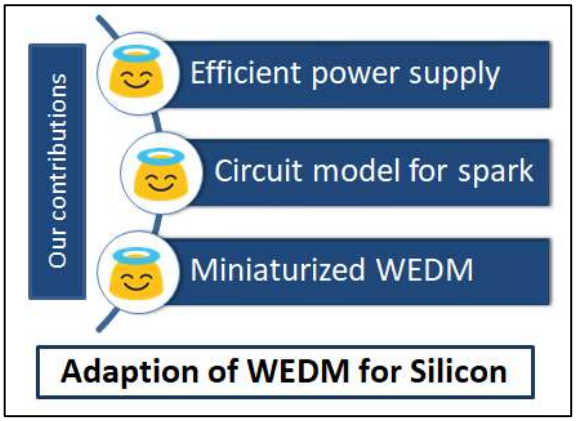


The spark demon! Its exact circuit model is yet unknown. We are trying to develop a model which will tell why the sparks are different while cutting wafers.

For cutting silicon wafers, we also need to modify the power supply, which provides voltage across the wire and the ingot. A special kind of **power-electronics**-based supply, known as *pulsed voltage* supply is necessary for WEDM. The name itself tells that, it is not the same as the conventional AC or DC power supplies. The word *pulsed* comes from the fact that it should be turned ON-OFF continuously (as explained before), 5000-8000 times per second! Till date, no much attention was given on improving the efficiency of the pulsed power supplies. We are trying to improve the **efficiency** from **40%** to **80%**. This will yield enormous power savings and hence, further reduce the *payback period* that is mentioned in

the very beginning. Further, our ***indigenous design*** would help to have full control over voltage, current, ON time and OFF time.

Ultimately, with better understanding of sparks and better power supply, we are planning to fabricate a customized WEDM for silicon. To begin with, we have designed a **fully indigenous WEDM that can fit on a table**. We did it by getting rid of some features, which are not required for wafer cutting.



In short, our research is a ***stepping stone towards the low-cost solar cells***. We save the silicon lost in manufacturing the wafers from ingots. In particular, we have reduced the silicon ***losses from* 40% *to* 15%**. We have also saved a significant amount of energy in the cutting process by ***improving the efficiency*** of the power supply (from **40% *to* 80%**). Our research is also targeted to develop an accurate circuit model for sparks between metals and semiconductors. This model can in general be used to simulate sparks in water and fluid environments.

Declaration: This article is original and has not been previously published elsewhere.

−Makarand M Kane

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