

Comprehensive Investigations into Electrical Characterization, Converter Topologies, and Electromagnetic Forces in Wire EDM for Semiconductors

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by

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*Dedicated to Late Nana Ajoba and Late Manda Aji,
who had the utmost respect for education*

Thesis Approval

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Abstract

Semiconductor wafer-fabrication is a multi-billion-dollar industry. There are mainly two applications of semiconductor wafers: (a) for manufacturing photovoltaic cells that convert solar energy to electricity and (b) for manufacturing integrated circuits (ICs) in electronics industry. Presently, the wafers are sliced from semiconductor ingots by using wire-sawing, which is an abrasive cutting technique. However, this method results in 40% kerf losses. Also, wire-sawing of hard materials like silicon carbide might result in cracks on wafers. The surface quality of cut wafers is poor due to uneven heat produced by abrasion of wires. Wire Electric Discharge Machining (WEDM) is an efficient alternative for slicing ingots as the kerf loss is around 15% only. Further, WEDM is an electro-thermal, non-contact cutting process, in which the machinability of any material is independent of its hardness. Hence, it is effective for hard materials like silicon carbide as well. The problem of surface contaminations is also not severe with WEDM. However, there are several challenges in implementation of WEDM by the semiconductor industry.

Efforts to find an optimum set of process parameters for semiconductors with available WEDM are limited because the parameters cannot be varied beyond the limits set by the machine manufacturers. Hence, there is a need to develop a WEDM where all the parameters can be varied in the desired range. The WEDM process is not completely understood for metals and the process is further complicated when the workpiece is semiconductor because the physics of the process is different from that when the work-piece is metallic. Hence, there is a requirement of exploring the physics of the process for semiconductors.

The available literature deals with the topic of EDM pulse generators (EPGs) mainly from the production engineering perspective and not from the power electronics perspective. Also, if the WEDM has to replace the conventional wafer manufacturing methods, the efficiency of the pulse generators is important. This topic is not addressed in literature till date. Apart from these, probably one of the most crucial issue is unavailability of multi-wire EDM (MWEDM) on commercial scale, which can compete with high throughput of the multi-wire saw. In this research, an attempt is made to solve the above issues, so that WEDM is industry-ready for semiconductor slicing applications.

Experimental investigations are done with p-doped silicon, to understand its behaviour with WEDM. Specifically, spark erosion of a silicon-workpiece is compared with that of a steel workpiece of the same dimensions. Taguchi design of experiments is used with L18 orthogonal array, to study the process systematically. The analysis is based on spark voltage-current (V-I) characteristics. This approach is different from the previously reported research, which is mainly focused on mechanical performance parameters.

A detailed classification and comparative study of 13 important EPG topologies is done from power electronics perspective, considering the structure, control, efficiency, component count and voltage stresses. One of the topologies from the comparative study is

chosen for hardware implementation. For that topology, the design and modeling issues are addressed. An efficiency improvement scheme is proposed for the topology which improves the efficiency by $\approx 30\%$.

A customizable miniature WEDM is developed that fits on a table-top and occupies a space of $120 \times 120 \times 60$ cm. The control system for the same is implemented on TMS320F28069 controller from Texas instruments. The machine can be used to determine the optimum set of parameters for semiconductors and to study the physics of the WEDM process for metals/semiconductors by closely probing the spark, which is not possible with commercial machines.

Analysis of the forces of electrical origin on wire is done for the case of semiconductor workpiece using Finite Element Method (FEM). These forces cause wire-vibrations affecting the flatness of the cut wafers. It is proved that, in the case of semiconductors workpiece, electrostatic forces are stronger than electromagnetic forces.

The developments till date in the domain of MWEDM are mostly limited to the mechanical design of the machine. In this work, the wire-wire forces existing in MWEDM are explored for the first time. Computation of forces is done using both: closed form analytical expression as well as FEM simulations. Based on the force computations, novel electrical supply schemes are proposed for MWEDM which can reduce the required tension to 20-40% of the that needed using the conventional schemes. This can avoid the wire-breakage and consequent problems of process hindrance. Novel pulse generator topologies required for the schemes are also proposed.

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Abbreviations

EDM	Electrical Discharge Machining
DEDM	Die-sinking Electric Discharge Machining
WEDM	Wire Electric Discharge Machining
MWEDM	Multi-Wire Electric Discharge Machining
EPG	EDM Pulse Generator
PCRS	Pulsed Current Reference Scheme
CCRS	Constant Current Reference Scheme
FEM	Finite Element Method
FEA	Finite Element Analysis
SEM	Scanning Electron Microscopy
EDX	Energy-dispersive X-ray Spectroscopy
ICPAES	Inductively Coupled Plasma Atomic Emission Spectroscopy
SSTF	Small Signal Transfer Function
CCRS	Constant Current Reference Scheme
PCRS	Pulsed Current Reference Scheme
CS	Current Source
VS	Voltage Source
ANOVA	Analysis Of Variance
AVG	Average
STD	Standard
PM	Phase Margin

Chapter 1

Introduction

This chapter gives a background of the research problems addressed in this thesis. Basics of WEDM are discussed in brief and its comparison with the conventional semiconductor-ingot-slicing technique is given with pros and cons of both methods. The chapter also presents the challenges coming in the way of acceptance of WEDM by semiconductor industry. In other words, these challenges are the lacunae in the research domain, which gives rise to the motivation of the present work. In the end, the scope of the work is also described.

Semiconductor wafers are thin (≈ 100 to $300\ \mu\text{m}$) slices used in solar and microelectronic industries, both of which have turnover of multi-billion dollars [1, 2]. In the case of solar industry, the photovoltaic (PV) cells are made up of semiconductor wafers. In the microelectronics industry, the wafers constitute a substrate (base) on which the integrated circuit blocks are developed or fabricated. Although alternatives of silicon like germanium, silicon carbide (SiC), CdTe, etc. are also popular, the most commonly used semiconductor is silicon: about 95% share in the PV industry [1]. Therefore, only silicon is considered in this work.

In order to understand the big picture, the place of “slicing of ingots” stage is indicated in Fig. 1.1 with respect to the complete solar cell/integrated circuit (IC) manufacturing chain [2, 3]. Raw silicon is mixed with dopant and heated at about 1420°C , i.e. above the melting point of silicon. Then a single crystal of silicon is positioned at the top of the liquified silicon in a crucible. The seed crystal and crucible are rotating in opposite directions to maintain uniformity in the ingot production. The seed is then slowly lifted

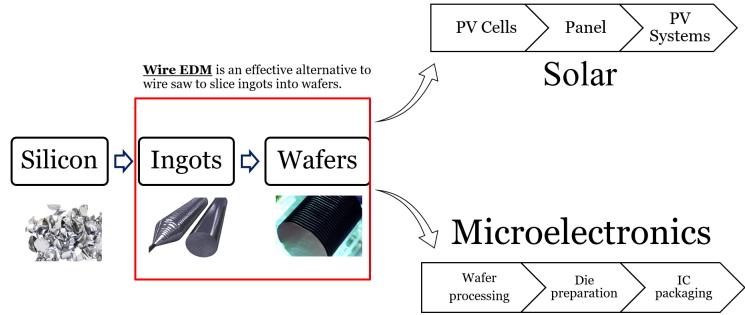


FIG. 1.1: Wafer manufacturing chain (inset-image source: [7–9])

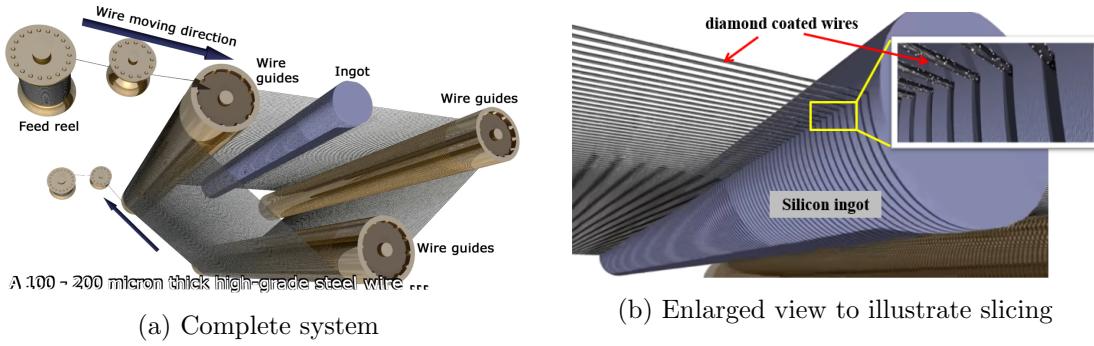


FIG. 1.2: Slicing semiconductor ingot with multi-wire saw (source: [10])

out of the molten pool to form the silicon ingot [3], which is nothing but a cylinder of silicon whose height is significantly larger than its diameter. This is called Czochralski process. In 1970s the ingot diameter used to be around 100 mm, however, the present day diameters of ingots range from 300 mm to 450 mm [2, 4].

The ingots are then sliced by using wire-saw which consists of multiple wires to cut through the ingots as shown in Fig. 1.2(a). Commonly used abrasives are SiC slurry or diamond particles [5]. The abrasives can be suspended in a slurry or the wires can be coated with diamond grits as shown in Fig. 1.2(b). The slicing produces several hundred of wafers in one go and several thousand wafers per day [5, 6]. The wafer surface is not as flat as required for fabrication of solar cells or semiconductor devices. The wafers undergo lapping, cleaning and polishing before they are sent for device or solar cell fabrication.

1.1 Wire EDM vs Wire-saw for Wafer Manufacturing

It is instructive to compare the present process i.e. wire-saw vis-à-vis WEDM with respect to slicing semiconductor ingots. Earlier research at IIT Bombay and elsewhere has already proved the following advantages of WEDM over the conventional wire-sawing techniques. They are summarized in Table 1.1 also.

1. Being an abrasive process, the wire saw can cause micro-fractures and cracks as deep as $20 \mu\text{m}$ into the surface of the wafers they produce. This leads to fragile wafers whose minimum thickness is limited to $\approx 180 \mu\text{m}$ [11]. Therefore, as mentioned above, further processing is required to make the wafers smoother. The surface finish of wafers obtained by the WEDM is better, as it is a non-contact process [12].
2. The kerf loss i.e. the material lost while cutting as shown in Fig. 1.3, is 40% in the conventional wire-sawing techniques. The loss can be reduced to 15% with WEDM [13]. Ultimately, this would reduce the overall cost of solar cells and semiconductor devices.
3. The abrasive process results in heat produced due to friction. It is reported that [14], the temperature of the wire at the exit point on the ingot would be higher than that at the entry point in wire-sawing. This phenomenon can cause tapered cut in the wire saw [14]. The problem of tapered cut due to unequal heating of wire is not present in the WEDM.
4. Silicon carbide is a wide-bandgap semiconductor material increasingly being used by electronics industry, especially for making high frequency power electronic switches. SiC has high hardness similar to that of diamond [15] therefore the cost of slicing SiC ingots with abrasive techniques is very high. The surface damage caused by abrasive methods is also high, particularly for large-diameter ingots [15, 16]. The machinability of a material with WEDM does not depend upon its hardness [17]. Therefore, the above problems with cutting SiC ingots do not arise if WEDM is used in place of conventional techniques.
5. There might exist a problem of contamination of the wafers due to the slurry which is used as abrasive material in wire-sawing [6].

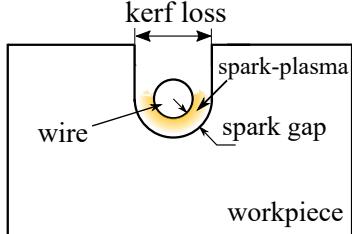


FIG. 1.3: Kerf loss in WEDM

TABLE 1.1: Comparison of Wire EDM vs Conventional Methods [13, 20]

	Parameter	Wire EDM	Conventional methods
	Principle	Erosion by spark plasma, Non contact cutting	Abrasive cutting, diamond particles, slurry used as abrasive
Advantages	Minimum wafer thickness	120 μm	180 μm
	Kerf loss (%)	15-20	35-40
	Thickness to polish (μm)	15-26	25-35
	Surface roughness $R_a \mu\text{m}$	1-3	2-5
Challenges	Physics of the process	Not yet fully understood	Some understanding is developed [21]
	Investigation of optimum set of process parameters	Efforts limited by commercially available WEDMs	Industrially established process
	Throughput	Multi-wire EDM developed only on prototype level. Single wire EDM cannot match the output of multi-wire saw.	Multi-wire saw is commercially available. It can produce thousands of wafers per day.
	Forces affecting surface roughness	Existence of electrical forces. Very few research articles present.	Only mechanical forces exist. Analysis of forces is done [21].

6. It is proved that ultra-thin wafers of width $\approx 100\text{-}130 \mu\text{m}$ can be cut easily with WEDM [18, 19].

The above points are summarized as advantages in Table 1.1. However, WEDM also faces challenges for acceptance by the wafer manufacturing industry as enumerated in Table 1.1. They will be elaborated in Section 1.3. In order to appreciate the challenges, it is important to understand basics of the WEDM process and the WEDM system, as elucidated in next section.

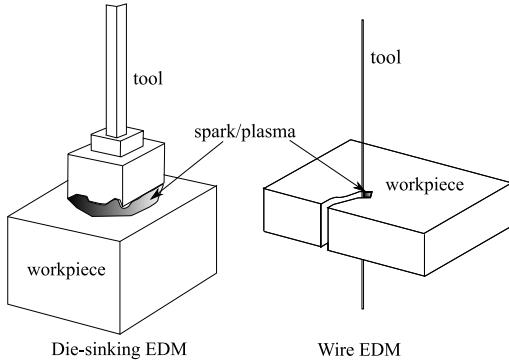


FIG. 1.4: Die-sinking EDM vs Wire EDM

1.2 Basics of WEDM: Process and System

WEDM is an electro-thermal non-contact machining process. The first effective use of electrical discharge for machining was invented by B. R. Lazarenko and N. I. Lazerenko in Moscow in 1943 [17, 22]. However, it was die-sinking EDM (DEDM), where the tool is a 3D die which sparks repeatedly over the workpiece surface and the die-shape is printed on the workpiece as shown in Fig. 1.4. In WEDM, the tool is a wire which traces a path defined in CAD and guided by CNC to cut desired shape in the workpiece as shown in Fig. 1.4. The first WEDM machines were made in late 1960s. Since that time, the WEDM has undergone many improvements due to advancement in CNC, power electronics and modern process-control techniques. It is widely used in many industries like electronics, automation, watches, surgical equipment, aerospace, biomedical, etc.

1.2.1 Principle

In WEDM, the material erosion takes place due to heat generated by sparks between the tool electrode (wire) and the workpiece electrode. The gap between the two electrodes is of the order of 10-100 μm [22, 23]. The electrodes are either submerged in dielectric fluid (like oil, deionised water, etc.) or the fluid is continuously flushed onto the gap.

1.2.2 Stages of operation

There are three stages of operation in WEDM as shown schematically in Fig. 1.5, where WP is the workpiece. The corresponding voltage and current waveforms are shown in Fig. 1.6. The stages are described below:

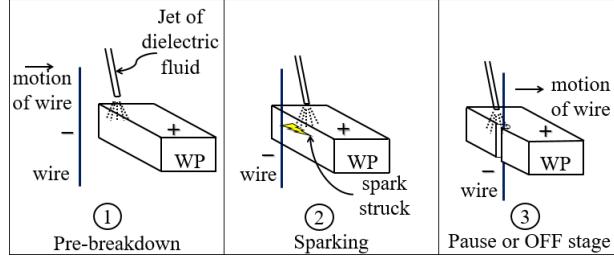


FIG. 1.5: Stages of WEDM process

1. **Pre-breakdown:** This stage represents the time delay between application of voltage V_{ref} and breakdown of the gap and hence it is also referred to as ignition delay time [17, 24]. V_{ref} has to be greater than V_b , which is the gap breakdown voltage. The delay is stochastic in nature [22] and usually ranges from few tens to hundreds of ns [25].
2. **Sparking:** This stage begins when the gap breaks down and a finite current starts to flow. The voltage across the gap is reduced to V_{spark} : the spark voltage. Both V_b and V_{spark} are governed by physical conditions, i.e. material of the tool and the workpiece, temperature of the dielectric fluid and plasma, material of the dielectric fluid, area of the electrodes, etc. [24, 26, 27]. Therefore, during this stage, the voltage v_o cannot be controlled however, the spark current is controlled. Higher the magnitude of the current, higher will be the material removal rate (MRR) [23].
3. **Pause:** This stage is necessary to avoid development of spark into a sustained arc and eventual short circuit. Hence, no voltage is applied across the load and the spark is allowed to implode [24]. This stage spans time from instant t_2 to the instant t_3 as shown in Fig. 1.6. During the transition from the sparking stage to the pause stage two processes occur: (a) recombination of electrons and ions and (b) implosion of spark plasma. The implosion actually helps the ejection of solidified debris particles from the workpiece and hence completes the material removal process. These two processes help the gap to regain its dielectric strength [17].

As shown in Fig. 1.6, the complete time period is T_m : machining time and the corresponding frequency is f_m and the ratio of ON time to T_m is called machining duty D_m . Note that $t_{\text{ON}} = D_m T_m = (d_1 + d_2) T_m$ and $t_{\text{OFF}} = d_3 T_m$.

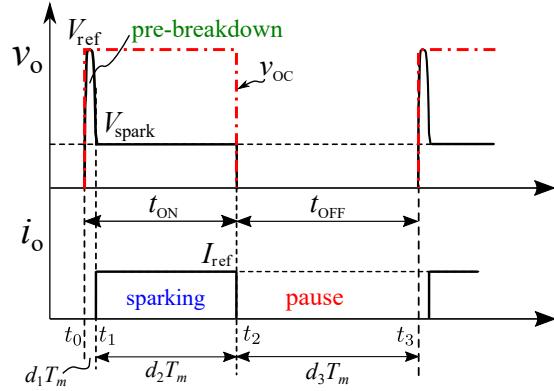


FIG. 1.6: WEDM load: voltage and current waveforms

1.2.3 Structure of WEDM system

The complete WEDM system consists of four subsystems as follows:

1. EDM pulse generator
2. Wire feed subsystem
3. Dielectric circulation system
4. CNC system

A schematic of the complete WEDM system is shown in the form of block diagram in Fig. 1.7. The pulse generator applies pulses across the gap. When the gap breaks down, a spark/plasma is formed. This causes localized heating and melting of the workpiece, and the subsequent material removal causes an increase in the gap length. CNC motion control advances the tool electrode depending on decrease in the gap voltage so that the sparking is initiated again. Then the successive pulses would cause the material erosion further. The required CAD path is fed apriori into the CNC control system, which imparts the motion along the path to the workpiece electrode. As WEDM is primarily used for precision cutting, the diameter of the wire is very less of the order of $\approx 50 - 300 \mu\text{m}$. If the wire is stationary, i.e. the same portion of wire faces the workpiece for successive sparks, the wire might break due to the heat produced. Hence, the wire feed subsystem continuously moves the wire in front of the workpiece. It also controls the speed and tension of the wire. The wire is used either once or several times before it is discarded [24]. The dielectric flushing serves as the cooling medium as well as it flushes the debris particles after the material removal. The dielectric system controls the flow

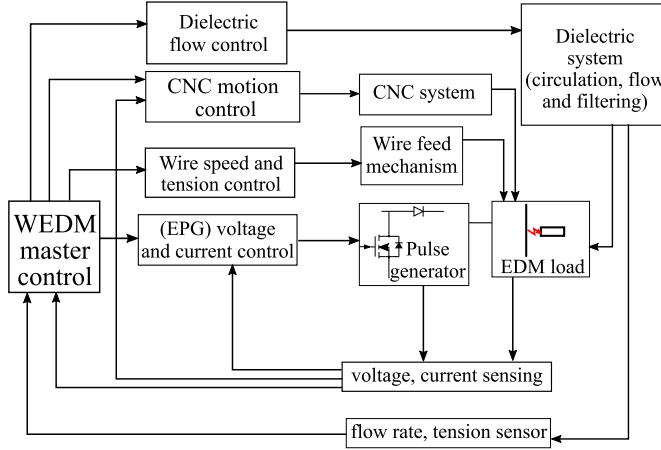


FIG. 1.7: Complete WEDM system structure

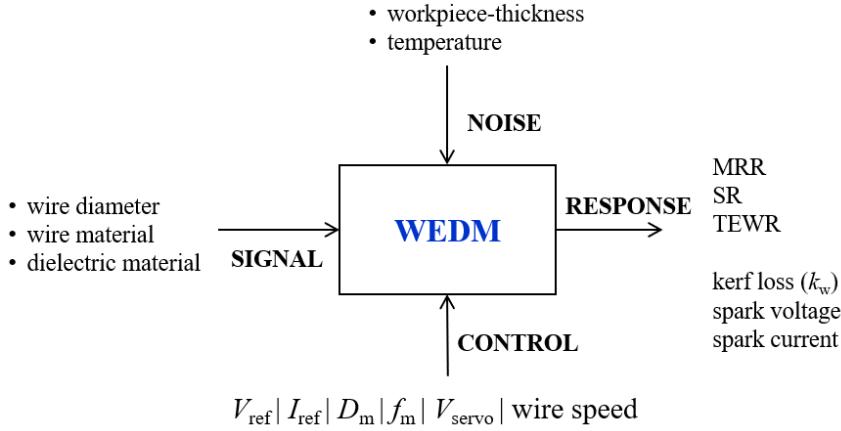


FIG. 1.8: P-diagram of WEDM system

rate of the dielectric fluid. The physics of the process can be altered by changing the dielectric fluid. Hence, the performance of the machine viz., MRR, surface finish etc., can be controlled by changing the dielectric fluid. Sometimes, instead of flushing only submerged type of dielectric system is used.

Another way to look at WEDM is as shown by the block diagram in Fig. 3.3. It is also called P-diagram from quality engineering perspective [28]. Here, ‘signal’ represents factors which the WEDM operator can select to get required performance. The ‘noise’ represents the factors which affect the process but the operator cannot set/select these factors. The ‘control’ represents the factors which the operator can set ‘freely’. These are usually factors available at the control panel of WED machine. Here, V_{servo} is the servo voltage [24] which is the reference voltage used by the CNC motion control.

The ‘response’ of WEDM is usually measured in terms of three important machining performance parameters [23]:

1. **Material removal rate (MRR):** This is the volume of the workpiece removed per unit time. It is usually measured in mm^3/min . In the case of slicing applications, it is also sometimes measured in mm/min .
2. **Surface roughness (SR):** Surface roughness is measured in roughness average (Ra) or total thickness variation (TTV) [29].
3. **Tool electrode wear ratio (TEWR):** Due to the heat generated by sparks, there is also some erosion of the tool, which is the wire in WEDM. Therefore, TEWR is the ratio of the eroded volume of the tool to the eroded volume of the workpiece. However, this parameter is more relevant in the case of DEDM than in the case of WEDM.

For slicing of semiconductor ingots, the other responses like kerf loss (k_w), spark voltage and spark current are also of interest.

1.3 Motivation

In spite of advantages of WEDM stated in Section 1.1, the WEDMs available in the market cannot be used “as they are” for slicing semiconductor ingots. The following issues need to be addressed, so that WEDM can be adapted for the ingot-slicing application. The points are also summarized as “challenges” in Table 1.1.

1. Understanding behavior of semiconductors vis-à-vis metals in WEDM:

When WEDM is employed for cutting semiconductors there is a discharge between the metallic wire and the semiconductor block. This is different from the metal-metal sparks occurring during cutting of metals with WEDM [26, 30, 31]. A better understanding of the physics of semiconductor cutting would be useful for modifications required in the machine/process especially for semiconductors.

2. EDM Pulse Generator (EPGs) - design and efficiency Improvement:

It would be necessary to design specialized pulse generators for WEDM made for cutting silicon. However, it is seen that there is no comprehensive literature, which can be used to design novel EPGs, from power electronics perspective. Also, the issue of modeling of the EPGs is not addressed in the literature till date.

Efficiency of EPGs is not dealt with thoroughly in the literature. Efficiency would be an important parameter once the WEDM becomes an important part in wafer manufacturing chain.

3. **Necessity of fully customizable WEDM:** The WEDMs available in the market are designed for cutting metals. Therefore, they provide a certain range of values within which the parameters can be varied. The range is obtained by manufacturers by prior experimentation. However, due to difference in physical properties of semiconductors and metals, it might be necessary to seek a set of parameter settings beyond the range offered by manufacturers. The settings include not only electrical pulse parameters like voltage, current, on time, etc., but also the other parameters like material of the dielectric, wire diameter, and wire speed. Therefore, there is a need of customizable WEDM which can be used to experiment with silicon.

Another disadvantage of commercial WEDM is that the spark-area cannot be probed easily to study the process physics. This is because of the high temperature of the spark and continuous flushing of the dielectric onto the spark make the placement of sensors near the spark very difficult in commercially available machines.

4. **Electrical forces in WEDM of semiconductors:** Forces of electrical origin are exerted on the wire in WEDM, which lead to wire vibrations. As the wire vibrates, the quality (flatness) of the cut surface is affected. Study of the forces for metallic workpieces is found several articles [32–34]. Analysis of such forces is not reported for semiconductor workpieces till date.

Such study is particularly important in the case of semiconductor-ingot-slicing operation due to the following reasons:

- (i) **Increase in effective kerf losses:** Due to wire-vibrations, the kerf width increases. Further, even if there is no significant increase in kerf width (in as-cut condition), the quality of cut surface is not good. The rough surface has to be smoothed by post-processing the wafers. Consequently, the net kerf width increases. More the surface roughness, more will be the effective kerf loss.
- (ii) **Increase in cost of post processing:** More the surface roughness, more will be the cost of post-processing.

5. **MWEDM– wire-wire forces and requirement of high tension:** WEDM cannot compete with the high throughput (several thousand wafers per day [5, 6]) of multi-wire-saw, unless MWEDM is developed. There have been certain attempts to develop MWEDM on prototype level [14, 35, 36], however there is no commercially available product in this domain.

Requirement of tension, as high as \approx 85-90% of failure strength of the wires, is reported in the MWEDM literature [14, 37]. One of the prime reasons behind this requirement is wire-wire forces, which are not investigated in the literature till date. There have been attempts to propose mechanical methods to alleviate the problem. However, such methods are *remedial* in nature, in a sense that, they will act upon the force which may try to deflect the wires against the applied tension. No method or scheme is proposed which would prevent the forces which are responsible for wire-deflection.

1.4 Scope of the Work

This research is hinged on the five points mentioned in the previous section. The following points describe the framework within which the work is carried out.

1. **Machining behaviour of silicon and steel in WEDM:** To get better understanding of behaviour of silicon while cutting with WEDM, investigation is done by systematic experimental work. L18 orthogonal array of Taguchi Method is used to set up the experiments to record current and voltage pulses during the spark-erosion. Important distinctions between the spark-erosion of silicon and steel are brought out in this study, which are particularly important for the applications considered.
2. **Design and development of WEDM pulse generator:** To help designing of novel EPGs, systematic study of EPGs is carried out from power electronics perspective. Typically, the articles in this domain are limited to the study of two main types of pulse generators viz., transistorized EPGs and RC oscillator type EPGs. In this work, classification and comparative study of 13 important EPG topologies is done considering their structure, control schemes, efficiency, component count, voltage stress, etc.

Further, hardware implementation is done for one of the topologies along with a detailed analysis and modeling in frequency domain. A novel control scheme is proposed which can improve the efficiency by 30%.

3. Design and development of miniature WEDM machine: A fully customizable miniature WEDM (mini-WEDM) is developed which can fit in a box of size 120 cm × 120 cm × 60 cm. This machine can be used to vary the process parameters and then find an optimum set of parameters for a particular semiconductor material. It can also be used to closely probe the sparks in WEDM, which is not possible with commercial WEDMs.

4. Analysis of electrical forces in WEDM and wire-wire forces in MWEDM: Earlier studies have reported differences in the nature of electromagnetic forces (in WEDM) for magnetic and non-magnetic metals. In this work, detailed analysis is done to quantify the forces in the case of semiconductors.

5. MWEDM - wire-wire forces and novel electrical supply schemes: It is found that in case of MWEDM, there exist wire-wire forces which are much stronger than the wire-workpiece forces. Detailed analysis of these forces is done from first principles and the results are verified by FEM analysis. An algorithm is also proposed to design MWEDM based on the quantification of maximum allowable deflection.

Based on the above analysis of wire-wire forces, novel supply schemes are proposed which can reduce the wire-wire forces in MWEDM to about 15-40% of that occurring in the conventional supply schemes. Analytical methods are developed to compute the forces and the results obtained by those methods are verified by FEM.

1.5 Organization of the Thesis

This thesis is divided into 8 chapters. Chapter 2 is dedicated for literature review. The chapter enlists important and relevant literature in all the five domains mentioned in the previous section.

The experimental work carried out to distinguish between the spark-erosion of silicon and steel is described in Chapter 3. Techniques in the field of design of experiments (Taguchi methods) are used to bring out distinguishing features of spark-erosion of silicon.

Chapter 4 presents classification and comparative study of 13 important topologies of the pulse generators for EDM. The comparison is based on their operation, control schemes, efficiency and voltage stress. MATLAB simulation results are also given to support the study. One of the topologies is realized in hardware. A detailed stage-wise modelling in frequency domain is presented in Chapter 5. The chapter also explains a novel control scheme to improve the efficiency by 30%. Experimental results are given to support the claims.

Development of the miniature WEDM is a major part of this research work. Hence, Chapter 6 is dedicated to the design and specifications of subsystems in the mini-WEDM. The kerf loss obtained with the machine is compared with that obtained using a commercial machine.

Chapter 7 discusses electrical forces in WEDM. Especially two cases are considered: (i) Analysis of forces for single-wire EDM with semiconductor workpiece (ii) Analysis of forces for MWEDM. An elaborate treatment is given to wire-wire forces in MWEDM. A method to estimate wire deflection is presented considering the wire as a string under tension. This is the first time that such a study is reported. Novel electrical supply schemes devised for MWEDM are also presented in Chapter 7 along with the pulse generator topologies for those schemes. Chapter 8 presents the summary of the work done and directions for future investigations in the research field.

Chapter 2

Literature Survey

Literature in all five sub-domains of research is enlisted in separate sections. Lacunae in the available literature and corresponding thrust areas are also indicated. At the end, the research presented in this dissertation is compared with respect to the work done till date in a tabular format.

The previous chapter described the background of how WEDM can prove to be an effective alternative for the conventional wire-sawing used for ingot slicing. The chapter has also outlined research gaps related to the adaption of WEDM by semiconductor wafer manufacturing industry and the directions of this research work. This chapter expounds the work that is already done by previous researchers in those directions.

However, initially, it is instructive to look at the literature on EDM/WEDM in general. There are two broad streams into which the literature relevant to the present research can be divided:

1. General literature on EDM/WEDM
2. Use of WEDM for slicing of semiconductors

2.1 General Literature on EDM/WEDM

WEDM is a complex process which involves interaction of electrical, magnetic, thermal, fluid, and structural phenomena along with plasma physics [23]. Texts books on

EDM/WEDM authored by Jameson [24], Jahan [17] and Sommer [38] are good starting points to understand the process and the machine from basics. The review papers related to EDM in general [23, 39, 40] and WEDM in particular [41] give a clear picture regarding a historical perspective and state-of-the-art research.

The literature on EDM/WEDM can be broadly categorized into four domains:

1. modelling of the process-physics [23, 42]
2. experimental investigations to study or optimize the process parameters [43, 44]
3. EDM pulse generators [45, 46]
4. patents related to the machine [47]

However, the focus area of this research is application of WEDM for wafer manufacturing. Therefore, the progress in this area till date is reviewed in the next section.

2.2 WEDM for Cutting Semiconductors

Use of WEDM to slice semiconductors is relatively new, with first reports given by Luo et al., in 1992 [48]. Later, Uno et al. [12] demonstrated the use of molybdenum wire for cutting 12 inch and 16 inch wafers. Peng and Liao [20] have stated that ID saw and wire saw can produce micro cracks and surface damage due to abrasives present in the process. They have stated that submerged type of WEDM can produce smoother surface at lower MRR, whereas the flushing type of WEDM has higher MRR at the cost of surface roughness. There have been several attempts to study various aspects of these methods since then [49–52]. A detailed chronological literature review can be found in [19, 53]. Punturat et al. [54] have reported experimental investigations of surface morphology of cutting n-type silicon. Some researchers have also reported cutting of other semiconductor materials like silicon carbide and germanium [15, 36, 37, 55, 56]. Especially, there are several attempts to develop multi-wire EDM for cutting SiC ingots [36]. Specific articles relevant to the presented research are listed in the following subsections.

The research in this domain started at IIT Bombay since 2009. The available wafer-dicing methods are compared with WEDM by Dongre et al. [13]. Joshi et al. [18]

have reported the effect of process parameters on cutting ultra-thin wafers ($\approx 130\text{-}150 \mu\text{m}$). The mathematical modeling of the process of spark-erosion of silicon is presented in [57]. In another paper, Joshi et al. [58] have reported experimental investigations into the effect of non-energy parameters on surface morphology and contamination of silicon wafers being cut. Effects of process parameters on variation in wafer thickness and surface roughness of ultra-thin wafers are investigated by experimental studies [18].

Thus, the research till date has demonstrated that WEDM can indeed prove to be an effective alternative for the traditional processes for wafer manufacturing. However, as stated in the previous chapter, further investigation is needed in the following domains.

1. Incomplete understanding of the physics of WEDM of semiconductors
2. EDM pulse generators: issues in efficiency and modeling
3. Unavailability of customizable WEDM
4. Analysis of electromagnetic force for semiconductor workpiece
5. Issue of wire-to-wire forces in MWEDM

Literature review specific to each domain is covered in the following sections. Significant contributions of the present work vis-à-vis those of the earlier literature are listed in Table 2.1 in Section 2.8.

2.3 Machining Behaviour of Silicon

Although DEDM was invented almost 60 years ago, the physics of spark-erosion in WEDM is not completely understood till date [59]. It is a complex process involving interaction of electromagnetic, thermal, fluid flow, plasma physics and mechanics [22]. Therefore, usually, various aspects of the process are modeled separately as described by Hinduja and Kunieda [32].

Studies in machining behavior of semiconductors can be broadly categorized into three subdomains:

1. Study of physics of machining of semiconductors with DEDM/WEDM

2. Studies reporting current/voltage waveforms in EDM/WEDM
3. Use of equivalent circuit to explain observed current/voltage waveforms

However, detailed investigations of current-voltage characteristics (CVC) and their comparison with steel is not found in the literature.

Study of physics of machining of semiconductors with DEDM/WEDM: The EDM process is not fully understood for metals [59] for which the process was discovered several decades ago. The process physics in the case of semiconductor machining is further complicated as the sparking takes place between metal and semiconductor. The electrical, mechanical and thermal properties of semiconductors are different from those of the metals [60]. Therefore, spark-erosion of semiconductor is a complex problem which is not fully understood.

Peng et al. [20] have reported the effect of t_{ON} on kerf loss, surface roughness (R_a) and Total Thickness Variation - TTV for a silicon workpiece cut with WEDM. They have also stated that the difference in physical properties of silicon and metals leads to distinct temperature profiles, heat production and cutting rates. However, they have not quantified this phenomenon. Wang et al. [61] have compared the surface roughness, reflectivity and micro-structural profile of cut silicon wafers using Wire Electric Spark Hybrid Machining (WESHM) with those cut with WEDM. Punturat et al. [54] have investigated how surface characteristics of n-type monocrystalline silicon ingots cut with WEDM is affected by open voltage and dielectric flushing rate. Huijun et al. [62] have analyzed small holes obtained after machining of silicon with EDM and stated that the following two properties are responsible for the observation: (a) the difference in absolute resistance of silicon (b) increase in resistivity of silicon with temperature. Zhidong et al. [63] have proposed a novel control system based on current pulse probability (ratio of normal discharges to short circuit discharges) because the voltage does not drop much while cutting semiconductors with WEDM. Hence, conventional mechanism based on detection of average voltage may not work. Mujumdar et al. [64, 65] have proposed a comprehensive coupled field model of single discharge in micro-EDM. The model contains interaction of plasma chemistry, bubble dynamics, power balance and electrical circuit.

Studies reporting current/voltage waveforms in EDM/WEDM: The current/voltage waveforms and CVC of spark can yield a significant information about the

spark-physics. This is reported by few researchers as follows. Li et al. [66] have reported spark current and voltages for several metals including cast iron, tungsten, 40Cr-steel, etc. Yang et al. [67] have analyzed current and voltage waveforms for micro-EDM of metals, ceramics and p-type monocrystalline silicon with RC pulse generators. They have observed that a low conductivity material like p-type monocrystalline silicon results in higher spark voltage than that of the metals. Zhao et al. [15] have compared the characteristics of cutting SiC with steel and they have reported that machining rate of SiC is higher than that of steel. They have also reported a voltage and current pulse waveform for spark-erosion of SiC and steel. However, their analysis is not *based* on the pulse waveforms. Mendes et al. [68] have demonstrated an on-line voltage and current monitoring system developed for WEDM using LabVIEW. They have illustrated how the system can be used to quantify the cutting rate as a function of discharge duration and discharge delay time.

Use of equivalent circuit to explain observed current/voltage waveforms:

Mingbo et al. [69] have investigated the unidirectional nature of spark current while cutting silicon with EDM. They have proposed the existence of two Schottky junctions while cutting of semiconductors. Chen et al. [70] have studied the multi-channel spark discharge phenomena in machining semiconductors with WEDM. They have confirmed the existence of higher potential difference between the surface of the semiconductor and the wire except at the point of actual discharge. They have stated that the spark voltage is higher whereas the current is lower for silicon than that for metals. However, they have not provided any quantitative measure for this phenomenon.

On one hand there are studies which try to propose the underlying mechanisms in spark-erosion of silicon. On the other hand there are studies which try to propose circuit models for the spark-erosion of silicon [69]. However, an analysis completely based on voltage and current pulse trains is not found in literature.

In the present study, Taguchi method based experiments are used to bring out the differences using the recorded spark current and spark voltage pulses. The equivalent circuit model proposed by Mingbo et al. [69, 70] is used to explain the observed phenomena wherever necessary.

2.4 Pulse Generators for EDM

Classical literature on EDM [17, 23, 24] mentions only two types of EPGs viz., RC pulse generators and transistorized pulse generators. They are discussed from production engineering perspective. A review of EPGs from historical perspective is reported by Sen et al. [45] and Lauter et al. [71]. EPGs represent a special class of converters which are distinct due to the cyclic nature of EDM load and existence of two dominant frequencies. Broadly, the literature in this domain can be categorized as:

1. articles in mechanical engineering domain
2. patents
3. articles in power electronics domain

Articles in mechanical engineering domain: Chen et al. [72] have proposed a pulse generator which is a modified form of a transistorized pulse generator. Han et al. [73] have proposed a transistorized iso-pulse generator which can provide pulses with discharge duration of 30-80 ns and hence improve MRR as compared to RC type pulse generators. These are particularly suitable for micro-EDM. Mysinski [74] has used TOP-switch based voltage source and current source, along with interfacing circuit composed of an H-bridge to construct a low power (35 V, 3 A) EPG. Wang et al. [75] have used very high frequency resonant pulse generator for micromachining on mesoscopic scale. Hu et al. [76] have proposed a multi-mode RC pulse generator. Mahmud et al. [77] have reported use of transistorized pulse generator for micro-machining of hip-implants.

Patents: Ozaki et al. [47] proposed first transistorized power supply in which multiple transistors are used in place of single transistor so that the current capability of the EPG increases. Kinbara et al. [78] have disclosed two EPG topologies which have an explicit interfacing circuit. Martin et al. [79] have also suggested two circuit topologies along with a special control scheme which controls rate of rise of spark current so that the TEWR is minimum. Okane et al. [80] have put forth an H-bridge like converter for EDM with a control scheme to keep the ratio of OFF time to ON time (t_{OFF}/t_{ON}) minimum. This scheme is proposed to improve the material removal rate. Nakashima et al. [81] describe high frequency AC voltage supply schemes for providing pulses for WEDM such

that the electrostatic forces between the wire and the workpiece are minimized, resulting in reduced SR and improved straightness accuracy.

Articles in power electronics domain: Tastekin et al. [46] have proposed a dual converter based topology in which one converter acts as a voltage source and the other acts as a current source. Lin et al. [82, 83] have proposed four phase interleaved buck converter with energy recovery scheme so that the ripple in the output current is less with a low value of inductor in individual DC-DC converters. Casanueva et al. have proposed several forms of EPG topologies consisting of LCC resonant converter [84–93]. This class of EPGs is proposed for a specific application of portable onsite machining. Odulio et al. have proposed a topology using an LLC resonant converter as well [94]. Looser et al. [95] have proposed a topology for the application of removing metal chips using dry EDM, where dielectric is air and spark gap is ≈ 1 mm. Hence, high voltage (≈ 1 kV) is provided by the cascaded connection of an H-bridge inverter, a high voltage transformer and a diode bridge rectifier. A circuit topology with adaptive voltage positioning control is reported by Yang et al. [96].

However, there is no systematic study of EPGs in any book or article from power electronics perspective. Significant amount of literature on EPGs is in the form of patents filed by EDM/WEDM manufacturers. Being in the patent format, their operation is not explained in detail. Therefore, there is a need of a structured account of available EPG topologies. Further, the efficiency computation of these converters is not treated thoroughly in literature. The efficiency is important for the ingot-slicing application as explained in Section 4.4. In this thesis, this issue is discussed along with the control schemes, voltage stresses and component count for 13 important EPG topologies. It is found that the efficiency of many topologies is of the order of 30-40%. A novel pulse current reference scheme is proposed in this thesis to improve the efficiency of the EPG proposed by Tastekin et al. [46] by 30%. The scheme is also verified by experimental results.

2.5 Development of Miniature WEDM Systems

As stated before, one of the contributions of the present work is design and development of a small-sized customizable WEDM machine. It can serve the purpose of experimenting

with silicon with wide variation in process parameters which is a difficult task with commercial WED machines.

A schematic of complete WEDM system is quite complex as shown in Fig. 1.7. As it involves four different subsystems, design of commercial WEDM system requires knowledge from a variety of engineering disciplines. The information/knowledge regarding design of machine or its subsystems is not found in a single resource, but mainly in patents filed by multinational enterprises which manufacture these machines. The text books [17, 24, 38, 97] and review papers [23, 39] are used to get guidance for design of various subsystems. Usually, commercial WED machines are designed such that they are able to cater to jobs of all sizes from smaller to larger jobs. However, recently, there have been some attempts to make small sized WEDM or EDM machines. The important literature covering such attempts is given below.

Hayakawa has built a WEDM where the wire feed mechanism is fitted inside the dielectric tank to reduce the overall size [98]. There are several patents related to small sized or movable/portable DEDM systems, devised for cutting workpieces which are so large in size that it is difficult to bring them near the machine [99–106]. Fleming’s “The EDM How-to Book” gives a good “Do-It-Yourself (DIY)” information mainly for any person having basic knowledge of engineering, to build an EDM machine [107]. Furutani et al. [108] have reported development of a machine for making a wire-coating by electrical discharges. Although the machine utilizes the principle of electrical discharges, it is essentially not an EDM machine. Apart from these, there are several resources on the internet which are used to build the mini-WEDM machine. They are listed in Section 2.8.

While building a machine, basics of mechanical engineering design are taken from classical text books like Shigley’s Mechanical Engineering Design [109].

2.6 Forces in WEDM

Four types of forces are known to be present in WEDM: (a) discharge reaction force (b) hydrodynamic force (c) electrostatic force and (d) electromagnetic force [32]. The discharge reaction force appears at the instant of gap breakdown due to rapid expansion of bubble. As the wire and the workpiece are always in the liquid dielectric environment,

the liquid-flow exerts *drag* which is classified as hydrodynamic force. The electrostatic force is present during ignition delay time or during an open pulse (i.e. when the voltage pulse is applied but the spark gap does not break down). Electromagnetic force appears due to generation of eddy currents in the workpiece. These forces are important from viewpoint of SR and geometrical accuracy as follows: (a) Unintended concavity appears in case of straight line cuts (b) Geometrical accuracy of corner cuts is affected (c) Surface roughness in terms of R_a , TTV increases. There are few research articles which deal with forces of electrical origin in WEDM as outlined below.

Iwata et al. [33, 110, 111] have investigated the effect of forces on WEDM for the first time. They have used the wire-plane geometry for computation of electrostatic force. Han et al. [34] have considered force value obtained by analytical solution as input to the structural analysis. They have considered a string vibration model to conclude that if the machining frequency matches with the natural frequency of vibrations of the wire, a resonance may occur and maximum amplitude of vibration may increase such that a short circuit might occur. They have validated findings of simulations with the marks obtained on the machined surface due to wire vibrations.

Obara et al. [33] have commented briefly about the nature of electromagnetic forces. Tomura and Kunieda [112] have analyzed electromagnetic forces with 2D-FEM simulations, with copper and steel as workpiece materials. Volgin et al. [113] have presented similar results about the forces, stating that the forces are attractive for steel workpiece and they are repulsive in the case of aluminum or copper workpiece. In another article [114], they have elaborated on variation of forces with depth of cut. The findings are verified by sensing wire movement with the help of optical sensors. Chen and Zhang [115] have employed a set of designed experiments to study the corner deformation. They have also done FEM simulations to qualitatively explain the nature of forces in case of 6061 Al alloy and Q235 steel. The simulations are distinct as they have assigned a finite conductivity to the spark channel, whereas the earlier researchers have used a dielectric material as surroundings which has negligible conductivity as compared to the metals. They have suggested practical methods viz., adjusting machining parameters and adapting the wire path in accordance with the forces as corrective measures to get accurate cutting. Conde et al. [116] have carried out experimental investigations to find out deflections of the wire and the resulting concavity of the cut surface. They have shown that the concavity is a function of radius intended to be cut from the workpiece.

All the researchers have analysed the forces for cutting metals. The forces in case of silicon are not investigated. Furthermore, for MWEDM, there are multiple wires which exert forces on each other. These forces are not investigated till date. In this work, these wire-wire forces are studied with both analytical and numerical approaches. Also, an algorithm to design MWEDM based on wire-deflection is given.

2.7 Multi-Wire EDM

First investigations of MWEDM were reported in form of three-wire EDM for slicing of silicon ingots by Okamoto et al. [117]. Bamberg and Rakwal have patented MWEDM for slicing semiconductor ingots [14]. Okamoto et al. [118] and Kimura et al. [37] have demonstrated experimentally that narrower kerf can be achieved with a track-shaped brass coated steel wire. Itokazu et al. [16] have explored MWEDM for dicing of SiC ingots, because multi-wire sawing becomes difficult with increasing diameter of ingots. They have presented results for cutting 100 mm² SiC ingot with 10-wire EDM. Ogawa et al. have demonstrated that surface roughness can be reduced with WEDM as compared to wire sawing by conducting experiments with 10-wire EDM for cutting 6-inch SiC ingots [119]. Okamoto et al. have investigated the influence of height of workpiece on kerf width to study cutting of circular ingots [36]. They stated that feed rate plays an important role in deciding the kerf width.

There are several patents dedicated to features specific to MWEDM [120–125]. Wai [120] and Takashi et al. [125] have proposed a wire-feed mechanism specially for MWEDM. Kazuhiko et al. [124] have presented an automatic (motorized) winding mechanism for the wires in the MWEDM, such that most of the pre-machining tasks are automated, thereby reducing the time required. Patent by Masatake et al. [123] gives a mechanical assembly which consists of a work presser, a box-shaped member with trapezoidal protrusions which can be pressed into the cut-side of the ingot so that the breakage of wafers due to bending can be avoided. Takashi et al. [122] have proposed a patent which describes a control method to reduce destabilization in the machining (variation of machining) process and disconnection of the wire due to variation of cutting width of cylindrical ingots. The location of discharge point is calculated by means of a current sensor at both electrical contacts of the wire. For the MWEDM, sensing of voltage between adjacent supply points is also necessary in addition to sensing of the current

flowing in the wires. Cutting width is calculated by the difference between upper limit and lower limit of the discharge position. Simon et al. [121] have proposed an MWEDM method for cutting cuboid shaped sintered rare earth magnets of 0.8 mm width.

In all of the reported work, the wire pitch (distance between adjacent wires) ranges from 0.5 mm to 1.1 mm and the wafer thickness ranges from 100 μm to 360 μm . Minimum allowable wire pitch is decided by the amount of wire vibrations. Kimura et al. [37] stated that higher than normal tension is required in case of MWEDM to reduce wire vibrations. They have explored the following ways to minimize wire vibrations: (a) use of track-shaped wire electrodes instead of circular wires (b) giving side support to wires and (c) reducing of distance between wire guides. However, these parameters are determined only experimentally, and hence, it is necessary to provide analytical support to quantify deflections of the wire. It is proposed in the present work that, the wire-wire force is a significant contributor to the wire deflections.

Besides slicing semiconductor ingots, MWEDM is also useful for other applications like:

1. production of thin metallic plates used for sputtering targets [122]
2. cutting of rare-earth magnetic materials, etc. [121]

In general, MWEDM can find widespread applications where conventional multi wire-sawing is used.

Although the MWEDM systems are developed by various industries on prototype level, no MWEDM system is available on commercial scale. One of the hurdles is requirement of high tension for the wires as reported by [14, 37]. In this work, novel electrical supply schemes for MWEDM and the corresponding EPG topologies are suggested to alleviate the issue. While the mechanical methods proposed by earlier researchers are mainly remedial in nature, the schemes in this work are preventive in nature. That is because, the schemes try to reduce the generation of force itself which is responsible for wire vibrations.

2.8 Salient Contributions

The following table gives a comparison of contributions by previous researchers with the work presented in this thesis.

TABLE 2.1: Salient contributions of this work vis-à-vis the work done by earlier researchers

Behaviour of Silicon in WEDM		
Main researchers and references	Contribution	Remarks
Schumacher, Hinduja, Kunieda, etc. [23, 32, 59, 64, 65]	Various aspects of modeling of DEDM/WEDM process are discussed.	The discussion is mostly limited to cutting of metals. Modelling of the process for silicon is not investigated.
Peng, Wang, Punturat, Mingbo, etc. [20, 54, 61– 63, 70, 126]	These articles are dedicated for discussion of the processes especially in the case of machining of silicon.	Few of the articles have reported current and voltage waveforms of spark, however, the works are not based on the CVC of spark.
Yang, Zhao, Mendes, etc. [15, 67, 68, 127]	These articles report investigations into current/voltage waveforms of EDM/WEDM.	The studies are limited to the CVC of spark erosion of metals. No study is done for semiconductors.
Mingbo, Chen, etc. [69, 70]	Unidirectional conductivity is investigated by using CVC. A representative circuit model is proposed which consists of two Schottky diodes and one Zener diode.	The motive of the study is to understand unidirectional conductivity. There is scope to analyse differences between the behaviour of silicon and that of steel during spark-erosion.

This work	<p>1. Spark-erosion of semiconductors is investigated using pulse parameters of current and voltage waveforms obtained by systematic experimentation using Taguchi methods.</p> <p>2. It is shown that, the current in the spark-erosion is not linearly related to the conductivity of silicon. It is related to the nonlinear behavior of metal-semiconductor junction present at the interface of spark and workpiece.</p>	<p>The implications of the findings on the equivalent circuit of the spark erosion as seen by the pulse generator are given for the first time. Further, guidelines are also provided regarding the design of new pulse generators.</p>
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EDM Pulse Generator		
Kinbara, Okane, etc. [47, 78, 80]	<p>Several pulse generator topologies are proposed in these patents. Some special control schemes are also suggested along with the circuit topologies to achieve specific machining performance parameter.</p>	<p>Modeling of the converter topologies is missing in all the patents. Also, experimental results are not presented in many patents.</p>
Lin, Casanueva, Yang, Looser, Tastekin, etc. [46, 82–93, 95, 96]	<p>These articles have proposed novel EPG topologies with analysis from power electronics perspective. Principle of operation and experimental results are proposed in many articles.</p>	<p>Several researchers have tested the topologies with resistive load and not with actual WEDM. Efficiency of the pulse generators by experimental method is not reported [82, 83, 96].</p>

This work	<ol style="list-style-type: none"> 1. A classification and comparative study of pulse generators is done for the first time. 2. Detailed modeling with respect to three distinct stages of operation is done. 3. A novel control scheme is proposed to improve the efficiency of a topology by 30%. 4. Experimental results are given to validate the scheme. 	<p>The review of pulse generators would help the power electronics engineers to develop the systems further. The modeling method can be applied to other topologies of EDM.</p>
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Development of Miniature WEDM Systems		
Jameson, Jahan, Sommer, Guitrau, etc. [17, 24, 38, 97]	These are text books on EDM. Functioning of various subsystems in EDM can be understood using these books.	Functioning of mechanical subsystems is described in detail. However, functioning of pulse generator is not dealt with in detail.
Hayakawa, Wang, OhJai, etc. [98–103]	These are patents which have proposed small-sized DEDM systems.	Most of these innovations are related to DEDM and not WEDM. Also, the applications considered here are different from cutting of semiconductor ingots.
Ben Fleming [107]	This book gives a good ‘DIY’ procedure for making EDM systems.	Several important design considerations are given to develop DEDM. However, the book is for a common person and hence it lacks some essential technicalities. Also the details of pulse generator are not given in the book. Several other technical details of the electrical system are also missing.

Internet resources [128–131]	These resources describe making of a DEDM or WEDM on prototype scale.	The videos are made by hobbyists and hence volume of the machine is not necessarily their concern. Most of them also lack information about EPGs.
This work	<p>1. Design and development of miniature WEDM system which can fit in size $120 \times 60 \times 60$ cm.</p> <p>2. All the subsystems are designed such that they can be used for a variety of applications with minor changes.</p>	<p>The miniature WEDM can be used for research purposes and also for making small parts used in medical, plastic moulding and other industries. This would be particularly useful for research institutes and small scale industries who cannot afford large and costly machines.</p>
Forces in WEDM		
Obara, Han, Kunieda, etc. [33, 34]	These papers report computation of electrostatic forces by using a cylinder and plane geometry. Han et al. [34] have modelled the wire as a string and calculated its natural frequencies.	The cylinder and plane geometry is valid only when the wire is outside the workpiece. When the wire goes inside the workpiece, different geometry needs to be used.

Tomura, Chen, Kunieda, etc. [112, 114, 115, 132]	<p>These articles present the computation of electromagnetic forces on the wire. They have proved that the nature of force is different for magnetic (e.g. ferromagnetic steel) and non-magnetic (e.g. copper or aluminium) materials. 3D computation of electromagnetic forces is done by Chen et al. [132].</p>	<p>No computation is done for semiconductors. No specific formula is given for electromagnetic forces. Most of the researchers have used trapezoidal current waveform. Other types of waveforms like triangular and exponential found from experimentation are not used for simulations.</p>
This Work	<ol style="list-style-type: none"> 1. Computation of electrostatic and electromagnetic forces for semiconductor workpiece is done by using FEM. 2. It is shown that the electrostatic forces are stronger in the case of silicon workpiece than the electromagnetic force. 3. Analytical formulation is presented for computation of wire-wire force in WEDM and it is validated by FEM. 4. It is shown that the wire-wire forces are dominant in MWEDM than the wire-workpiece forces. 	<p>The force computation is important because it can affect the wire vibrations which would determine the surface finish of wafers cut with WEDM.</p>

Multi-Wire EDM

Bamberg, Rakwal, etc. [120, 122– 125, 133, 134], [135–139] [140]	These patents are dedicated primarily to design of mechanical parts in MWEDM. There are two main types of MWEDM seen in the patents: (a) single wire is wound over multiple guide rollers and (b) multiple wires are used with multiple rollers	Electrical supply schemes of MWEDM are not mentioned. Also, there is no mention of wire to wire electromagnetic forces.
Simon Regis Louis, Chen, Yang, etc. [121] [141]	These inventors have proposed multi-wire EDM for cutting magnetic materials.	They have not specified wire-wire electromagnetic forces in the setup.
Hashimoto Takashi, Fuchiyama Masatake, Kurihara Haruya, Tawa Yasunobu, etc. [142–146]	These patents have proposed circuit topologies or their control schemes, specifically for MWEDM. Various issues tackled by the circuit topologies or the control schemes are: (a) requirement of large power (b) detection of short circuit (c) maintaining same current through each wire out of several wires (d) increased cost of power supply	All the circuit topologies and control schemes are proposed for the conventional type of electrical supply. Therefore, they are not similar to the ones proposed in this work.
Okamoto, Kimura, Itokazu, Ogawa, etc. [16, 36, 37, 117, 119]	Results of experimental investigations of cutting SiC blocks with 3-wire, 10-wire and 40-wire MWEDM are reported in these articles.	Kimura et al. [37, 118] have reported that higher than normal tension is required for MWEDM. They have also proposed various mechanical means to reduce the vibrations like side supporting wire, use of track-shaped wires, etc.

This work	<ol style="list-style-type: none"> 1. In order to reduce the wire-wire electromagnetic forces, novel electrical supply schemes are proposed. 2. Novel pulse generator topologies are also proposed for the novel supply schemes. 3. It would help the designers to develop functional MWEDM with reduced wire tension and hence reduced chances of occurrence of wire-breakage. 4. Positive-Zero-Negative type of polarity is used for the first time in MWEDM. 	<p>None of the articles by previous researchers discuss wire-wire forces. Therefore, the analysis and schemes presented in this work are novel.</p>
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Chapter 3

Electrical Characterisation of Spark-erosion in WEDM: Silicon and Steel

This chapter describes experimental work done to distinguish between spark-erosion of silicon and steel, using current voltage characteristics (CVC). The efforts can be divided into two parts: preliminary experiments done to understand the primary effect of process settings on CVC and the systematic experiments done by Taguchi Method. Differences in the equivalent circuit of WEDM sparks as seen by the pulse generator are brought forth from the statistical analysis. Based on the observations, guidelines are provided to design a WEDM customized for silicon.

3.1 Introduction

In general, the characteristics of EDM sparks can be gauged in terms of: (a) mechanical performance i.e. MRR, SR, and TEWR, (b) spark current and spark voltage waveforms, and (c) thermal or photographic images captured with thermal or a high speed camera [22]. This work focuses on spark voltage and current waveforms to understand sparks in WEDM of silicon and presents their comparison with those observed in steel. Specifically, WED machining of silicon is compared with that of steel as a base, with two approaches

TABLE 3.1: Properties of silicon and steel

Property	Silicon	Steel
Electrical Conductivity (S/m)	32.77	4.63×10^6
Temperature coefficient of resistivity ($^{\circ}\text{K}$) [147, 148]	(−0.005) to (−0.0015)	0.004 to 0.006
Relative permittivity	11.2	1
Relative permeability	≈ 1	≈ 1

of experimentation (a) one factor at a time (OFAT) and (b) design of experiments (DoE).

It is expected that the WEDM-sparks in the case of silicon workpiece would show distinct characteristics than those in the case of metallic workpiece due to difference in their mechanical, thermal and electrical properties. As this work is mainly focused on electrical characteristics, Table 3.1 lists properties of silicon and steel [60], which clearly indicate the differences in the two materials. The electrical conductivity is obtained from experimentation as mentioned in Appendix A.

This chapter is organized as follows. Section 3.2 describes approach to the experimentation in the form of two methods used and the statistical parameters. Results of both methods of experimentation and the corresponding discussion are given in Section 3.3. In section 3.4, the inferences pertaining to equivalent circuit of spark erosion as well as those pertaining to design of new EDM system are presented. The last section gives the concluding remarks.

3.2 Approach of Experimentation and Analysis

3.2.1 Theme of the experiments

In this work, experiments are performed on a flushed type dielectric to record pulse train data. The pulse parameters are then obtained by post-processing the data. It should be noted that the usual performance parameters i.e. MRR, SR and tool electrode wear ratio (TEWR) are not recorded in this work, although some inferences regarding MRR and SR are indeed drawn.

TABLE 3.2: Specifications of the Experimental Setup

Machine	ServoControl High Quality Wire Cut EDM BM400C-C
Wire (anode)	Molybdenum wire with OD = 180 um
Dielectric fluid	Water
Workpiece (cathode)	p-type silicon and steel
Workpiece dimensions	22 mm × 74 mm × 42 mm
Voltage probe	Standard probes for Yokogawa DL850E DSO
Current probe	Tektronix A 622

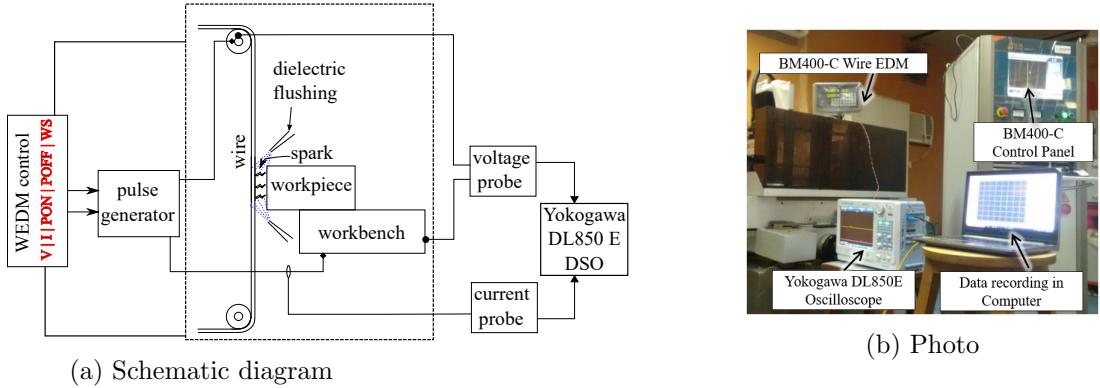


FIG. 3.1: Experimental setup

3.2.2 Experimental Setup

The experiments are conducted on BM400 Servo Control Wire Cut EDM (referred to as BM400 machine hereafter). A schematic and a photograph of the experimental setup are shown in Figs. 3.1(a) and 3.1(b), respectively. A Molybdenum wire of $\phi 180 \mu\text{m}$ is used in the experiment. Silicon and steel blocks are used as workpieces. The other details of the experimental setup are given in Table 3.2. The machine is a flushed dielectric type of WEDM, where deionized water is continuously flushed onto the spark gap. The input settings or parameters which an operator can set in WEDM are termed as ‘factors’ in DoE parlance [28]. There are five ‘factors’ available in the BM400 machine - V, IP, PON, POFF and WS as indicated in Fig. 3.1(a).

The experiments are conducted in two stages. In the first stage, one factor at a time (OFAT) approach is used to get preliminary differences between silicon and steel. In the second stage, systematic experimentation is done using robust design methods [28]. The methodologies and objectives of the two stages are elucidated in the following subsections.

3.2.3 OFAT Experimentation

The experiments in this stage are performed by varying one factor at a time and keeping the remaining factors constant. For one set of factors, four to five pulses are recorded. Overall, more than 500 of such pulses are recorded for silicon and steel. Fig. 3.2 shows three sample pulses for $V = HV$, $IP = 3$, $PON = 10$, $POFF = 18$, $WS = 2$. Section 3.3.1.2 elaborates on the observations made from the voltage and current plots in Figs. 3.2(a) and 3.2(b), respectively. There are two main objectives of this experimentation¹:

1. **To find correlation between input-factors and pulses:** Usually, the WEDM systems allow the user to select factors in terms of indices. The relationship of these factors with the pulse parameters is not given by the machine manufacturer. For example, the voltage setting in BM400 has two levels: LV and HV. However, a WEDM-operator does not know the actual voltage values in volts. The preliminary experiments are done to get a quantitative relationship between the indices and the pulse parameters.
2. **To investigate prima-facie difference between silicon and steel:** Preliminary or qualitative differences in pulse train data for spark-erosion of silicon and steel are observed. It is also interesting to see, how the actual waveforms appear in comparison with the ideal waveforms given in the EDM literature [17, 24].

3.2.4 Systematic experimentation by DoE techniques

Once the relationship between indices of factors and pulse parameters is established, systematic experimentation using robust design methods is done for the characterization exercise. A P-diagram of this problem is shown in Fig. 3.3. Here, the settings available on the machine are ‘independent’ factors as the user can set their levels. The response is measured in terms of four parameters derived from voltage and current pulses, such as V_{max} , V_{avg} , I_{max} and E_p . These pulse parameters vary with each pulse and several pulses are recorded for each experiment. Fig. 3.3 shows summary statistics used to express outcome of an experiment in the form of a single metric.

¹Some part of this work is published as:
M. M. Kane, A. Jadhav, M. Kumar, S.V. Kulkarni, S.S. Joshi, “Machining Behaviour of Silicon in Wire EDM for PV Applications”, *EU PVSEC, European PV Solar Energy Conference and Exhibition, Amsterdam, 25 - 29 September 2017*, pp 333 - 338.

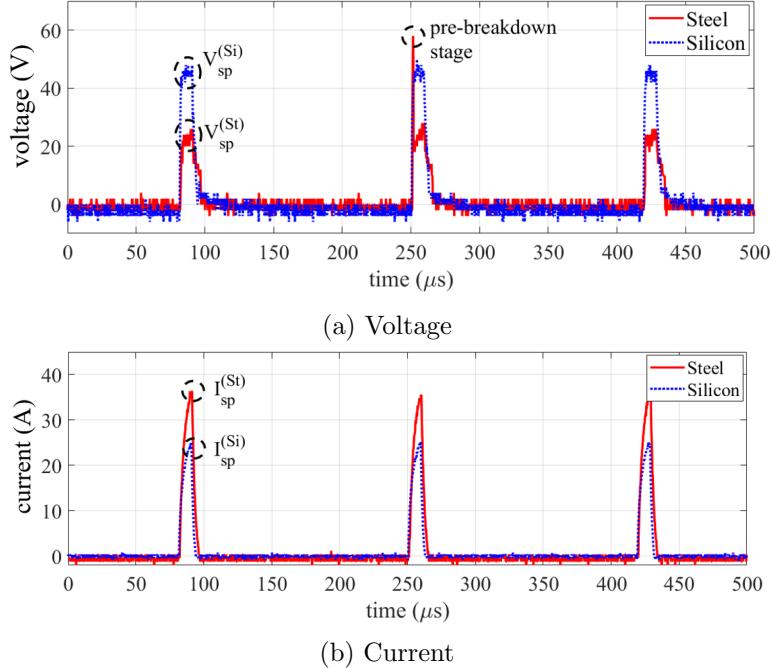


FIG. 3.2: Preliminary pulse waveforms for silicon and steel

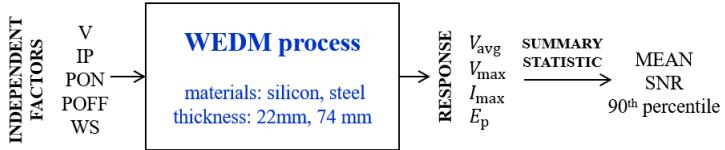


FIG. 3.3: P-diagram of WEDM system

TABLE 3.3: Factors and levels for design of experiments

Parameter	Levels selected for DOE		
	1	2	3
Voltage (V)	LV (75 V)	HV (110 V)	-
Current (IP)	2	4	6
ON time (PON)	12	14	18
OFF time (POFF)	16	18	20
Wire Speed (WS)	0	1	3

Particularly, two levels of ‘V’ and three levels of the remaining factors are chosen as shown in Table 3.3 to form L18 orthogonal array (L18 OA), see Table 3.4. For each experiment, data is recorded using Yokogawa DL850E ScopeCorder and Tektronix A622 current probe for 50 ms, with sampling interval of 0.1 μ s. The total duration of recording is the same for each experiment, however, the pulse period T_m is varied for each experiment. Therefore, the number of pulses N_p for each experiment are different which are given in Table 3.4.

Two sets each of L18 OA are performed on silicon and steel samples: set A is performed

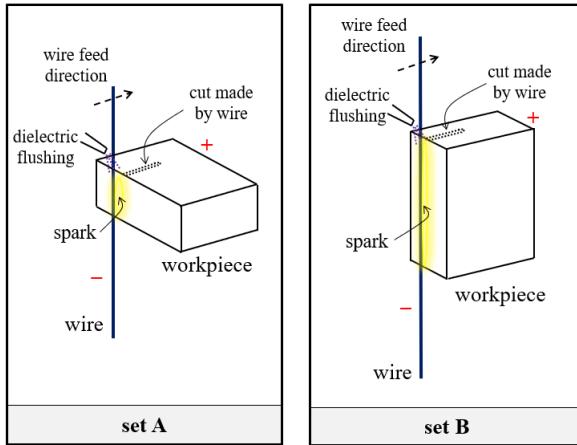


FIG. 3.4: Schematic picture of two sets of L18 OA experiments

TABLE 3.4: Details of L18 orthogonal array

Exp. No	V	IP	PON	POFF	WS	Number of pulses
1	75	2	12	16	0	276
2	75	2	14	18	1	210
3	75	2	18	20	3	146
4	75	4	12	16	1	276
5	75	4	14	18	3	209
6	75	4	18	20	0	145
7	75	6	12	18	0	245
8	75	6	14	20	1	188
9	75	6	18	16	3	183
10	110	2	12	20	3	221
11	110	2	14	16	0	236
12	110	2	18	18	1	162
13	110	4	12	18	3	244
14	110	4	14	20	0	188
15	110	4	18	16	1	182
16	110	6	12	20	1	220
17	110	6	14	16	3	235
18	110	6	18	18	0	161

on the shorter side (22 mm) of the workpiece and set B on the longer side (74 mm) of the workpiece, as shown in Fig. 3.4. Therefore, L18 OA is performed four times, two times for the two materials and two times by varying workpiece thickness (height of cut), thus amounting to 72 experiments in total. Typical characteristics of some pulses from experiment 1 in set A are shown in Fig. 3.5. Here, all the pulses are plotted together to bring out pulse-to-pulse variation as described in the subsequent sections.

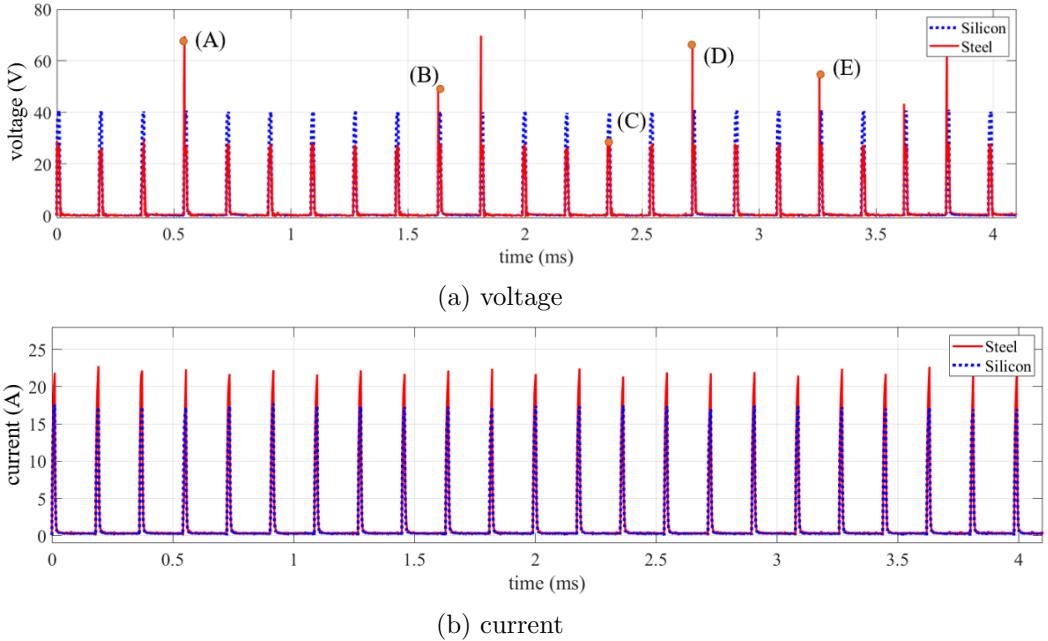


FIG. 3.5: Pulse train recorded for silicon and steel for exp 1 in set A

3.2.5 Pulse parameters

The following pulse parameters are considered for the comparative study.

1. **Maximum current (I_{\max})**: It is the maximum value of current obtained for a current pulse signal. $I_{\max} = \max(i(t))$
2. **Maximum voltage (V_{\max})**: Similarly, it is the maximum value of the corresponding voltage pulse signal. $V_{\max} = \max(v(t))$. The maximum voltage indicates the spark voltage V_{sp} in the case of silicon (see Figs. 3.2(a) and 3.5(a)). Because of the pulse-to-pulse variation in steel, V_{\max} for steel indicates either different values of pre-breakdown voltage as indicated by (A), (B), (D), and (E) in Fig. 3.5(a) or the sparking voltage as indicated by (C) Fig. 3.5(a) or in Fig. 3.2(a).
3. **Average voltage (V_{avg})**: It is the average value of the voltage signal over one pulse. With T_m as the period of pulse, it is calculated as follows:

$$V_{\text{avg}} = \frac{1}{T_m} \int_0^{T_m} v(t) dt \quad (3.1)$$

For an ideal spark voltage waveform (in Fig. 3.8(a)), V_{avg} is given by

$$V_{\text{avg}} = \frac{V_{OC}(t_1 - t_0) + V_{sp}(t_2 - t_1)}{T_m} \quad (3.2)$$

V_{avg} is important for two reasons:

- (1) The pre-breakdown period is negligible as compared to the sparking period in most of the cases i.e. $(t_1 - t_0) \ll (t_2 - t_1)$, therefore, V_{avg} is indicative of V_{sp} .
- (2) V_{avg} is often used by CNC control system in the WEDM to sense state of the pulse and hence to control advancement or retraction of the wire electrode [24]. Therefore, this parameter helps to gauge the difference in the gap voltage for silicon and steel.

4. **Pulse energy (E_p)**: Energy of a pulse is evaluated as follows:

$$E_p = \int_0^{T_m} i(t)v(t)dt \quad (3.3)$$

It is noted by the earlier researchers that the total force on a wire in WEDM is proportional to pulse energy [149], especially in the case of iso-energy pulse generator. Therefore, E_p can give an indication of the force experienced by the wire while machining and consequently of the quality of cut surface.

3.2.6 Pulse parameter metrics

The number of pulse parameter values for an experiment are equal to the number of pulses for that experiment. In the DoE parlance, it is a common practice to convert the observed values into a single metric or summary statistic for easy comparison [28]. Let us assume that there are N_p pulses in an experiment. Therefore, the outcome of an experiment (in terms of pulse parameter y) will be $N_p \times 1$ vector \mathbf{y} . Let the elements of vector \mathbf{y} be y_i . The following metrics are chosen in this case, which are also indicated in Fig. 3.6.

1. **Mean**: Then mean of the parameter y for an experiment is given by:

$$\text{mean}(y) = \frac{\sum y_i}{N_p} \quad (3.4)$$

2. **Signal to noise ratio (SNR)**: SNR for an experiment is given by the following ratio:

$$\text{SNR} = 10 \log_{10} \frac{[\text{mean}(y)]^2}{\text{var}(y)} \quad (3.5)$$

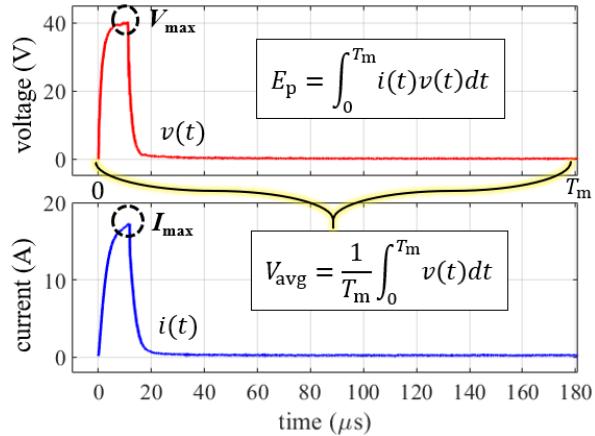


FIG. 3.6: Graphical definition of pulse parameters

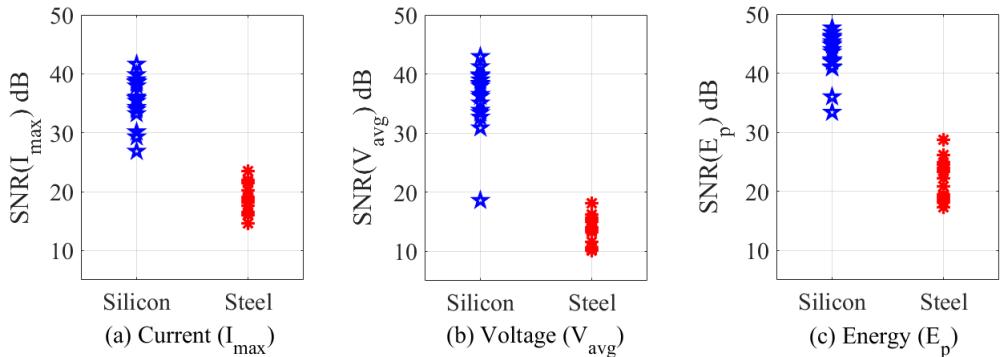


FIG. 3.7: SNR of pulse parameters for all 18 experiments in L18 array

where, $\text{var}(y)$ stands for the variance of the signal. The SNR indicates the level of uniformity across pulses for a pulse parameter y . More the value of $\text{SNR}(y)$, lesser will be the variation in y across pulses i.e. lesser is pulse to pulse variation. Here, it should be noted that the pulse-to-pulse variation is taken as the response as shown in Fig. 3.3 and the possible reasons for the same are discussed in the following sections.

3. **90th percentile:** Every experiment contains n pulses and corresponding n values of pulse parameters. When the parameter values are arranged in ascending order, there would be a value (or values) of the parameter, below which there would be 90% (in number) of all the data values. That value is the 90th percentile value for the pulse parameter. This metric or summary statistic is chosen to eliminate any outliers, especially in V_{\max} data.

SNR values for silicon and steel are compared in Fig. 3.7, where all the experiments corresponding to a material are plotted on a common abscissa. It shows that SNR values for silicon are higher by 20-30 dB than those for steel. Figs. 3.7(a) and 3.7(c) indicate that there is a significant difference in SNR of pulse parameters I_{\max} and E_p as well, for silicon and steel. This underlines that, although the pulse-to-pulse variation is clearly ‘seen’ in the voltage waveforms, it is also present in the current pulse-trains.

3.3 Results and Discussion

3.3.1 OFAT Experiments

3.3.1.1 Relation between factors and pulse parameters

Each factor has several levels available in the form of indices in BM400. From the observed data, the values in standard scientific units corresponding to indices are deciphered and they are given in Table 3.5. Here, the column ‘Range’ indicates the levels available for each factor.

3.3.1.2 Prima facie differences between spark-erosion of silicon and steel

Ideal spark voltage and spark current waveforms are shown in Fig. 3.8(a) for easy comparison with the recorded waveforms in Fig. 3.8(b), these are the pulses in Fig. 3.2, plotted over one another with an enlarged time scale. The three stages of operation, (1) pre-breakdown, (2) sparking, and (3) pause, are marked in Fig. 3.8(a). The following observations are made from Figs. 3.2 and 3.8.

1. From Figs. 3.8(a) and 3.8(b), the measured waveforms deviate significantly from the ideal waveforms. The pre-breakdown stage is visible only for some pulses in the case of steel as shown in Fig. 3.8(b). However, it is not seen for all 500+ pulses in the case of silicon. It could be due to two possible reasons:
 - (a) The pre-breakdown period is too short to be captured by the voltage probe.
 - (b) The pre-breakdown period does not exist for silicon due to difference in mechanism of spark-erosion.

TABLE 3.5: Values in standard units corresponding to indices or levels of factors

Parameter	Range of indices	Values in terms of SI units
V (voltage)	HV and LV	$HV \equiv 100 \text{ V}$ and $LV \equiv 75 \text{ V}$. Both refer to the open circuit voltage V_{OC} .
IP (peak current)	1-6	IP refers to the limit on the <i>peak current</i> . The actual peak values are <u>not</u> equal to 1-6 A, however they depend on the workpiece material and the level of voltage ‘V’. For example, in Fig. 3.2, for the same value of IP = 3, the $I_{sp}^{(St)} = 38 \text{ A}$ and $I_{sp}^{(Si)} = 25 \text{ A}$. Therefore, there is no single expression which relates the ‘IP’ with the current in Amperes.
PON (ON time)	10-30	This is the <i>pulse on time</i> (t_{on}) in μs .
POFF (Period of the pulse)	18-30	This factor is related to the period of the voltage pulse. With analysis of values of POFF, PON and the corresponding pulse period T_m , it is found that $T_m = (\text{POFF} - 1) \times t_{ON}$
WS (Wire Speed)	0-3	This is the speed of the wire in the direction of axis of the wire and not in the direction of wire-feed shown in Fig. 3.4. The wire speeds corresponding to the indices are calculated by measuring the rotational speed of wire-storage drum with tachometer. The correlation between the indices and the speeds is as follows: 0 \equiv 11 m/s, 1 \equiv 7.5 m/s, 2 \equiv 5 m/s, 3 \equiv 2.5 m/s

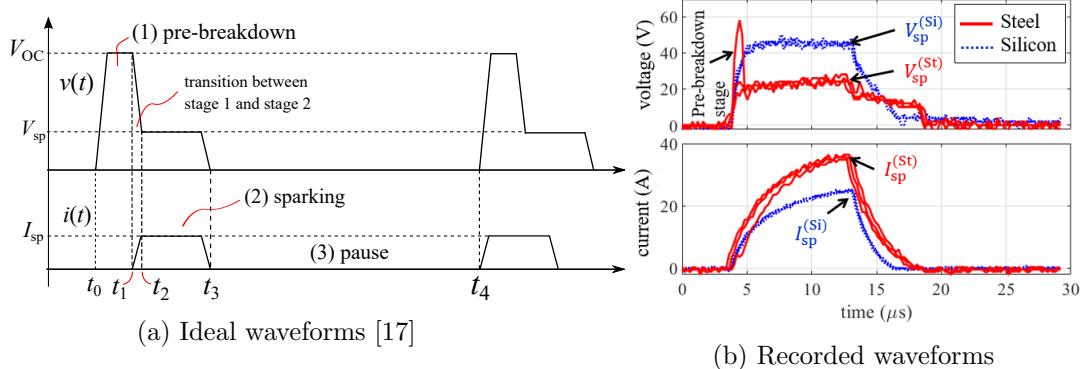


FIG. 3.8: Voltage and current pulses in WEDM

2. During the sparking stage, Fig. 3.8(a) shows that the spark current is constant for the ideal waveform, whereas in the recorded waveforms in Fig. 3.8(b), the current rises exponentially.
3. The sparking voltage magnitude for silicon is more than that for steel i.e. $V_{sp}^{(Si)} > V_{sp}^{(St)}$.

4. The sparking current for silicon is lesser than that for steel, i.e. $I_{sp}^{(Si)} < I_{sp}^{(St)}$, as indicated in the first current pulse in Fig. 3.2.
5. A close look at the pulses in Fig. 3.8(b) reveals that the pulse-to-pulse variation in voltage pulses for silicon is negligible. However, there is a considerable pulse-shape variation between the voltage pulses recorded for the steel. There is no pulse-to-pulse variation in the current waveforms for both materials.
6. It is found that for same set of parameter values, energy of the WEDM spark is the same. This indicates that the machine BM400 uses a pulse generator that is an iso-energy pulse generator [150].

3.3.1.3 Difference in current voltage characteristics (CVC)

Another important feature is observed, when current is plotted against voltage i.e. in current-voltage characteristics (CVC), as shown in six representative plots in Fig. 3.9(a). The CVC can also be viewed as a trajectory traversed in the C-V plane by WEDM sparks. The corresponding directions are indicated in Fig. 3.9(a) by arrows.

Four distinct stages can be observed in the CVCs for steel - marked by four segments in plot B in Fig. 3.9(a) : O-P1, P1-P2, P2-P3, P3-O. These CVCs are similar in shape to that of a thyristor as reported previously [66, 151]. As shown in Fig. 3.9(a) and 3.9(b), O-P1 and P1-P2 constitute pre-breakdown stage, P2-P3 represents the sparking stage, whereas P3-O represents decay of voltage and current, after the supply voltage pulse is removed.

For steel, due to some variation in the spark-erosion process, the CVCs for some pulses do not exhibit four distinct stages as indicated by plots D, E, F in Fig. 3.9(a). This type of pulse-to-pulse variation is not seen in CVC for silicon, where only three stages are evident in all the pulses. The stages are marked in plot 'B' (Fig. 3.9(a)) as: O-R1, R1-R2 and R2-O. Here, O-R1 represents the initial rise of voltage and current, R1-R2 represents the sparking stage, where voltage slightly decreases and current rises, R2-O represents decay in voltage and current. The pulse-to-pulse variation may be contributed to the local variations in steel which would be absent in silicon. It is also seen for this set of factors that $V_{sp}^{(Si)} = 48$ V and $V_{sp}^{(St)} = 26$ V.

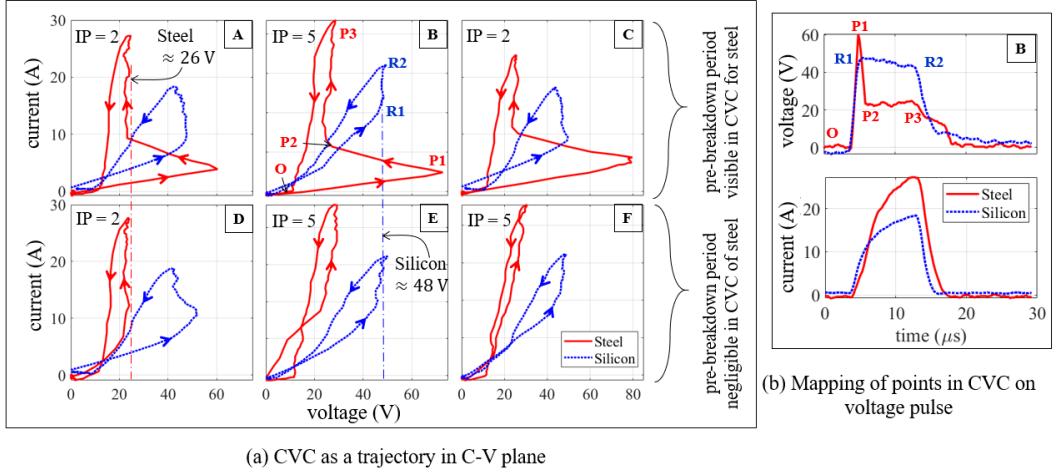


FIG. 3.9: Difference in patterns of CVC: $V = HV$, $PON = 10$, $POFF = 18$, $WS = 2$

Thus, OFAT experiments yielded information regarding relation of indices of factors with pulse parameters, the qualitative differences between spark-erosion of silicon and steel, as well as differences in CVCs of spark for silicon and steel. However, the information is not sufficient to make quantitative inferences regarding the effect of factors on the pulse parameters, as given in the next section, which gives a detailed account of the experiments done by robust design (Taguchi) method.

3.3.2 Experimentation by DoE Methods

Observing the pulse-train data in Fig. 3.5, the following observations can be made regarding the levels of voltage and current, which agree with the observations from the OFAT experimentation.

$$I_{sp}^{(St)} > I_{sp}^{(Si)} \quad \text{and} \quad V_{sp}^{(St)} < V_{sp}^{(Si)} \quad (3.6)$$

3.3.2.1 Effect of factors on pulse parameters

The following are the significant observations regarding the effect of factors on the pulse parameters.

1. Maximum value of current: Fig. 3.10 shows the main effects plot for ‘mean(I_{max})’.

Figs. 3.10(a) and 3.10(b) indicate that, I_{max} increases with increase in ‘V’ and ‘IP’. Figs. 3.10(c) through 3.10(e) do not show any particular trend of change in

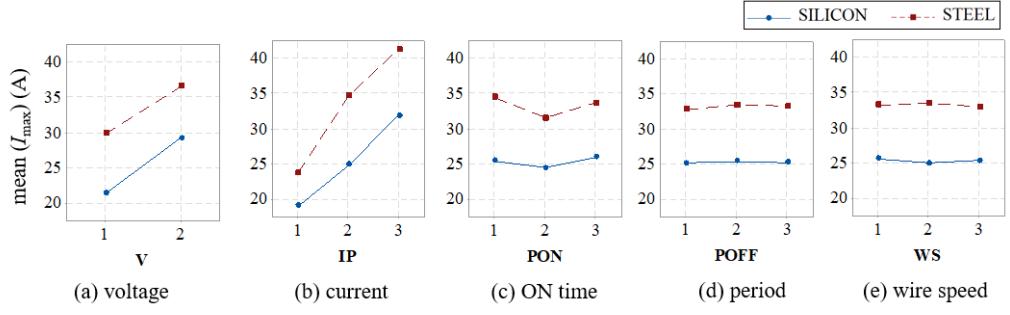


FIG. 3.10: Main effects plot for mean(I_{\max})

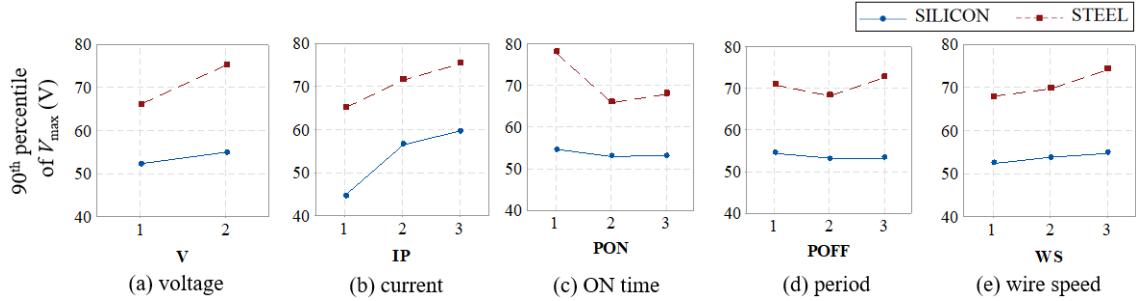


FIG. 3.11: Main effects plot for mean(V_{\max})

I_{\max} with PON, POFF and WS. It means that temporal factors do not affect I_{\max} significantly. In general, it is observed that current for steel is 10-15 A more than that for silicon.

2. Maximum value of voltage: The main effects plots for ‘90th percentile of V_{\max} ’ are shown in Fig. 3.11. It is observed that the maximum voltage for steel is 20-30 V more than that of silicon. This agrees with the observations made by Yang et al. [67]. Figs. 3.11(a), 3.11(b), and 3.11(e) indicate that, V_{\max} increases with V, IP and WS. However, Figs. 3.11(c) and 3.11(d) indicate that V_{\max} does not show any peculiar trend with PON and POFF. Thus, the temporal factors do not affect V_{\max} significantly.

3. Average voltage: V_{avg} is more for silicon than that for steel, as seen in Fig. 3.12. Figs. 3.12(a), 3.12(c), and 3.12(d) show that V_{avg} increases with an increase in ‘V’ and decreases with an increase in ‘PON’ and ‘POFF’. This is expected from eqn. (3.2), because when ‘PON’ and ‘POFF’ increase the denominator in (3.2) increases. However, the effect of IP on V_{avg} is not clear, as seen in Fig. 3.12(b).

The main effects plots for SNR of V_{avg} are shown in Fig. 3.13. SNR of V_{avg} in the case of silicon is 20 - 30 dB more than that in the case of steel. From (3.5),

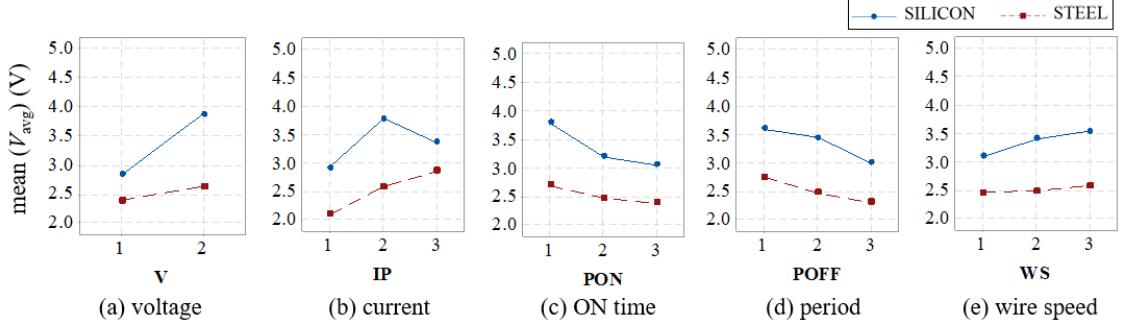


FIG. 3.12: Main effects plot for mean(V_{avg})

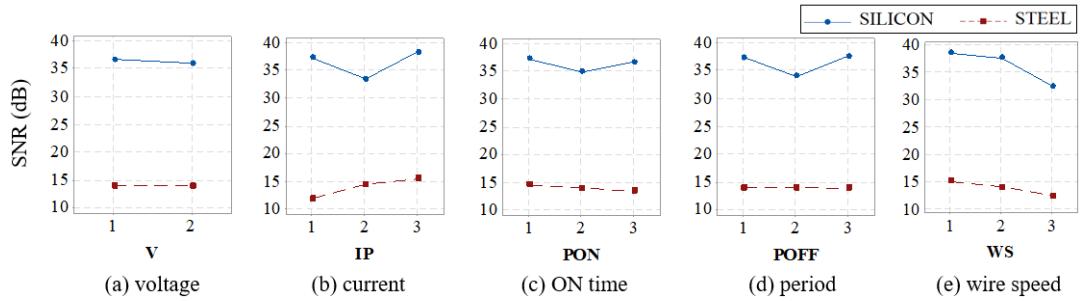


FIG. 3.13: SNR for mean(V_{avg})

this implies that the pulse to pulse variation in steel is 100 times more than that in silicon. Also, Figs. 3.13(a) to 3.13(d) show that there is no particular trend in SNR of V_{avg} with V, IP, PON and POFF. However, there is a slight decrement in $\text{SNR}(V_{avg})$ with an increase in WS index, i.e. a decrease in WS as seen in Fig. 3.13(e).

4. **Energy:** The main effects plots of mean(E_p) (see Fig. 3.14) show that the energy consumed for silicon is more than that for steel. Also, Figs. 3.14(a) and 3.14(b) illustrate that mean(E_p) increases with the increase in V and IP however, there is no particular trend observed in Figs. 3.14(c) to 3.14(e). Fig. 3.15 shows that the $\text{SNR}(E_p)$ of silicon (40-45 dB) is significantly more than that of steel (20-25 dB). Therefore, as far as energy consumed per pulse is concerned, there is almost 100 times more pulse-to-pulse variation in the case of steel than that for silicon. This implies that the material removal also varies from pulse to pulse for steel. There is no particular trend of $\text{SNR}(E_p)$ with IP, PON, and POFF as seen from Figs. 3.14(b), (c) and (d). However, SNR of E_p increases with an increase in V and a decrease in WS as seen in Figs. 3.14(a) and 3.14(e).

Fig. 3.15 shows that, for silicon, higher voltage, lower current, higher PON and higher wire speed are recommended for the least variation among pulses which

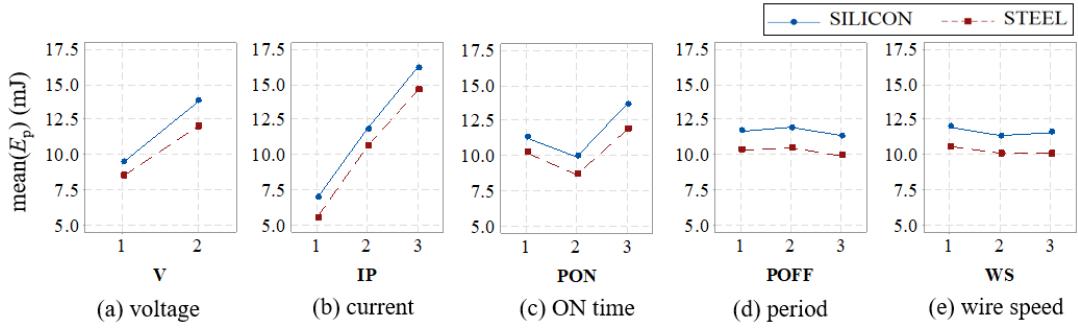


FIG. 3.14: Main effects plot mean(E_p)

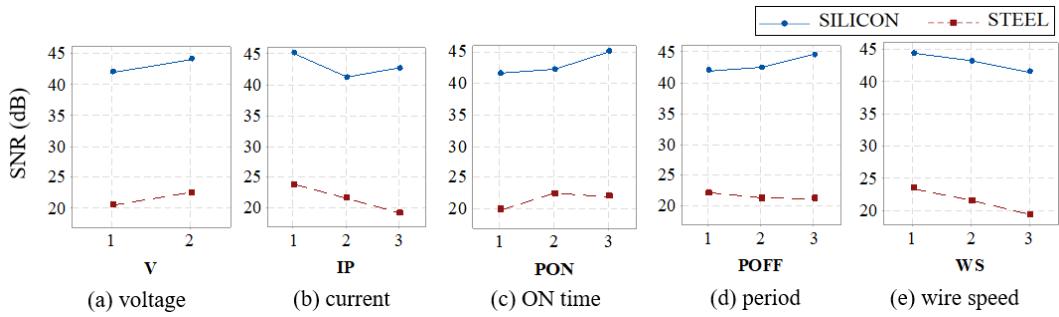


FIG. 3.15: Main effects plot for SNR for energy

leads to more consistent material removal. Puri et al. [149] have observed that the pulse energy is proportional to the force acting on the wire in WEDM. Therefore, more the pulse-to-pulse variation in energy, more will be the variation in the force on the wire, and hence more are the chances of vibration in wires. However, the exact nature of vibrations produced due to pulse-to-pulse variation in forces needs more investigation of wire vibrations which is out of scope of this work.

3.3.2.2 Analysis of Variance (ANOVA) of pulse parameters

Analysis of variance (ANOVA) is a technique to gauge the percentage effect of individual factors on the response or outcome of an experiment. In this technique, variation in the response due to a factor is found out by computing sum of squared deviation of response from the overall mean, considering the experiment involving that factor $SS_F|_A$. Deviation of response from mean is also computed considering effects of all the factors together. This is called total sum of squares SS_T . Percentage effect of a factor is computed as [28]

$$\% \text{effect of factor A} = \frac{SS_F|_A}{SS_T} \quad (3.7)$$

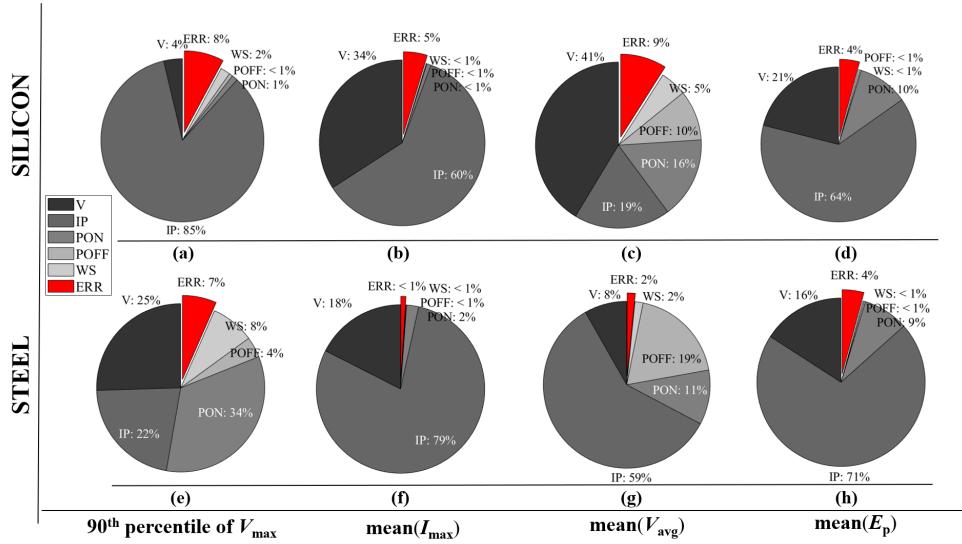


FIG. 3.16: ANOVA: % effect of factors on pulse parameters

This technique is also used to check null hypothesis, i.e. whether there is no variation due to different levels of a factor or the otherwise [28, 152]. Using this technique, the percentage effect pie charts are obtained and shown in Figs. 3.16 and 3.17. Here, *y*-axis denotes the material and *x*-axis indicates summary statistics of the pulse parameters. The percentage effect of each factor is obtained by dividing ‘sum of squares’ by ‘total sum of squares’ [28]. ERR % indicates the percentage error in predicting the factor effects in the additive model in the robust design method [28].

Percentage effect on mean and 90th percentile

The error percentage is very low in all the pie-charts, see Fig. 3.16. This confirms the fact that the model assumed in L18 OA is indeed valid for predicting the mean and the 90th percentile of pulse parameters. The effect of factors on individual parameter metrics are discussed below.

- 1. 90th percentile of V_{\max} :** Fig. 3.16(a) shows that, for silicon, IP affects V_{\max} the most, whereas the effect of other factors is not significant. For steel, V_{\max} is affected by settings of V (25%), IP (22%) and PON (34%), see Fig. 3.16(e). For steel, V_{\max} is mostly the pre-breakdown voltage, whereas for silicon, it is the voltage in the sparking stage (see Fig. 3.8). Therefore, the effect of factor ‘V’ on 90th percentile of V_{\max} is more for steel (25%) than that for silicon (4%).
- 2. Maximum current (I_{\max}):** Fig. 3.16(b) and 3.16(f) portray that the significant factors affecting I_{\max} are current (IP) and voltage (V), for both silicon and steel.

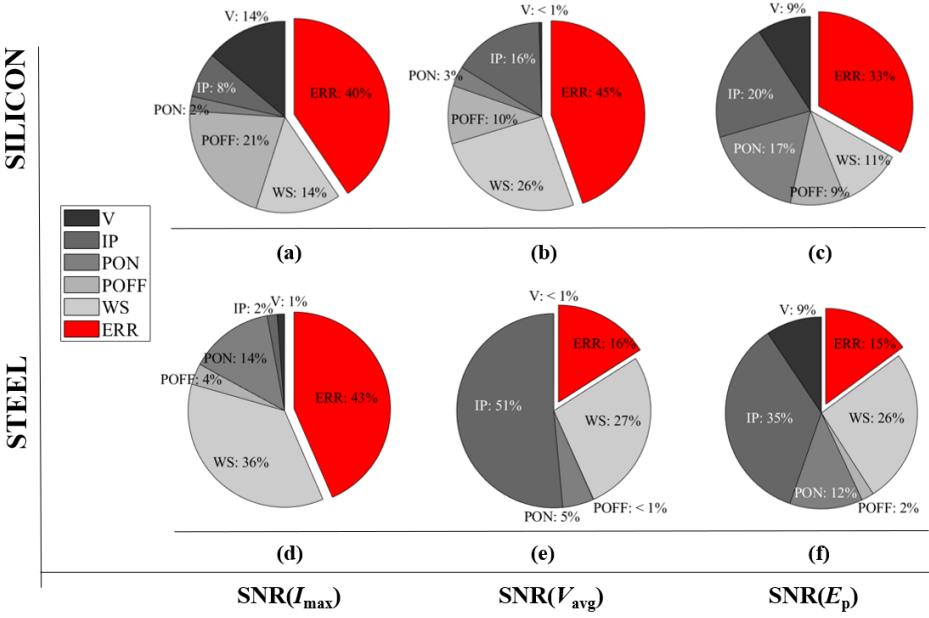


FIG. 3.17: ANOVA: % effect of factors on SNR of pulse parameters

The effect of other factors is insignificant. The role of IP on I_{\max} is as expected. However, it should be noted that the voltage setting also has a significant effect on peak current in the case of silicon (34%) as well as steel (18%). The difference in percentages is discussed in Section 3.4.

3. Average voltage (V_{avg}): The percentage effect of factors on mean(V_{avg}) is shown in Figs. 3.16(c) and 3.16(g) for silicon and steel, respectively. It is seen that V_{avg} depends on V, PON and POFF for both materials, which is expected from (3.2). The effect of IP on V_{avg} can be explained as follows. V_{avg} is indicative of the voltage in the sparking stage as seen from (3.2). After the spark formation, the dielectric breakdown is completed and hence there is no control over the spark voltage. However, the spark current is controlled by a current control algorithm as explained in Chapter 4. Consequently, the charge carriers and hence the voltage in the spark gap are determined by the current control strategy. Thus, the term V_{sp} in eqn. (3.2) is affected significantly by IP. Moreover, the effect of 'V' on V_{avg} is more significant for silicon (41%) as compared to that for steel (8%). This may be due to the MS junctions in spark-erosion of silicon.

4. Energy (E_p): V, IP and PON are the significant factors affecting mean(E_p) as seen in Figs. 3.16(d) and 3.16(h). This is expected from (3.3). It is also seen that IP plays a significant role in deciding E_p (64% for silicon and 71 % for steel).

Percentage effect on SNR values

Fig. 3.17 shows ANOVA of SNR values, i.e. pulse-to-pulse variation of the parameters. Here, the ERR percentage is larger ($\approx 30\text{-}40\%$) as compared to that in Fig. 3.16 ($< 10\%$). Although the percentage error is large, it is seen that the additive model still explains 60-70% of SNR values. However, the effect of factors on SNR values can be better explained if (a) the model with cross terms is considered, or (b) some additional factors are considered e.g. the value of servo voltage.

From all the subfigures in Fig. 3.17, it can be observed that wire speed WS is a prominent factor affecting the SNR values of pulse parameters. For example, WS affects $\text{SNR}(I_{\max})$ for steel (36%) more than that for silicon (14%), as seen in Figs. 3.17(a) and 3.17(d). Similarly, the effect of WS on $\text{SNR}(E_p)$ is more for steel (26%) than that for silicon (11%) as shown in Figs. 3.17(c) and 3.17(f). In the case of $\text{SNR}(V_{\text{avg}})$, the effect is almost the same for silicon (26%) and steel (27%). This shows that although wire speed does not appear in (3.3), it affects the pulse to pulse variation in energy significantly.

The effect of V on $\text{SNR}(I_{\max})$ is significant for silicon (14%) and not for steel (1%), see in Figs. 3.17(a) and 3.17(d). It is interesting that, the effect of 'V' on $\text{SNR}(V_{\text{avg}})$ is insignificant ($< 1\%$) for both silicon and steel as shown in Figs. 3.17(b) and 3.17(e), which means that the pulse-to-pulse variation in V_{avg} is not affected by the factors. As V_{avg} is used as a feedback variable to control the motion of electrodes, it can be deduced that the variation V_{avg} corresponds to variation in cutting speed. From the above observations, it can be deduced that the variation in the cutting speed is unaffected by the spark current settings in the case of an iso-energy pulse generator.

The effect of POFF on $\text{SNR}(I_{\max})$, $\text{SNR}(V_{\text{avg}})$ as well as $\text{SNR}(E_p)$ is much lesser for steel (4%, $< 1\%$ and 2%, see Figs. 3.17(d), 3.17(e), and 3.17(f), respectively) than that for silicon (21%, 10%, and 9%, see Figs. 3.17(a), 3.17(b), 3.17(c), respectively). Therefore, is clear that the OFF time and pulse period affect the variation in spark current, spark voltage and energy. This effect may be investigated further to see the underlying mechanism that is responsible. Figs. 3.17(c) and 3.17(f) also indicate that the error percentage for silicon is 33%, which is more than twice than that for steel (15%).

It should be noted that such quantification is not possible with OFAT or factorial type of experiments. Robust design methods enable experimenter to quantify the effects of factors and the particular factor to be investigated further.

3.3.2.3 Effect of Thickness of Workpiece

To study the effect of thickness (t_w) on the pulse-parameters and their metrics mentioned above, the results from set B are compared with that of set A (see Fig. 3.4). Figs. 3.18 and 3.19 show a distinct effect of thickness on the pulse parameter metrics for the two materials, which is discussed in the following subsections.

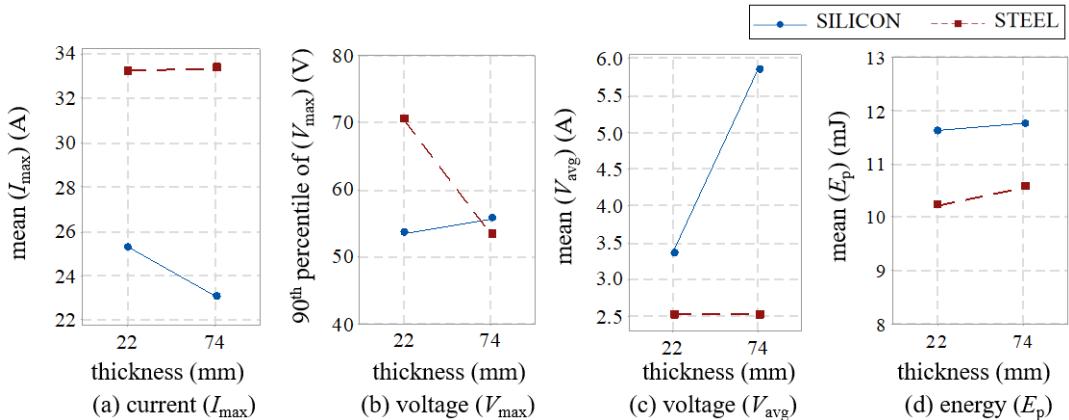


FIG. 3.18: Effect of workpiece thickness on pulse parameters

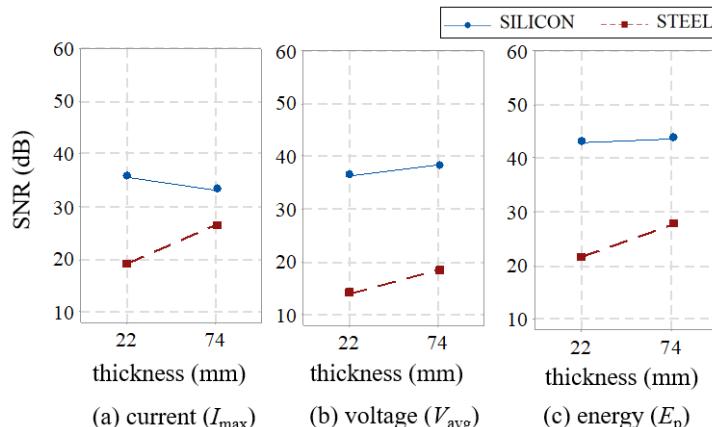


FIG. 3.19: Effect of workpiece thickness on pulse parameters

- Maximum current:** Fig. 3.18(a) shows that, $\text{mean}(I_{\max})$ decreases with an increase in t_w for silicon, whereas it remains almost unchanged for steel. Similar trend is also seen in Fig. 3.20, which shows ‘ $\text{mean}(I_{\max})$ ’ for all the experiments

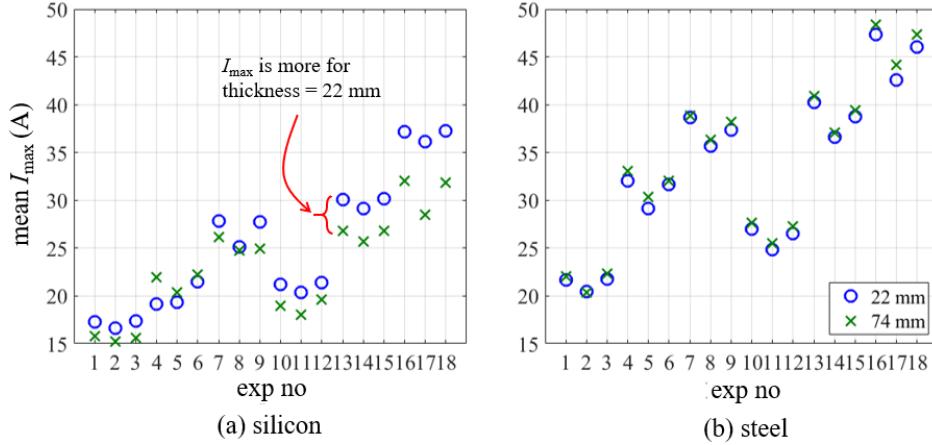


FIG. 3.20: Variation of mean(I_{\max}) with thickness of the workpiece

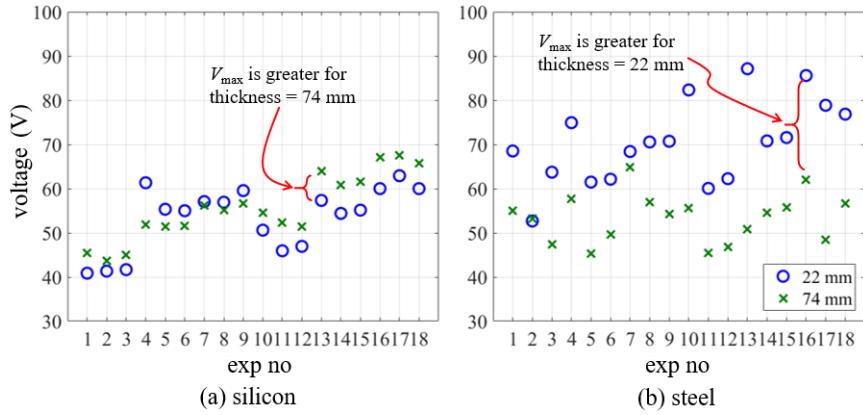


FIG. 3.21: Variation of 90th percentile of V_{\max} with thickness of the workpiece

for both silicon and steel. Fig. 3.20(a) portrays that, for silicon, the effect is more significant for experiments 10 to 18, for which $V = HV$ (see Table 3.4).

Pulse-to-pulse variation also exhibits different trends for silicon and steel as seen in Fig. 3.19(a). For steel, the SNR increases significantly with an increase in t_w . However for silicon, there is a slight decrease in SNR with an increase in t_w .

2. **Maximum Voltage:** Fig. 3.18(b) shows that, when t_w increases, V_{\max} increases slightly for silicon, and decreases for steel. Figs. 3.21(a) and 3.21(b) exhibit 90th percentile of V_{\max} in all the experiments for both silicon and steel. Fig. 3.21(a) shows that, the effect is more pronounced for experiments 10 to 18, for which $V = HV$. However for steel, the effect is seen in all the experiments, see Fig. 3.21(b).
3. **Average Voltage:** Fig. 3.18(c) shows that, when t_w increases V_{avg} increases for silicon, however it remains unchanged for steel. From Fig. 3.22(a), it is clear that for V_{avg} , the effect is visible for all the experiments unlike that in I_{\max} and

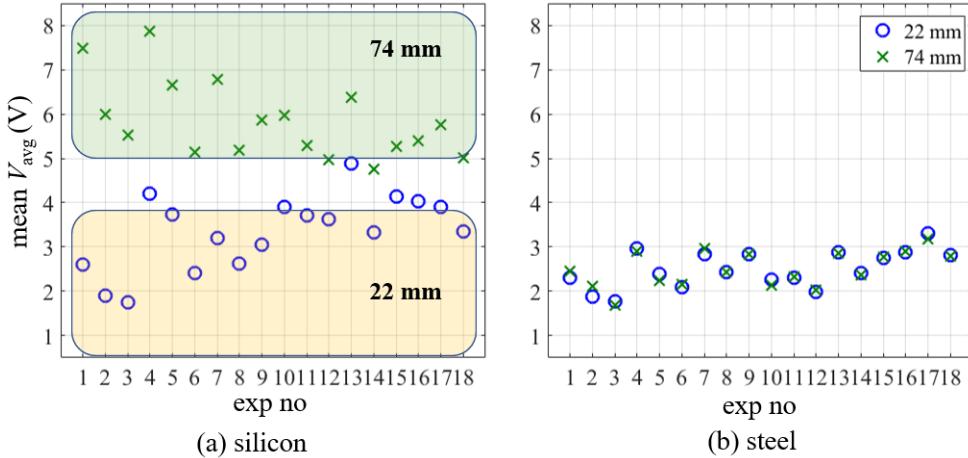


FIG. 3.22: Variation of V_{avg} with thickness of the workpiece

V_{max} , where the effect is significant only for experiments with $V=HV$. Fig. 3.22(b) illustrates that V_{avg} does not change with the workpiece thickness for steel.

There is a slight increase in $\text{SNR}(V_{\text{avg}})$ i.e. a slight decrease in pulse to pulse variation with an increase in t_w for both silicon and steel, see Fig. 3.19(b). Therefore, when the thickness of the workpiece increases, the pules-to-pulse variation in the spark voltage reduces.

Thus, the thickness t_w affects V_{max} , whereas it does not affect V_{avg} for steel. However, it affects both V_{max} and V_{avg} for silicon. V_{max} indicates pre-breakdown voltage for steel (see Fig. 3.8), whereas V_{avg} is indicative of the spark voltage. Thus it can be inferred that the spark voltage is unaffected by workpiece thickness for steel, with an iso-energy pulse generator. On the contrary, the voltage is affected by workpiece thickness for silicon (Figs. 3.18(c) and 3.22(a)).

4. **Energy:** Fig. 3.18(d) shows that there is no significant change in $\text{mean}(E_p)$ with a change in t_w for both silicon and steel. Further, Fig. 3.23 clearly indicates that E_p is constant for one set of parameters, confirming that BM400 indeed uses an iso-energy pulse generator. Fig. 3.19(c) shows that with an increase in t_w , the $\text{SNR}(E_p)$ increases in the case of steel, whereas it remains unchanged in the case of silicon. It means that when the workpiece thickness increases, the pulse-to-pulse variation in energy reduces for steel, whereas it remains almost unchanged for silicon.

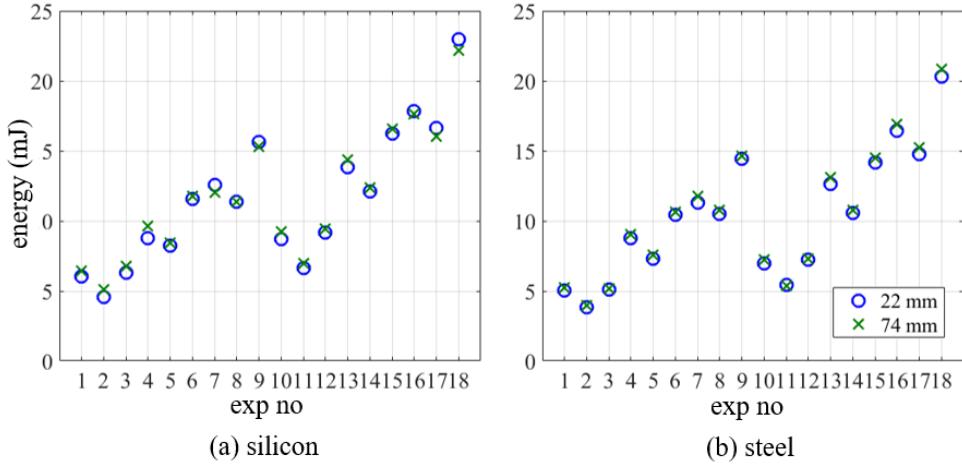


FIG. 3.23: Effect of cutting width on pulse energy

3.4 Inferences

From the observed trends in the change in electrical pulse parameters of WEDM of silicon, the following implications can be deduced for the equivalent circuit and design of WEDM for silicon.

3.4.1 Equivalent circuit of spark gap in WEDM of silicon

The analysis presented above helps us to infer the following points about the equivalent circuit as seen from the terminals of the pulse generator.

1. The ratio of currents is not equal to the ratio of the conductivities of the materials. Therefore, it can be hypothesized that in the post-breakdown representative circuit, the bulk conductivity is not an important parameter. This is because the ratio of experimentally measured conductivity (σ) given in Table 3.1 is:

$$\frac{\sigma_{\text{steel}}}{\sigma_{\text{silicon}}} = 1.41 \times 10^5 \quad (3.8)$$

Also, it can be derived from Fig. 3.10

$$\frac{I_{\max}^{(\text{St})}}{I_{\max}^{(\text{Si})}} \approx 1.5 \quad (3.9)$$

As stated earlier, there are two MS junctions in the spark-erosion process of silicon as shown in Fig. 3.24(a) and also noted in [49, 63, 153]. Therefore, the circuit

should contain non-linear elements like diode, as suggested by Mingbo et al. [69], see Fig. 3.24(b). It consists of two Schottky diodes: D_1 represents the MS junction between the workpiece and workbench, while D_2 represents the MS junction between the semiconductor-workpiece and the spark-plasma. Here, the plasma is considered similar to metals as it is full of charge carriers i.e. electrons and ions. D_c is a voltage regulator tube [69] (similar to a zener diode), which represents the the spark-discharge. The resistance R_w represents the lumped resistance of the workbench, workpiece, wire and the plasma channel.

2. When the gap breaks down, the current flows through the path $D_1-D_2-D_c-R_w$. It is clear that the diodes D_c and D_1 are reverse biased, i.e. the voltage across them is already above their respective breakdown voltages. Therefore, they do not play a significant role in deciding the magnitude of spark current. The MS junction of D_2 is in the forward conduction region. The forward current in a diode is dictated by the Shockley diode equation (3.10), where I_s is reverse saturation current, k is a constant which depends upon the material, T_K is the temperature in Kelvin and V_D is the voltage across the diode [154].

$$I = I_s \left(e^{\frac{kV_D}{T_K}} - 1 \right) \quad (3.10)$$

Here, the current rises exponentially and not linearly. Therefore, once the gap breaks down, the current would be dictated by V_D , T_K and the current control scheme used in the pulse generator [155]. Thus, the spark current is not directly proportional to the bulk electrical conductivity of the semiconductor workpiece. The current is decided by the forward biased MS junction between the semiconductor and the plasma.

3. Variation of pulse parameters with workpiece thickness confirms the role of semiconductor-plasma junction in the spark-erosion of silicon. This is because, when the thickness of the workpiece changes, the parameters of semiconductor-plasma junction also change. Therefore, it is expected that the voltage and current values for different thicknesses of the workpiece would be different for silicon, which indeed is observed in the results presented in section 3.3.2.3 (Figs. 3.18-3.22).
4. Based on the circuit shown in Fig. 3.24(b), a circuit which represents cutting of steel, is shown in Fig. 3.24(c). When the workpiece is metal, there is no difference

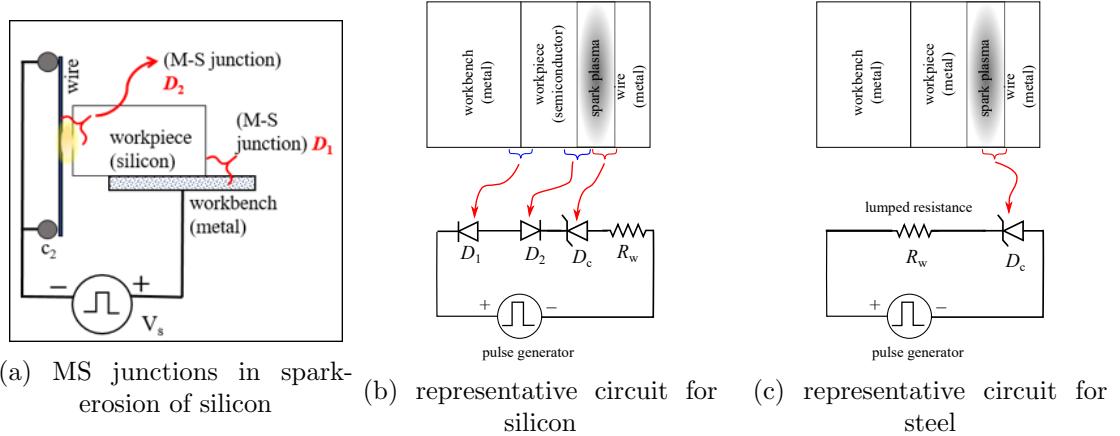


FIG. 3.24: Schematic and representative circuit for spark erosion of silicon and steel

in the work-functions of the workpiece and the workbench. Therefore, the diodes D_1 and D_2 are absent in this circuit. The zener diode D_c should be present which represents the spark-plasma in the circuit. After breakdown, the current for steel workpiece would be decided by the lumped resistor R_w only. The workpiece thickness does not affect the current and voltage values for steel as it is evident from Fig. 3.18. It is primarily decided by the current control schemes of the pulse generator [155].

5. Thus, the current in the case of silicon workpiece is mainly decided by the current control scheme and the Schockley diode eqn. (3.10). However, the amount of spark current in the case of steel workpiece is decided by the current control scheme in the pulse generator as well as the electrical conductivity.

3.4.2 Design of WEDM for silicon

Presently, off the shelf WED machines are used for experimentation on cutting of silicon. However, when WEDM is to be used as a technology for slicing of silicon ingots for the mass production of wafers, a dedicated WEDM is required for slicing of silicon or other semiconductor wafers too. The following are some inferences which should be considered while designing such machines.

1. As V_{max} is more for steel (see Fig. 3.11), the voltage required to initiate spark for silicon cutting is ‘not more’ than that for steel. Therefore, the pulse generator for a dedicated WEDM for silicon can be designed accordingly.

2. It is seen that the actual current (or the current ‘drawn’ by the spark) is increasing with an increase in workpiece thickness, in spite of same current settings (see Fig. 3.20), for silicon. From the last section, the reason behind this is the change in dimensions of spark-silicon junction (see D_2 in Fig. 3.24(a)). It might be necessary to ramp up the current setting when the thickness of the workpiece increases in the case of cylindrical ingots. Similarly, it might be necessary to decrease the voltage setting as the thickness of the ingot increases.
3. ANOVA of pulse parameter metrics has revealed that the SNR is affected by POFF (i.e. pulse period) and wire speed for both silicon and steel. Therefore, these parameters should also be included as important design considerations while designing new WED machines.
4. The pulse-to-pulse variation in steel is significantly higher than that in the case of silicon, see Figs. 3.7, 3.13 and 3.15. SNR for silicon is almost 20 dB higher than that for steel, which indicates that the pulse-to-pulse variation is 100 times higher in steel than that of in silicon. Thus, it is hypothesized that, it is possible to design a specialised pulse generator or CNC mechanism for WEDM of silicon than those designed for steel/other metals.

3.5 Conclusion

CVC based analysis of spark-erosion of silicon vis-à-vis steel is presented in this chapter. It is observed that the spark current is more whereas spark voltage is lesser in the case of steel irrespective of the input factors. Such a systematic study by using Taguchi design of experiments and recording voltage and current waveforms is presented for the first time.

It is also shown that the representative circuit as seen by the pulse generator cannot be a simple linear resistor. Instead, it should be a non-linear circuit consisting of two Schottky diodes because of existence of two M-S junctions. Earlier researchers [69] have used the circuit to explain the unidirectional conductivity seen in case of machining of silicon. Also, they have used the die-sinking EDM for their experiments, whereas wire EDM is used in this work. It is shown that the current required for machining does not

depend upon the resistivity. The nature of rise of current is qualitatively explained with the Shockley equation which governs the forward conduction of the diode.

Further, the effect of thickness of the workpiece on the voltage and current pulse parameters is also investigated by using workpieces of different thickness. It is seen that the trends of change in the pulse parameters are different for silicon and steel. This phenomenon confirms that the M-S junction between spark plasma and workpiece plays more important role than the junction between the workpiece and the workbench. This finding is particularly useful for slicing semiconductors because the ingots are usually cylindrical in shape and therefore, the thickness varies as the cutting progresses.

This chapter also underlines the limitations imposed by the presently available machines and pulse generators, especially while experimenting with non-metallic materials like silicon. Some of them are as follows:

1. Variation of input factors beyond the settings provided by manufacturer is not possible. For example, one cannot infer what happens with a voltage level different from the levels ‘HV’ and ‘LV’ provided the manufacturer.
2. Even if the current is set at the same level for two materials, the current drawn by the two materials is different. This behavior cannot be explained unless the algorithm used for current control is exactly known.
3. This machine does not provide a facility to adjust the servo voltage, which is the feedback variable commonly used in CNC control [156]. Such problem might arise with many commercial machines. This might be a reason for the large percentage of error obtained in ANOVA.
4. The discussion in this chapter is limited to the factors available on ‘control panel’ of the WEDM. However, there are other factors like wire material, diameter of wire, dielectric material, which should also be experimented with, in order to optimize the process for silicon. Such experimentation with readily available machine may lead to malfunctioning of the machine.

Therefore, major portion of the work in this thesis is regarding making a dedicated customizable miniature WEDM machine. Next chapter discusses the study regarding pulse generators as well as design and control of a particular topology of pulse generators.

Chapter 4

Classification and Comparative Study of EDM Pulse Generators

This chapter presents an exhaustive classification and comparative study of the latest pulse generators for EDM. This is a detailed review and study done from power electronics perspective, which is not found in the literature till date. This study would be helpful for engineers who wish to design EPG for a particular application. This study can also be used to design newer topologies for specific application like slicing of semiconductor ingots in this case.

4.1 Background

EPGs are at the core of any EDM or WEDM system as already seen in Chapter 1 (Fig. 1.7). They are used to apply the spark initiation voltage of the order of $\approx 100\text{-}400$ V across the gap at a repetition frequency ranging from several kHz to few MHz [23]. If the voltage is applied for a duration more than few 10s of μs , the spark may develop into a sustained arc [26]. Hence, a pulsed voltage with a finite ON time (t_{ON}) and a finite OFF time (t_{OFF}) is necessary for the very functionality of the process. However, systematic study of EPGs from power-electronics perspective is found in very few articles [45, 157]. The following points underline the necessity of such study:

- (a) Although EPG topologies are derived from some standard DC-DC or DC-AC converters, their operation is significantly different. This is because, the nature of load

is such that, it requires control of both spark initiation voltage and the spark current *within one pulse period* [23].

(b) The output pulses contain two dominant frequencies: the pulse repetition frequency and the switching frequency used in voltage and current control. Besides the conventional voltage and current control, EPGs can also employ control of other pulse parameters like control of rate of rise of current (RRC) [79] to achieve certain machining objectives. Such aspects are not covered in the literature till date.

(c) Efficiency of the EPGs is important particularly from the viewpoint of sustainable manufacturing [158]. Li et al. have proposed empirical formulations to compute energy efficiency of the EDM process [159]. They have given specific energy consumption (kJ/mm^3) as a function of MRR. Recently, Zheng et al. stated that the EPGs consume a considerable amount ($\approx 17\%$) of power in the complete EDM system [160]. They have also given an empirical formulation to compute energy consumed as a function of MRR and other process parameters. In the domain of power electronics, however, there is a very little discussion of efficiency computation of EPGs [45], [96].

(d) The typical ratings of EPGs are several orders of magnitude different from those of the conventional pulsed power systems. The difference in typical ratings is as follows: power (several GW vs several hundred W), voltage (several kV vs several 100s V) and current (several kA to several A) [23, 161–163]. They are also distinct from the conventional high voltage pulse generators [164].

Sen et al.[45] have given an overview of EPGs from historical perspective. However, many topologies mentioned in [45] (like thyristorized pulse generator) are seldom used today. Using the available literature, it is difficult for a design engineer to understand and select a pulse generator for some specific objectives and constraints.

Therefore, this chapter¹ presents classification and comparative study from efficiency and control perspective of EPGs for the first time considering 13 important topologies. To understand the uniqueness of EPGs, the pulsed nature of EDM load and structure of EPGs are discussed in next section. Categorization of EPGs is presented considering

¹The study in this chapter is published as:

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their structure and control strategy, in Section 4.3. Operating principle of each topology is explained at length and it is aided by simulation results obtained using MATLAB Simulink. Section 4.5 describes variety of control schemes, besides the conventional voltage and current control schemes, which are specially used for the EDM load. The section also discusses the effect of these schemes on the machining parameters. Section 4.4 gives a generic methodology to compute the efficiency of EPGs along with an example. Section 4.6 presents a comparative study of component count of the topologies. This section also illustrates how the pulsed nature of the spark-load needs to be considered while sizing passive components in EPGs. Section 4.7 is dedicated to the overall comparison of topologies for various characteristics such as efficiency, complexity of feedback control system and component count.

4.2 Structure of EDM Load and EPGs

It is important to understand the nature of EDM load and generic structure of EPGs before studying them in detail. The two are discussed in detail in the following subsections.

4.2.1 Circuit representation of EDM load

Some researchers have tried to simulate the spark behavior with a circuit model consisting of spark resistance R_{sp} , inductance L_{sp} and capacitance C_{sp} [165, 166]. In those models, the spark resistance R_{sp} is a non-linear function of the spark current, time, dielectric material, materials of the electrodes, geometry, etc. [167, 168]. Consequently, the spark voltage is governed by non-linear differential equations. However, those models have considered discharges in *air*, not in water, and for electrode geometries different from that of EDM. As far as the sparks in EDM are concerned, there is no conclusive literature in this domain [23, 169]. Also, as geometries are different in DEDM and WEDM, there would be two distinct circuit models for DEDM and for WEDM. The parameters of the non-linear model consisting of diodes described in Section 3.4 makes the design of pulse generator quite complex.

Parameter	Value
f_m	1 kHz
D_m	20%
R_{sp}	1 Ω
I_{ref}	10 A
V_{ref}	100 V

FIG. 4.1: EDM load: symbol, equivalent circuit and parameters used in this work

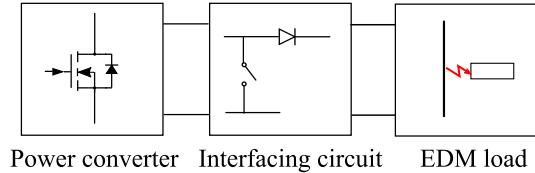


FIG. 4.2: Generic structure of EDM pulse generator

Researchers in the power electronics domain have mainly used a resistance and a switch to represent the EDM load [83, 90, 95]. Similarly, in this work, the EDM load is considered as a constant resistance in series with a switch. Fig. 4.1 shows the “symbol”, the “equivalent circuit” and the parameter-specifications used for the EDM-load in this work.

4.2.2 Structure of EPG

Generic structure of EPG is shown in Fig. 4.2. It has the following parts: (a) *power converter unit* which consists of DC-DC converter(s), usually modified to suit the EDM load, (b) *interfacing circuit* which facilitates the pause-time by connecting or disconnecting the converter unit with the EDM load. One of the characteristic features of EPGs is that there are two switching frequencies in the circuit: PE switches in the interfacing circuit are switched at frequency f_m , whereas those in the power converter unit at f_{sw} , such that $f_{sw} \gg f_m$. Also, usually the duty ratio of PE switches in the interfacing circuit is decided by the EDM operator and there is no explicit feedback loop for the same. However, duty ratio for PE switches in the power converter unit is decided by the EPG voltage and current control block, as shown in Fig. 1.7.

4.3 Classification of Pulse Generators

Classical literature on EDM [17, 23, 24] mentions only two types of EPGs viz., RC pulse generators and transistorized pulse generators, as they are discussed from production engineering perspective. However, from power electronics perspective, the EPG topologies can be classified into the following three types:

1. **Single converter based:** In this type, there is a single converter which acts as a voltage source (VS) during the pre-breakdown stage and a current source (CS) during the sparking stage. As only a single converter is present, the spark-initiation voltage is decided by the input voltage of the DC link itself or it can be controlled by resistive elements. There is no separate voltage control loop in this converter.
2. **Dual converter based:** In these topologies, two converters are connected across the EDM load, and hence they are called dual converter based topologies. One converter serves as a VS to provide spark-initiation voltage and the other converter serves as a CS to provide the necessary sparking current. Due to the presence of two separate converters, both v_o and i_o can be controlled with a single topology.
3. **Resonant converter based:** These topologies use a resonant converter as the basic unit. The output voltage and hence the current is decided by the operating frequency of the converter.

Important topologies of each type are described in the following subsections. The topologies are labeled as T1, T2, T3, \dots , etc. for easy referencing. Here, EPGs are treated as “DC to pulsed DC” converters and hence, the circuit to convert AC mains to DC link is not considered in this study. Current paths for the three stages of operation are marked in the circuits as well as summarized in Tables 4.1 and 4.2.

4.3.1 Single-converter based pulse generators

Operation of eight important topologies (T1 to T8) is discussed in this subsection. Out of those, topologies T1-T5 do not have explicit interfacing circuit whereas topologies T6-T8 have explicit interfacing circuit.

TABLE 4.1: Current paths for single converter based topologies

Topology	Sparking	Pause
T1 (Fig. 4.3(a))	V_{in} - R -gap	V_{in} - R - C
T2 (Fig. 4.4)	V_{in} - R -gap- Q	No current flows
T3 (Fig. 4.5)	Several parallel paths V_{in} - R_{lim} - Q_1 -gap V_{in} - R_{lim} - Q_2 -gap ... V_{in} - R_{lim} - Q_n -gap	No current flows
T4 (Fig. 4.7(a))	V_{in} - Q - L_1 -gap OR L_1 -gap- D_1	L_2 - D_2 - V_{in}
T5 (Fig. 4.8(a))	V_{in} - Q_1 -gap- L - D_3 - Q_2 AND D_1 -gap- L - D_3 - D_2	gap- L - R_1
T5a (Fig. 4.9(a))	Positive polarity: V_{in1} - Q_1 -gap- L - D_3 - Q_2 AND D_1 -gap- L - D_3 - D_2 - V_{in} Negative polarity: V_{in2} - Q_3 - D_4 - R_2 - L -gap	gap- L - R_1
T6 (Fig. 4.10(a))	V_{in} - Q_1 - L - Q_2 - D_4 -gap	D_4 -gap- V_2 - D_3 AND D_1 - L - D_2 - V_{in}
T7 (Fig. 4.11(a))	Positive polarity V_{in} - Q_1 - L_1 - Q_2 -gap- Q_3 gap- Q_4 - D_2 - V_{in} - Q_5 Negative polarity V_{in} - Q_1 - L_1 - Q_4 -gap- Q_5 gap- Q_2 - D_2 - V_{in} - Q_3	Positive polarity L_1 - D_2 - Q_1 Negative polarity L_1 - D_2 - Q_1

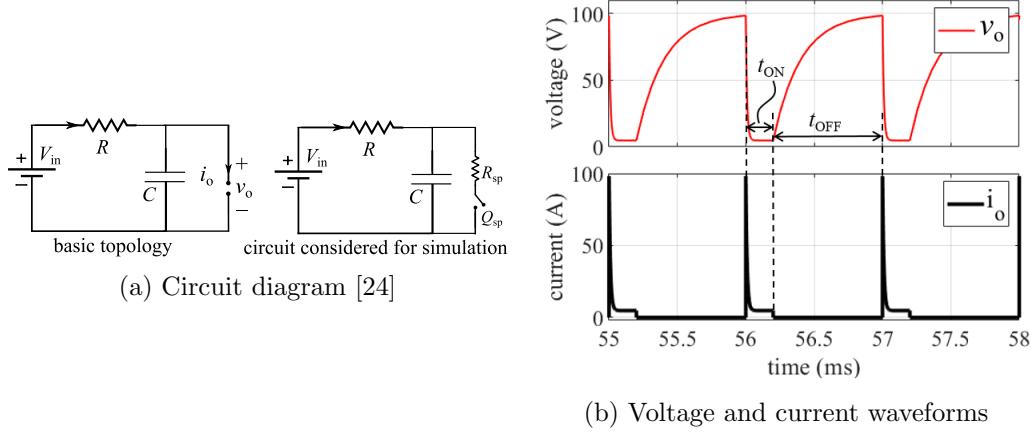


FIG. 4.3: T1: RC pulse generator

4.3.1.1 RC pulse generators

These are the earliest pulse generators consisting of a simple RC oscillator, as shown in Fig. 4.3(a) [17]. The voltage V_{in} has to be greater than the breakdown voltage V_b of the gap. When the capacitor voltage exceeds V_b , a spark is struck and the spark current i_o is supplied by both V_{in} and the capacitor. It can be seen that, as no active switching

element is used, the voltage and current waveforms are governed by the choice of circuit elements R and C . For example, the differential equation governing capacitor voltage after breakdown is given as (4.1)

$$v_o = \frac{-1}{R_{eq}C} v_o + \frac{1}{RC} V_{in} \quad (4.1)$$

where, $R_{eq} = \frac{RR_{sp}}{R+R_{sp}}$, R_{sp} is the spark resistance. Therefore, when the capacitor discharges i.e. during t_{ON} , the time constant is given by $R_{eq}C$. Usually, R is also used as current limiting resistor apart from deciding values of f_m and D_m , therefore $R \gg R_{sp} \Rightarrow R_{eq} \approx R_{sp}$. During t_{OFF} the capacitor charges and the time constant is given by RC . It is considered that it takes 5 time constants to reach the final value [170]. From the load specifications given in Fig. 4.1, $R = 20 \Omega$ and $C = 10 \mu F$ are chosen and simulation results are given in Fig. 4.3(b).

4.3.1.2 Transistorized pulse generators

Fig. 4.4 shows transistorized pulse generators which has a PE switch in order to control f_m and D_m [17, 24, 45]. When the switch Q is turned ON, the current flows to the load. When Q is turned OFF, the pause stage is initiated. The simulation output waveform is shown in Fig. 4.4(b). Load specifications given in Fig. 4.1 are used for the simulation.

Single transistor topology T2 cannot source the required current when the load demands more current. This may happen due to several reasons such as (a) MRR needs to be increased, (b) the combination of materials of the tool, the workpiece and the dielectric, is such that it requires more current to achieve same set of MRR, SR, and TEWR, (c) mode of operation changes from smooth cutting to rough cutting. In such scenario, it might be required to connect multiple transistors in parallel. Such topology is shown in Fig. 4.5 where n pairs of resistor (R_{lim}) and PE switch (Q_1, Q_2, \dots, Q_n) are connected in parallel [17, 45, 47]. Simulation output waveform is shown in Fig. 4.5(b), where 3 PE switches are used in parallel. Here, it is assumed that R_{sp} is reduced to $R_{sp}/3$ so that load current i_o increases. It should be noted that the load voltage v_o is the same in Figs. 4.4(b) and 4.5(b), whereas load current in 4.5(b) is thrice the load current in Fig. 4.4(b). However, in actual scenario, the increased demand of spark current may not be related to a proportional decrease in R_{sp} .

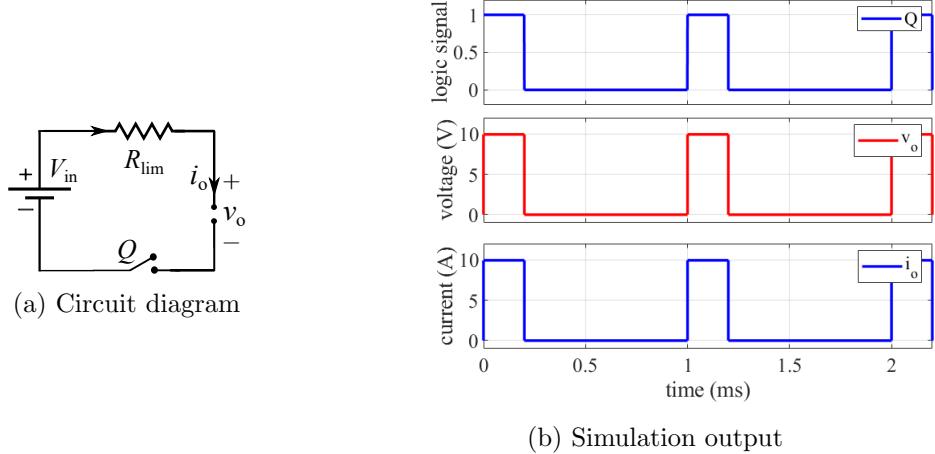


FIG. 4.4: **T2**: Transistorized pulse generators with single switch [17, 24]

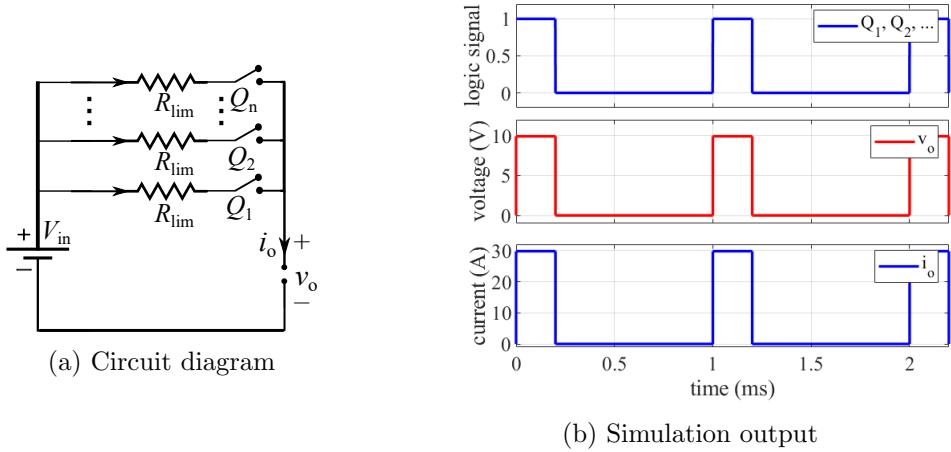


FIG. 4.5: **T3**: Transistorized pulse generator with multiple switches [17, 24]

4.3.1.3 Interleaved buck converter with energy recovery scheme

Lin et al. [82, 83] have proposed a buck-converter based topology with energy recovery scheme. When the conventional buck converter modified as a current source is used, it can lead to overvoltage across the gap as explained below. Fig. 4.6(a) shows a buck converter modified as a current source during the sparking stage. During this stage i_L is controlled by current mode control. When the pause stage begins, Q is turned OFF and the gap is non-conducting. The energy stored in L has to go to the parasitic capacitance C_{gap} between the two electrodes as shown in Fig. 4.6(b). The current flows through the loop $L-C_{\text{gap}}-D$. Lin et al. [83] have shown that the voltage at the output, just after the end of the sparking stage is given by (4.2):

$$v_o(t) = [-V_d - v_o(0)] \left(1 - \cos \frac{t}{\sqrt{LC_{\text{gap}}}} \right) + \frac{Li_L(0)}{\sqrt{LC_{\text{gap}}}} \sin \left(\frac{t}{\sqrt{LC_{\text{gap}}}} \right) + v_o(0) \quad (4.2)$$

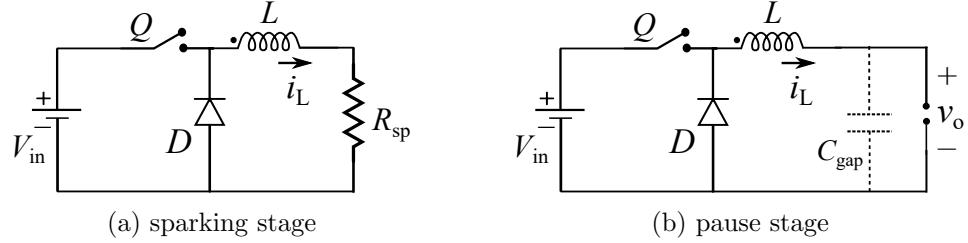


FIG. 4.6: Conventional buck converter modified as current source [82, 83]

Using typical values [26, 83], $V_d = 1$ V, $v_o(0) = 10$ V, $i_L(0) = 10$ A, $C_{\text{gap}} = 256$ nF, and $L = 150 \mu\text{H}$ we get $v_o(\text{max}) = 241$ V. Here, V_d is the voltage drop across the diode. Such high values of v_o can lead to unintentional sparking during the pause stage. Here, it should be noted that C_{gap} is the gap capacitance computed by $\frac{\epsilon A}{d}$, where A is the area of the electrodes and d is the separation between the workpiece and the tool electrodes. It should be noted that, the formula is valid only for DEDM and for WEDM, a different formula must be used. Considering water as dielectric $\epsilon_r = 80$, circular electrode of diameter 10 cm and $d = 110 \mu\text{m}$, the capacitance can be computed as ≈ 256 nF. For the value of $C = 4.7$ nF, as given in [83], the transient voltage can be computed to be as high as 56 kV. L is computed considering the output ripple to be within 1.5 A.

This can be alleviated with the Energy Recovery Scheme (ERS) which consists of D_2 and a coupled inductor L_2 as shown in Fig. 4.7(a). The inductors L_1 , L_2 (which form an isolated transformer) in Fig. 4.7(a) can be replaced with a center-tapped transformer as well [82]. Current paths for the two stages of operation are clearly indicated in Fig. 4.7(a). This topology is simulated in MATLAB simulink for $V_{\text{in}} = 100$ V, $L_1 = 150 \mu\text{H}$, and $L_2 = 753 \mu\text{H}$ and the results are shown in Fig. 4.7(b). While only single buck converter is shown in Fig. 4.7(a), the proposed topology in [82, 83] has four interleaved converters to reduce the effective current ripple to $\Delta i/4$, where Δi is the current ripple at the output of single converter.

4.3.1.4 H-bridge like converter

This topology is patented by Okane et al. [80] and is depicted in Fig. 4.8(a) along with the current paths for the stages of operation (described in Table 4.1). It is a modification of a standard H-bridge like converter, except that it has no explicit energy storage elements. The inductor L is a parasitic inductance of the EDM setup. During the pause stage, the current through the gap flows through the resistor R_1 which limits

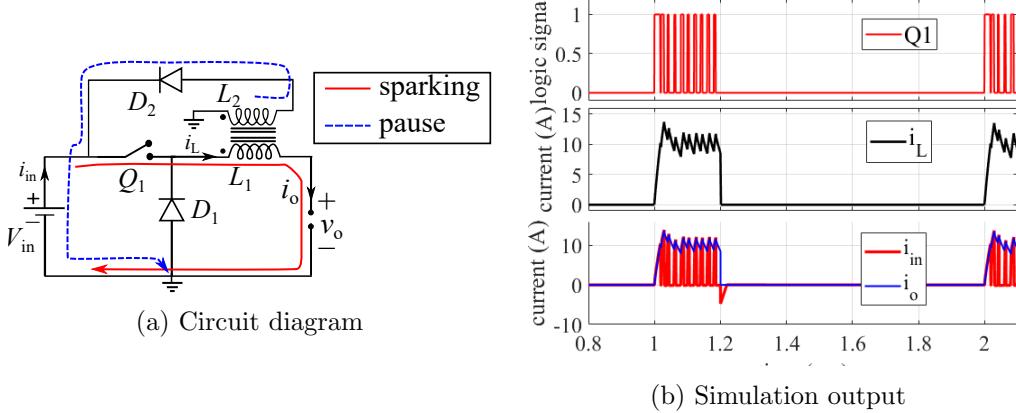


FIG. 4.7: T4: Isolated buck converter with energy recovery scheme [83]

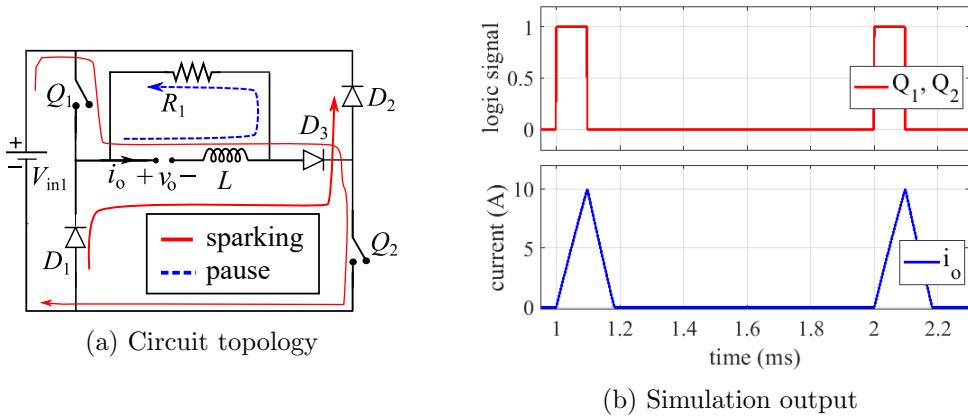


FIG. 4.8: T5: H-bridge like converter [80]

the current. It also provides a discharge-path for any charge accumulated across the stray capacitance between the electrodes.

This topology is simulated in MATLAB Simulink for $V_{in} = 100$ V, $R_1 = 5$ k Ω and the waveforms for triggering signals of switches and output current are shown in Fig. 4.8(b). Contrary to Fig. 4.7(b), it can be seen that the current waveform is triangular, because peak current control is used in place of current programmed control [171].

Topology T5 can be modified with an additional circuit to provide reverse polarity pulses as shown Fig. 4.9 [80]. R_2 is a large value resistor added in this path to avoid erosion of the tool electrode. Fig. 4.9(a) shows the current path for reverse polarity only to avoid cluttering. The current paths for positive polarity are same as those in Fig. 4.8(a). The simulation output is shown in Fig. 4.9(b). It should be noted that the fall time of current is different during the positive and negative cycle due to the change in time-constant of

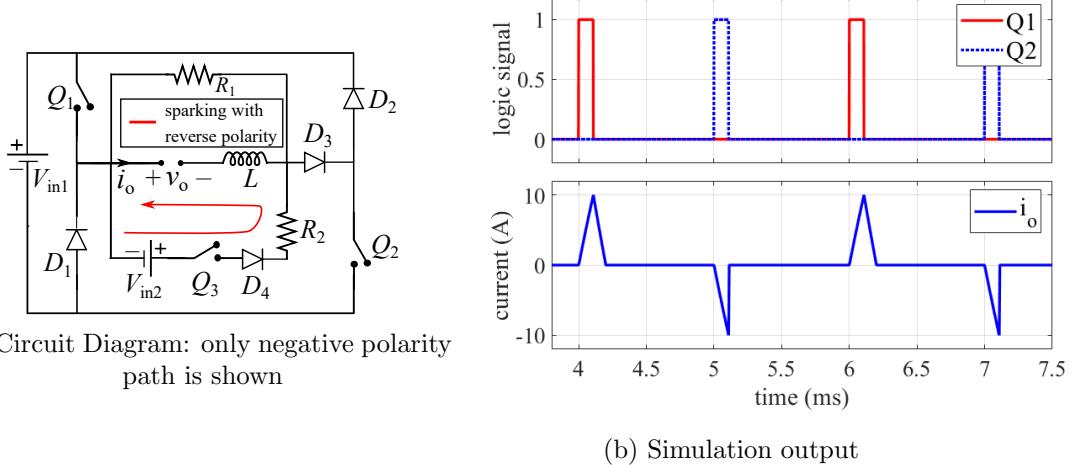


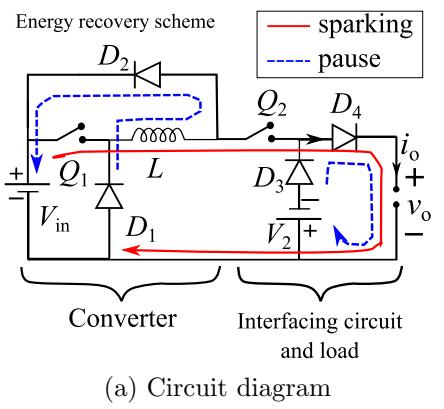
FIG. 4.9: **T5-a:** H-bridge like converter with an additional circuit to provide reverse polarity pulses [80]

the circuits. A similar topology is also proposed by Jeong et al. [172] as a high power (10 kW) EPG.

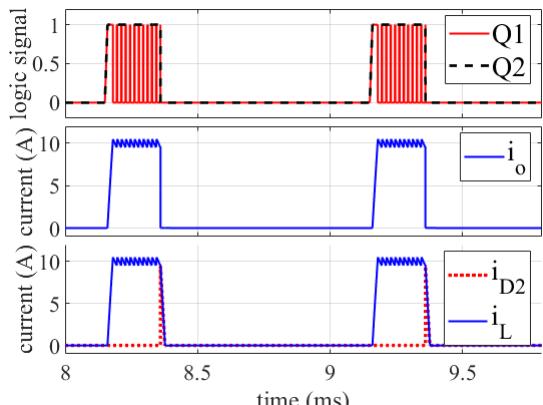
4.3.1.5 EPG with interfacing circuit

Contrary to the topologies T1 through T5, the topologies T6, T7 and T8 (Figs. 4.10(a), 4.11(a) and 4.12) presented in this section have an explicit interfacing circuit. Topology T6 (Fig. 4.10(a)) has the converter similar to topology T4 (Fig. 4.7(a)) and an interfacing circuit which consists of Q_2 , D_4 , D_3 and V_2 . Polarity of V_2 is opposite to that of v_o to assist recombination of charges during the pause stage. Simulation results of topology T6 are shown (for $V_{in} = 110$ V, $L = 2 \mu\text{H}$ and $V_2 = 10$ V) in Fig. 4.10(b). When Q_2 is switched ON, the voltage V_{in} gets connected across the gap and spark current flows. Then, Q_2 is kept ON, whereas switching of Q_1 is dictated by hysteresis current control. Hence, the switching frequencies of Q_1 and Q_2 are clearly different from each other. Q_2 is turned OFF to initiate the pause stage, when the inductor current completes its path through D_2 , whereas the load current decays to zero through V_2-D_3 . As the EDM load considered for the simulation is only resistive with no inductive elements, the current i_o in Fig. 4.10(b) reduces to zero at once. Current paths for various stages of operation can be referred from Table 4.1.

In topology T7, the interfacing circuit is an H-bridge circuit which facilitates bipolar voltage pulses at the output. However, Fig. 4.11(a) shows the current paths for positive polarity pulses only. The paths for the reverse polarity pulses are given in Table 4.1.

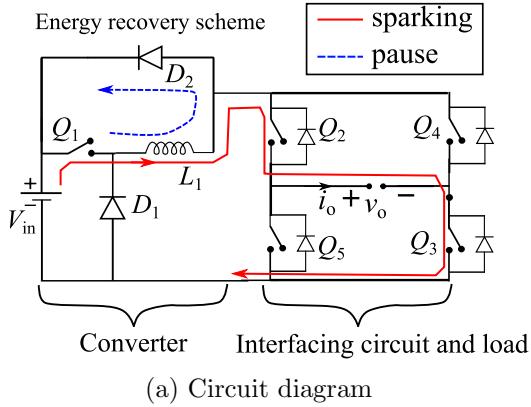


(a) Circuit diagram

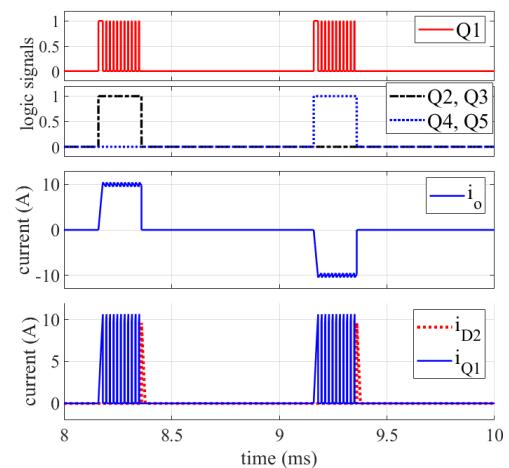


(b) Simulation output

FIG. 4.10: T6: EPG with unipolar interfacing circuit [78]



(a) Circuit diagram



(b) Simulation output

FIG. 4.11: T7: EPG with bipolar interfacing circuit [78]

Simulation output for topology T7 is shown in Fig. 4.11(b). It can be seen that, although the component count is increased, the switching frequency for Q_2 through Q_5 is half f_m . Therefore, the switching losses would be lesser in each switch. For both T6 and T7, hysteresis current control is proposed [78], by using the current through inductor (L or L_1) as the feedback signal. A third topology in this category is proposed by Yang et al. [96], as shown in Fig. 4.12(a). Here, the component count is reduced because, the interfacing circuit consists of a single switch Q_3 and ERS consists of only a diode. Current paths for various stages of operation are shown in Fig. 4.12. The novelty of this topology lies in adaptive voltage positioning (AVP) control, which is discussed in Section 4.5.2. The simulation output waveform with simple current control is shown in Fig. 4.12(b).

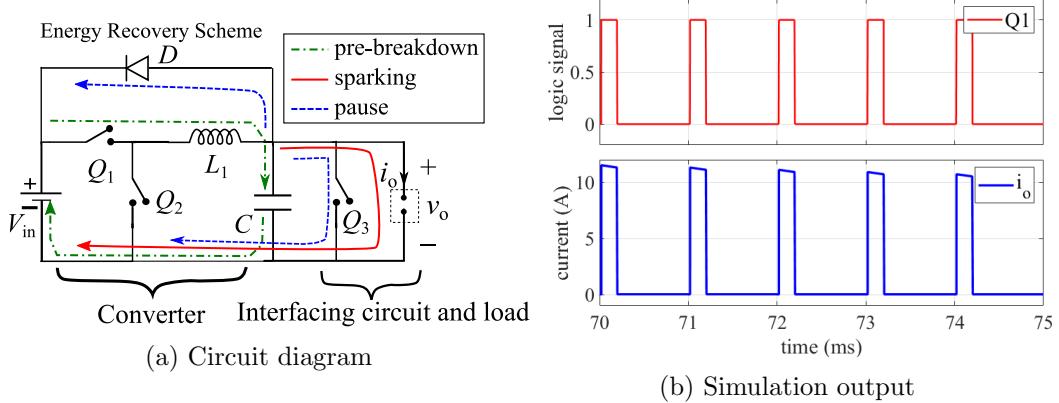


FIG. 4.12: **T8:** EPG with AVP control [96]

TABLE 4.2: Current paths for dual converter based topologies

Topology	Pre-breakdown	Sparking	Pause
T9 (Fig. 4.13)	$V_{in3}-R_3-Q_3-D_5-L_2$ -gap	$V_{in1}-V_{in2}-Q_1-L_1-Q_2-D_4$ - L_2 -gap	$V_{in2}-Q_1-L_1-D_2$ OR $L_1-D_2-V_{in1}-D_1$
T10 (Fig. 4.15)	$V_{in3}-R_3-Q_3-D_4-L$ -gap	high RRC $V_{in1}-Q_1-V_{in2}-D_3-L$ -gap- Q_2 low RRC $V_{in2}-D_3-L$ -gap- D_1-Q_1	$V_{in2}-D_3-L$ -gap- $D_1-V_{in1}-D_2$
T11 (Fig. 4.17(a))	$V_{in}-Q_1-L_1-D_2-C$	$V_{in}-Q_1-L_1$ -gap	$V_{in}-Q_1-L_1-Q_4$ AND $C-L_2-Q_3$
T12 (Fig. 4.18)	$V_{in}-Q_4$ -transformer- Q_3 AND transformer- D_6 - gap- D_7	$V_{in}-Q_1-L_1-D_3$ -gap	$V_{in}-Q_1-L_1-Q_2$

4.3.2 Dual converter based pulse generators

This section describes four important topologies T9 to T12. Here, topologies T9 and T10 use two or more separate DC links, whereas topologies T11 and T12 use a single DC link. They are subsequently named as per the number of DC links.

4.3.2.1 Dual converter with control of rate of rise of current (RRC)

Martin et al. [79] have proposed two topologies T9 and T10, in which the RRC is controlled at an optimum value such that the TEWR is minimum. However, it should be noted that the optimum value of RRC is not equal to its minimum value [79, 80]. Hence, transistorized pulse generator (topology T2 and T3) cannot be used in place of T9 and T10. Topology T9 consists of three parts: CS, VS and the interfacing circuit with load, as shown in Fig. 4.13. This topology is simulated in MATLAB simulink,

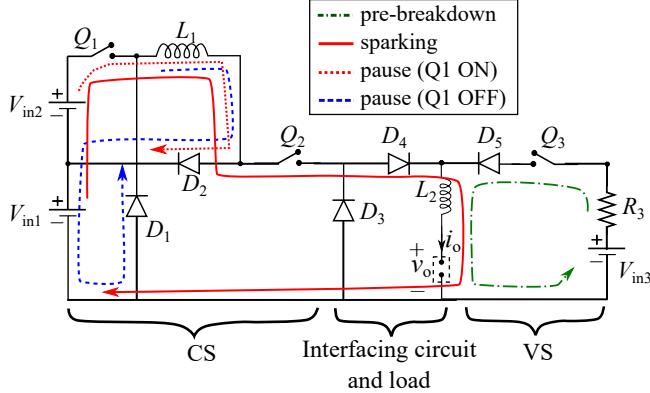


FIG. 4.13: **T9:** Dual converter with DC-link-controlled RRC [79]

with $V_{in1} = 30$ V, $V_{in2} = 5$ V, $V_{in3} = 100$ V, $L_1 = 300 \mu\text{H}$, and $R_3 = 100 \Omega$. Selected waveforms are shown in Fig. 4.14. To initiate the spark, Q_2 and Q_3 are switched ON simultaneously. The large resistance R_3 limits the current from V_{in3} , so that it is used only for the pre-breakdown stage and major portion of the required sparking current is supplied by the converter CS. During the sparking stage Q_2 is kept ON, whereas the switching of Q_1 is dictated by a current control loop. Hence, the switching frequencies of Q_2 and Q_3 are distinct from that of Q_1 as shown in Fig. 4.14. Various stages of operation can be seen in Fig. 4.13 and Table 4.2. Besides the current control, the RRC of spark current is also controlled by adjusting the DC link voltage V_{in1} , which is discussed in Section 4.5.3. Hence, this topology is referred to as dual converter with DC-link-controlled RRC. For simulations, only hysteresis current control is implemented to illustrate the basic operation of the topology.

Topology T10 is shown in Fig. 4.15, where L is the parasitic inductance, and current paths for different stages of operation are given in Table 4.2. The pre-breakdown stage is similar to the topology T9, obtained by closing of switch Q_3 . During the sparking stage, converter CS supplies the sparking current. Unlike topology T9, RRC is changed by operating either both the switches Q_1 and Q_2 (for high RRC) or only one of them (for low RRC) as shown in Table 4.3. Hence, this topology is referred to as dual converter with switching-controlled RRC. Simulation output of this topology is shown in Fig. 4.16. As reported by [79], the output switch Q_3 is triggered during the complete sparking stage. However, it would be sufficient to turn this switch only for triggering the spark.

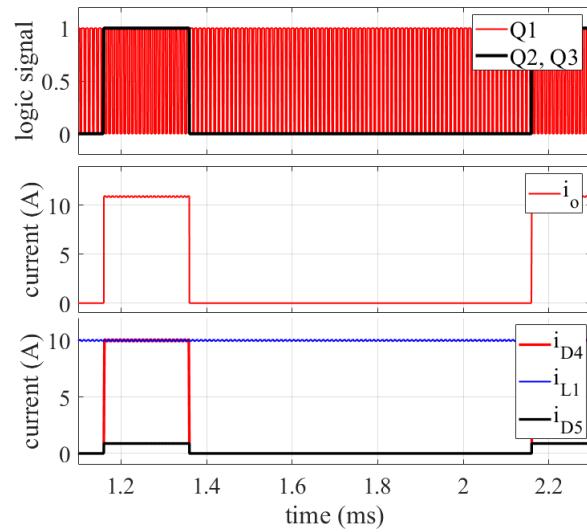


FIG. 4.14: Simulation output of topology T9

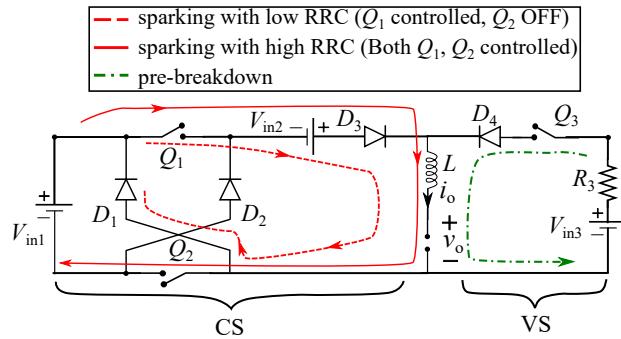


FIG. 4.15: T10: Dual converter with switching-controlled RRC [79]

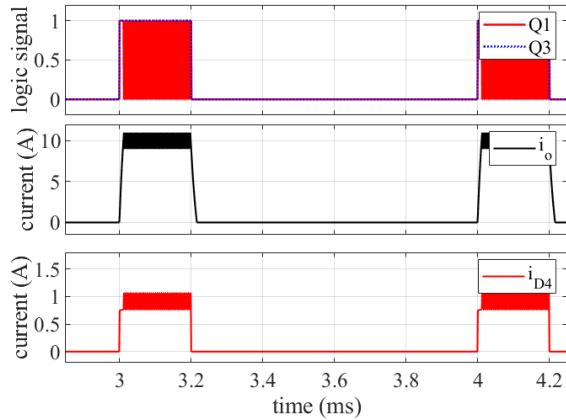


FIG. 4.16: Simulation output for T10

TABLE 4.3: Change in RRC by changing the switches in operation

RRC	Switches in operation	RRC
High	Both Q_1 and Q_2	$\frac{V_{\text{in}1} + V_{\text{in}2} - v_o}{L}$
Low	Q_1 in operation, Q_2 OFF	$\frac{V_{\text{in}2} - v_o}{L}$

4.3.2.2 Dual converters with a single DC-link

Topologies in this category have single DC link as against the topologies T9 and T10 in the last section. The first topology of this category, proposed by Tastekin et al. [46], is shown in Fig. 4.17(a) which has three parts the CS, the VS, and the interfacing circuit. Converter VS is a two-quadrant converter, with voltage across C kept at V_{ref} such that $V_{\text{ref}} > V_b$. Converter CS is a buck converter modified as current source where switch Q_1 is controlled using current through inductor L_1 as feedback.

During *pre-breakdown* stage, the switch Q_4 is OFF and the gap is yet to break down. Hence, i_{L1} flows from L_1 to C via D_2 . When the gap breaks down, the *sparking* stage begins, i_{L1} flows from L_1 to the WEDM load and hence $i_o = i_{L1}$. During the prebreakdown stage, the capacitor may be charged to a voltage greater than V_{ref} . In such a case, the controller acts such that Q_2 is turned OFF and Q_3 is turned ON. The capacitor then discharges through either Q_3 via path $C-L_2-Q_3$ or the body diode of Q_2 via path $C-L_2-Q_2-V_{\text{dc}}$. To initiate the *pause* stage, the switch Q_4 is turned ON, the voltage v_o reduces to zero and i_{L1} flows from L_1 to Q_4 . Simulation studies of this topology are presented in next chapter.

Another topology is proposed by Looser et al. [95] for the application of removing metal chips using dry EDM, where the dielectric is air and spark gap is of the order of 1 mm. Hence, a high voltage (≈ 1 kV) is provided by the cascaded connection of an H-bridge inverter, a high voltage transformer and a diode bridge rectifier, which is referred to as HVS in Fig. 4.18. The operation of this topology is similar to that of T11 except the following changes. HVS provides a high voltage for spark initiation. Until the breakdown, in the pause stage, switch Q_1 is controlled using current through L_1 as a reference signal, whereas switch Q_2 is continuously ON. When Q_3 and Q_4 are turned ON, a high voltage is applied across the load, which marks the beginning of pre-breakdown stage. Q_2 is turned OFF immediately so that the current flows to the

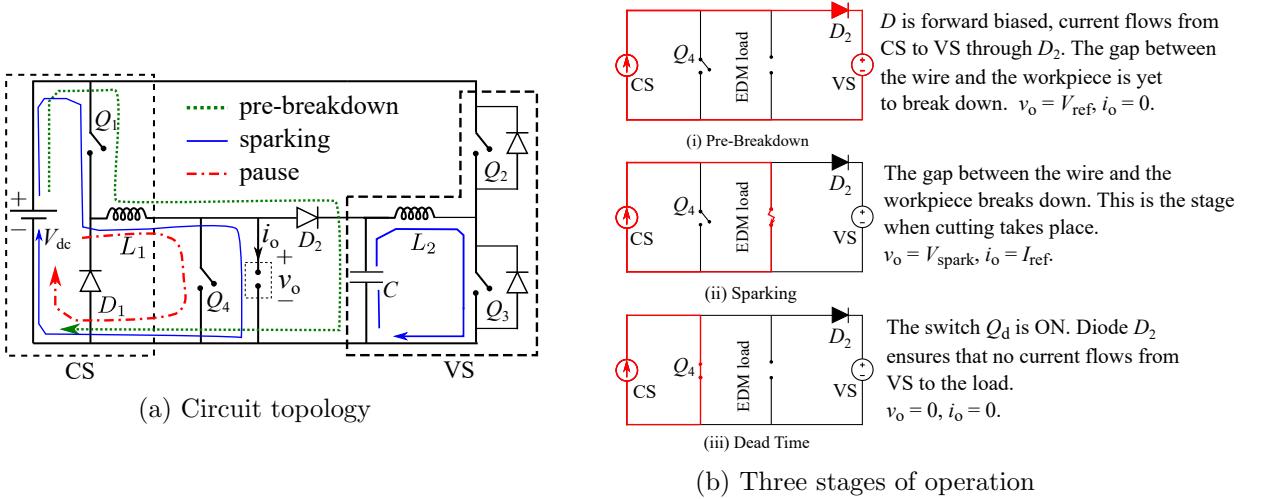


FIG. 4.17: T11: Dual converter with single DC link [46]

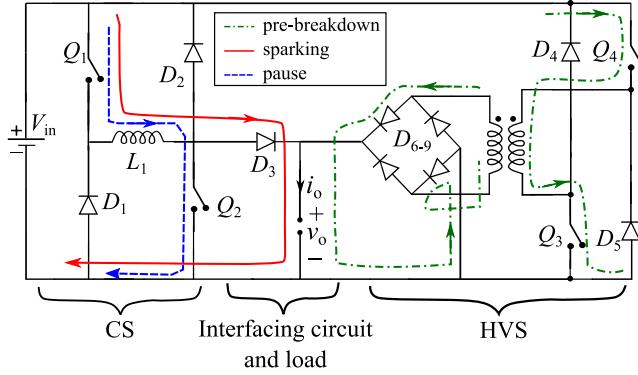


FIG. 4.18: T12: HV dual converter with single DC link [95]

load via D_3 , as shown in Fig. 4.18. Simulation results for this topology are shown in Fig. 4.19 for $V_{in} = 100$ V, $L_1 = 100 \mu\text{H}$, turns ratio = 1. It can be noted that, the duty ratio of switch Q_1 is varying as it is controlled by the current mode control. Whereas, duty ratios of switches Q_2 , Q_3 and Q_4 are constant. While this topology is originally proposed for HV pulses, the specifications stated in Fig. 4.1 are used for simulation.

4.3.3 Resonant converter based pulse generators

There are several forms of EPG topologies consisting of LCC resonant converter proposed by Casanueva et al. [84–93]. Recently, Odulio et al. have proposed a topology using an LLC resonant converter as well [94]. This class of EPGs is proposed for a specific application of *portable* onsite machining.

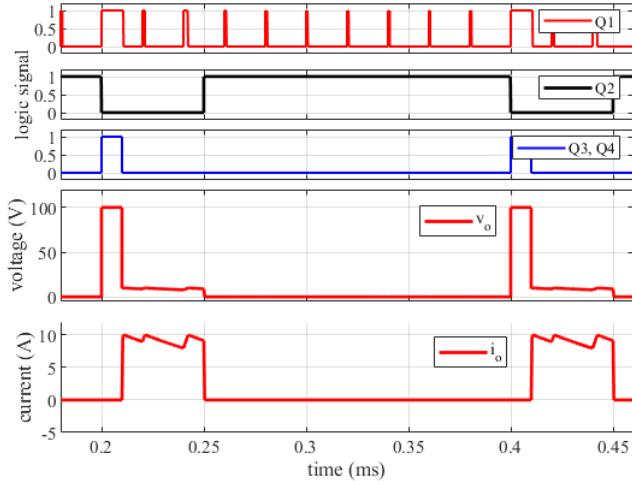


FIG. 4.19: Simulation output of topology T12

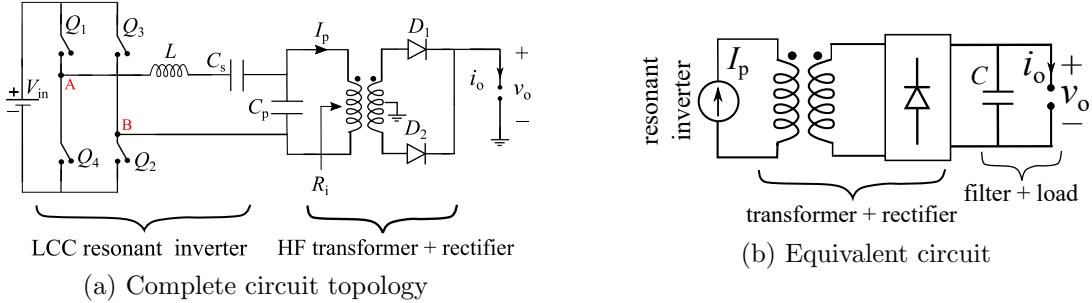


FIG. 4.20: T13: Resonant converter based EPG [87]

One form of EPG based on a resonant converter is shown in Fig. 4.20(a). Here, the current flowing into the primary winding (I_p) is given by (4.3) [90], [173]:

$$I_p = \frac{4V_{in}}{\pi Z_p Q_p} \sqrt{\frac{1 + Q_p^2 \left(\frac{\omega}{\omega_p}\right)^2}{1 + \left[\frac{1}{Q_p} \left(\frac{\omega}{\omega_p} - \frac{\omega_p}{\omega} A\right) \left(1 + Q_p^2 \left(\frac{\omega}{\omega_p}\right)^2\right) - Q_p \frac{\omega}{\omega_p}\right]^2}} \quad (4.3)$$

where, $\omega_p = 1/\sqrt{LC_p}$: ω_p is parallel resonant frequency

$$Z_p = \omega_p L = 1/(\omega_p C_p)$$

$$Q_p = R_i/Z_p: Q_p \text{ is parallel quality factor}$$

$$A = C_p/C_s$$

$$\omega_o = \omega_p \sqrt{A + 1}: \omega_o \text{ is unloaded natural resonant frequency}$$

R_i is the equivalent impedance of the transformer, rectifier and the gap resistance, as seen from terminals of the primary of transformer [90]. From (4.3), it can be derived

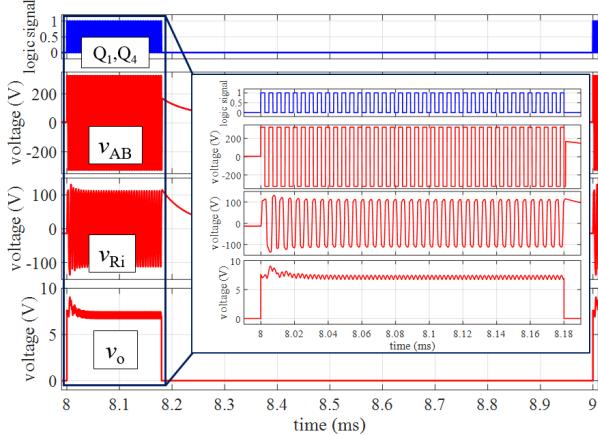


FIG. 4.21: Simulation output of topology T11

that, when $\omega = \omega_o$, the current amplitude through R_i becomes:

$$I_p \Big|_{\omega=\omega_o} = \frac{4V_{in}\sqrt{A+1}}{\pi Z_p} \quad (4.4)$$

From (4.4), I_p becomes independent of R_i i.e. the load, and therefore the circuit acts like a constant current source irrespective of the stage of the operation of EDM. Hence, the topology can be represented as an equivalent circuit shown in Fig. 4.20(b) where, I_p represents the resonant inverter. Thus, the topology can be viewed as a derived form of the basic topology T1 (Fig. 4.3(a)), where $V_{in}\cdot R$ is replaced by the cascaded connection of ‘‘resonant inverter-transformer-rectifier’’. The transformer turns ratio is chosen appropriately to get the desired spark-initiation voltage [90]. The circuit is operated at a frequency just above the resonant frequency in order to achieve zero voltage switching.

Fig. 4.21 shows the simulation results with $L = 447 \mu\text{H}$, $C_s = 7 \text{ nF}$, $C_p = 1.76 \text{ nF}$, $f_{sw} = 200 \text{ kHz}$, transformer ratio = 5. It can be seen that the voltage v_{AB} is a square wave, whereas the voltage v_{Ri} is almost sinusoidal. To initiate the spark, triggering pulses are given to the switches Q_1 through Q_4 during t_{ON} . To initiate the pause stage, the triggering pulses are removed. It can be seen that here also, there are two dominant frequencies in the waveforms. Appropriate switches which allow high frequency switching should be used to realize this topology.

4.3.4 Summary of operation of topologies

Single-converter based topologies do not have a separate circuit for spark-initiation hence, only two stages can be explicitly indicated in these circuits (except for the topology T8) as listed in Table 4.1. For the topology T8 (Fig. 4.12), the current flows through V_{in} - Q_1 - L_1 - C and V_{in} - Q_1 - L_1 -gap during the pre-breakdown and the sparking stage respectively. For the pause stage, Q_3 is turned ON and the inductor current flows back through diode D .

For the dual-converter based topologies, all the three stages can be explicitly seen as listed in Table 4.2. In case of the resonant converter based topologies, the current flows through the “inverter-transformer-rectifier- C -gap” path during t_{ON} and through “ C -gap” during t_{OFF} .

4.3.5 Other Topologies

Apart from the important topologies described in the previous subsections, some researchers have proposed some EPGs which are modified forms of some topologies described above. For example, Chen et al. [72] have proposed a pulse generator which is a modified form of transistorized pulse generator topology T3. Han et al. [73] have proposed a transistorized iso-pulse generator which can provide pulses with discharge duration of 30-80 ns and hence improve MRR as compared to the RC type pulse generators. These type of pulse generators are particularly suitable for micro-EDM. Mysinski [74] has used TOP-switch based voltage source and current source, along with interfacing circuit composed of an H-bridge to construct a low power (35 V, 3A) EPG. Wang et al. [75] have used very high frequency resonant pulse generator for micromachining on mesoscopic scale. There are various kinds of electromagnetic forces which can affect the surface finish in WEDM [32]. Nakashima et al. [81] have patented a bipolar supply which uses a bridge circuit to create a bipolar output, so that the electrostatic forces are reduced giving a better surface finish. Hu et al. [76] have proposed a multi-mode RC pulse generator. Mahmud et al. [77] have proposed transistorized pulse generator for micro-machining of hip-implants.

4.4 Efficiency Computation

4.4.1 Basic formulation

Sen et al. [45] and Yang et al. [96] have stated that the efficiency of EPGs is given by the following formula.

$$\eta = \frac{V_{\text{spark}}}{V_{\text{in}}} \times 100\% \quad (4.5)$$

For $V_{\text{in}} = 100$ V and $V_{\text{spark}} = 20\text{-}30$ V, the efficiency would be 20%-30%. This formulation is valid only for the topology T2 (Fig. 4.4). It can be easily derived by considering the efficiency $\eta = P_{\text{out}}/P_{\text{in}}$ as follows. It is assumed that the current flows in the loop $V_{\text{in}}\text{-}R\text{-gap}$ during t_{ON} and no current flows during t_{OFF} . Then, the average value of the current for both input and output is the same given by

$$I_{\text{avg}} = D_m I_{\text{ref}} \quad (4.6)$$

Therefore, efficiency η is given by

$$\eta = \frac{D_m I_{\text{ref}} V_{\text{spark}}}{D_m I_{\text{ref}} V_{\text{in}}} = \frac{V_{\text{spark}}}{V_{\text{in}}} \quad (4.7)$$

However, for the other topologies there are several current loops and it is not straightforward to get the input current waveforms in each case. Hence, (4.8) is used to calculate the efficiency, where, the total losses (P_{loss}) comprise of the conduction loss (P_{cond}) and the switching loss (P_{swch}).

$$\eta = \frac{P_{\text{out}}}{P_{\text{loss}} + P_{\text{out}}} = \frac{P_{\text{out}}}{P_{\text{swch}} + P_{\text{cond}} + P_{\text{out}}} \quad (4.8)$$

Referring to load voltage (v_o) and load current (i_o) in Fig. 1.6, the output power can be computed by (4.9).

$$P_{\text{out}} = \frac{1}{T_m} \int_0^{T_m} v_o(t) i_o(t) dt = \frac{1}{T_m} \int_{d_1 T_m}^{(d_1+d_2)T_m} V_{\text{spark}} I_{\text{ref}} dt = d_2 V_{\text{spark}} I_{\text{ref}} \quad (4.9)$$

Due to the different functionality of each topology, the computation of losses would be different for each topology. However, the complete efficiency computation is illustrated with an example in the following subsection.

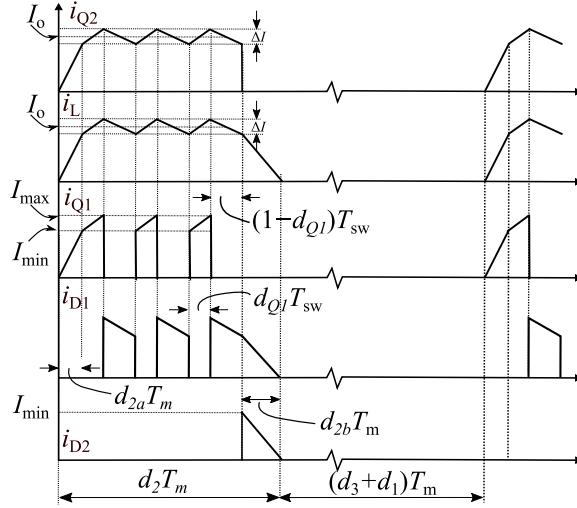


FIG. 4.22: Current waveforms for elements in topology T6 (Fig. 4.10(a))

4.4.2 Example of efficiency computation

Let us consider the example of topology T6 (see Fig. 4.10(a)). Operation of the topology is already explained in Section 4.3.1.5. Accordingly, waveforms for current through elements Q_2 , L , Q_1 , D_1 and D_2 are sketched in Fig. 4.22, which match closely with those in Fig. 4.10(b). Note that intervals $d_{2a}T_m$ and $d_{2b}T_m$ represent the finite rise and fall times of currents. The duty ratio of Q_1 (d_{Q1}) is decided by the current control feedback loop with i_L as the feedback variable. It should be noted that the duty ratio d_{Q1} is with respect to the time period T_{sw} whereas the other duty ratios are with respect to time period T_m . Expressions for RMS values of i_{Q2} , i_L , i_{Q1} and average (AVG) values of i_{D1} , i_{D2} are derived and given in (4.10) and (4.11) below.

$$\begin{aligned} \text{RMS}(i_{Q2}) &= \sqrt{I_{\max}^2 \frac{d_{2a}}{3} + (d_2 - d_{2a} - d_{2b}) \left(I_o^2 + \frac{\Delta I^2}{12} \right)} \\ \text{RMS}(i_L) &= \sqrt{I_{\max}^2 \frac{d_{2a} + d_{2b}}{3} + d_2 \left(I_o^2 + \frac{\Delta I^2}{12} \right)} \\ \text{RMS}(i_{Q1}) &= \sqrt{I_{\max}^2 \frac{d_{2a}}{3} + d_{Q1}(d_2 - d_{2a} - d_{2b}) \left(I_o^2 + \frac{\Delta I^2}{12} \right)} \end{aligned} \quad (4.10)$$

$$\begin{aligned} \text{AVG}(i_{D1}) &= \frac{I_{\max} + I_{\min}}{2} (1 - d_{Q1})(d_2 - d_{2a}) + \frac{I_{\min}}{2} d_{2b} \\ \text{AVG}(i_{D2}) &= \frac{I_{\min}}{2} d_{2b} \end{aligned} \quad (4.11)$$

It should be noted that the formulae contain the product of two duty ratios corresponding to two distinct frequencies. Instead of this, an *equivalent* duty ratio can be computed and then it can be multiplied with the appropriate magnitude of current to get the RMS/AVG value as elaborated in Section 5.2. The conduction loss is then computed as

follows [171]:

$$P_{\text{cond}} = \begin{cases} I_{\text{rms}}^2 R_{\text{EQ}} & \text{for PE switches/cap./inductors} \\ I_{\text{avg}} V_{\text{D}}^{\text{ON}} & \text{for diodes} \end{cases} \quad (4.12)$$

where, R_{EQ} is the DC resistance for inductors, the ESR for capacitors and $R_{\text{EQ}} = R_{\text{DS}}^{\text{ON}}$ i.e. the ON state resistance for MOSFET switches; V_{D}^{ON} is the ON state voltage drop across the diode. The switching losses are calculated as follows [171, 174]:

$$P_{\text{swch}} = \begin{cases} (E_{\text{ON}} + E_{\text{OFF}}) f_{\text{swn}} & \text{for active switches} \\ E_{\text{rr}} f_{\text{swn}} & \text{for diodes} \end{cases} \quad (4.13)$$

where, E_{ON} , E_{OFF} are the energy losses during turning ON and turning OFF a switch, respectively. E_{rr} is the energy lost during reverse recovery of the diodes. These values can be obtained from the device datasheets [174]. The frequency f_{swn} indicates the number of times switching happens per second for a particular switch. This depends on operation of a topology. In case of the topology T6 (Fig. 4.10(a)), Q_1 is switched at f_{sw} for the duration t_{ON} out of the period T_m , hence $f_{\text{swn}} = f_{\text{sw}} t_{\text{ON}} / T_m = f_{\text{sw}} D_m$. Q_2 is switched only once during the pulse period T_m , hence for Q_2 , $f_{\text{swn}} = f_m$. In some topologies, $f_{\text{swn}} = f_{\text{sw}}$, where the switches are operated throughout the pulse period T_m , e.g. Q_1 in the topology T11 (Fig. 4.17(a)).

The following values are taken for calculations: $R_{\text{sp}} = 1 \Omega$, $i_o = 10 \text{ A}$, $\Delta I = 1 \text{ A}$, which means $I_{\text{avg}} = 10 \text{ A}$, and $I_{\text{max}} = 10.5 \text{ A}$, $d_2 = 20\%$, $d_{2a} \approx d_{2b} \approx 0.2\%$, $d_{Q1} = 10\%$, $V_{\text{D}}^{\text{ON}} = 1 \text{ V}$. These values are substituted in (4.10) and (4.11) to get RMS and average values of currents. A MOSFET suitable for these ratings - IRFP4137PbF is considered and the switching losses are computed from the datasheet information [175]. Then using (4.9), (4.12), (4.13) and (4.8), the efficiency value can be computed as 72.54%.

4.4.3 Generic procedure for efficiency computation

From the above example, it is evident that the following points need to be accounted for in efficiency computation for EPGs: (a) There are two distinct switching frequencies: f_m and f_{sw} . Hence, there are two distinct duty ratios as well. (b) Due to pulsed nature of the load, many converters operate in discontinuous mode of operation, and hence the current waveforms need to be sketched carefully, before deriving expressions for RMS or average values.

As every EPG topology is different from others in terms of control strategy and operation, general steps to be followed while computation of efficiency can be stated with the following assumptions:

1. I_{ref} , V_{spark} , f_m , and f_{sw} are fixed depending on the required machining performance parameters: MRR, SR and TEWR.
2. d_{2a} and d_{2b} are assumed to be negligible.
3. The pre-breakdown phase is stochastic in nature. So it needs to be accounted only for the cases where the delay is significant. In this work, it is assumed that $d_1 \approx 0$. Therefore, $d_2 = D_m$.

From (4.10) and (4.11), the RMS and average values of the currents are approximately proportional to d_2 , i.e. D_m .

$$I_{\text{rms}}^2 \propto D_m \quad \text{and} \quad I_{\text{avg}} \propto D_m \quad (4.14)$$

From (4.12) and (4.14), it can be easily seen that

$$P_{\text{cond}} \propto D_m \quad (4.15)$$

It should be noted that the switching losses are a function of f_m or f_{sw} or both as it is seen from (4.13). For a given topology and the given values of V_{ref} , I_{ref} , f_m and f_{sw} , the switching losses can be considered to be approximately constant: $P_{\text{swch}} = \alpha$. The conduction losses can be considered to be: $P_{\text{cond}} = \beta D_m$, where α , β are constants which need to be determined for each topology. From (4.8), (4.9), (4.15) and (4.14) the expression for efficiency can then be given by (4.16).

$$\eta = \frac{V_{\text{spark}} I_{\text{ref}} D_m}{\alpha + \beta D_m + V_{\text{spark}} I_{\text{ref}} D_m} \times 100\% \quad (4.16)$$

If the pulse repetition frequency is not fixed, then by putting $D_m = t_{\text{ON}} f_m$, another equivalent generic expression for the efficiency would be:

$$\eta = \frac{V_{\text{spark}} I_{\text{ref}} t_{\text{ON}} f_m}{\alpha + \beta t_{\text{ON}} f_m + V_{\text{spark}} I_{\text{ref}} t_{\text{ON}} f_m} \times 100\% \quad (4.17)$$

Based on the discussion above, some generic steps to compute the efficiency of the power-electronics based EPGs are given in Fig. 4.23.

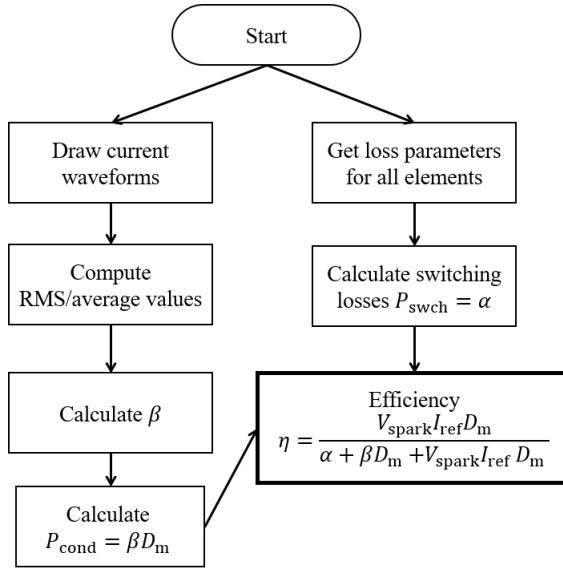


FIG. 4.23: Steps in calculation of efficiency

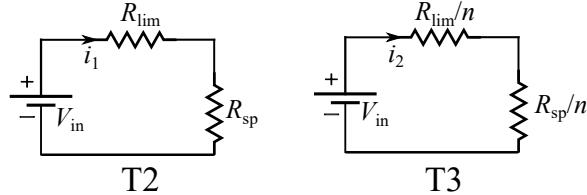


FIG. 4.24: Equivalent circuit during the sparking stage for topologies T2 and T3

4.4.4 Efficiency comparison

Efficiencies are computed for all the topologies using this method and the values are listed in Table 4.9 in Section 4.7. All the efficiency values are computed for the load values as given in Fig. 4.1. It should be noted that for topology T3, the number of parallel branches in operation are increased only when the EDM-load increases [47]. Hence, for the sake of comparative study, the equivalent circuits during the sparking stage for the topologies T2 and T3 are shown in Fig. 4.24. Here, it is assumed that the load resistance is scaled down by n . It is proved in Table 4.4 that, the efficiencies of both topologies are the same. However, in practice, it may not always be possible to express the increase in the spark load by scaling down the original load by an integer n . Hence, in practice, the efficiency of T3 might not be the same as that of T2. From the efficiency column in Table 4.9 at the end of the chapter, it can be seen that the efficiencies of many EPG topologies are around 30% to 50%. Lower values of efficiencies can be attributed to the following reasons:

TABLE 4.4: Comparison of quantities for topologies T2 and T3

Quantity	Topology T2	Topology T3
Current	$i_1 = \frac{V_{in}}{R_{lim} + R_{sp}}$	$i_2 = \frac{V_{in}}{R_{lim}/n + R_{sp}/n}$
Output power	$i_1^2 R_{sp}$	$i_2^2 R_{sp}/n = ni_1^2 R_{sp}$
Losses	$i_1^2 R_{lim}$	$i_2^2 R_{lim}/n = ni_1^2 R_{lim}$
Efficiency	$\frac{i_1^2 R_{sp}}{i_1^2 R_{lim} + i_1^2 R_{sp}}$	$\frac{i_1^2 R_{sp}}{i_1^2 R_{lim} + i_1^2 R_{sp}}$

1. Topologies T1, T2, T3, T5, T5-a, T9 and T10 use resistive elements to limit the spark currents.
2. Due to pulsed nature of the load, many topologies operate in discontinuous mode of operation. This resembles part-load operation of standard DC-DC converters and hence a lower value of efficiency is expected [170, 176].
3. The control schemes of some topologies are such that the current continues to flow in parts of the circuit other than the gap during the pause stage e.g. in topology T11. As $D_m = 20\%$ for these computations, the current contributes to losses for 80% of the machining cycle.

The actual losses may vary depending upon the choice of passive elements and PE switches. However, this chart is the first time that an account of comparison of efficiencies is given for the EPG topologies.

In production engineering parlance, the machining efficiency is given by the specific energy consumption (SEC) as follows [159]

$$SEC = \frac{\text{Energy consumed}}{\text{Volume of workpiece removed}} \quad \text{kJ/mm}^3 \quad (4.18)$$

If the other mechanical process parameters e.g. materials of the workpiece and the tool, feed rate etc., are kept the same, the above efficiencies can be easily translated into the machining efficiencies.

4.5 Control Schemes

4.5.1 Effect of electrical parameters on machining performance

Control schemes of EPGs should be understood with respect to the WEDM block diagram in Fig. 3.3. EPG control parameters viz., V_{ref} , I_{ref} , D_m and T_m affect the machining performance.

V_{ref} should be selected appropriately such that it is greater than the breakdown voltage V_b , which is decided by the geometry and material of electrodes, dielectric material and temperature and pressure. If application demands a high voltage for breakdown e.g. in case of dry EDM for rotor balancing application as discussed in [95], an appropriate provision for high voltage is necessary.

TABLE 4.5: Effect of I_{ref} and t_{ON} on machining performance parameters [23]

Current (I_{ref})	ON time (t_{ON})	MRR	TEWR	SR	Suitability
Medium (10 - 50 A)	Medium (20 - 50 μs)	High	Low	High	Rough Machining
Low (2- 10 A)	Long (100 - 400 μs)	Poor	Low	Low	Finishing
High (70 - 120 A)	Short (1 - 10 μs)	High	High	Low	WEDM

Effect of I_{ref} and t_{ON} on MRR, TEWR and SR is consolidated in Table 4.5 [23]. It is clear that only two of these three machining performance parameters can be improved at a time. Depending on which two parameters are improved, the machining is classified as rough machining, finishing or WEDM as denoted in Table 4.5. The other possible combinations like high current and long discharge duration or short discharge duration with low current are not used as they are not useful for machining [23]. It should be noted that short discharge duration is required for WEDM, hence fast switching wide-bandgap devices can be used if EPG is to be designed for WEDM.

EPG topologies are originally proposed to improve either (a) some machining performance parameters - MRR, SR or TEWR or (b) some electrical performance parameters e.g. efficiency (EFF), reduction in overall volume (VOL) etc. Some specific control schemes are implemented on top of the conventional voltage and/or current control schemes to achieve these objectives. Such schemes are described in the following subsections.

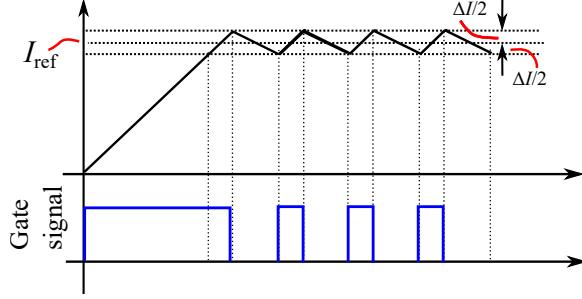


FIG. 4.25: Hysteresis current control

4.5.2 Control schemes for single converter based topologies

Most of the single converter based EPGs employ current control as indicated by the block diagram in Fig. 4.26. It can be either current programmed control, peak current control or hysteresis current control [171], [170]. In hysteresis current control, a tolerance band is defined around the desired reference value. In the context of EDM, this reference value is mostly a DC value I_{ref} as indicated in Fig. 4.25. The upper limit is defined by $I_{\text{ref}} + \Delta I/2$ and the lower limit is defined by $I_{\text{ref}} - \Delta I/2$. When the current exceeds an upper limit i_H , the triggering signal is removed or the switch is turned OFF. When the current hits a lower limit i_L , the PE switch is turned ON. This is schematically shown by the gate signal in Fig. 4.25. This scheme suffers from the disadvantage of variable switching frequency. Due to the desired operating band between i_H and i_L , this scheme is also sometimes called as hysteresis band current control (HBCC) [177].

Besides that, there are special schemes which are part of WEDM master control. Some crucial schemes out of these are described below. H-bridge like converter (topology T5, T5-a in Figs. 4.8(a) and 4.9) has been originally proposed for DEDM to improve MRR and reduce TEWR. Inventors of this topology have experimentally proved that, the MRR is maximum when the ratio $\frac{t_{\text{OFF}}}{t_{\text{ON}}}$ is kept between 0.1 and 0.2. However, as stated in the previous section, an improvement in performance parameters MRR and TEWR is accompanied by a corresponding increase in SR as well. As the output voltage of the topology T5-a (Fig. 4.9(a)) is bipolar, it can reduce the galvanic corrosion of the electrodes in DEDM [80]. In topologies T6 and T7 (in Figs. 4.10(a) and 4.11(a)), as there is an explicit interfacing circuit, it is ensured that the spark current starts always from zero irrespective of t_{OFF} . Also, the bipolar output in T7 (Fig. 4.11(a)) can prevent minor cracks in the workpiece [78].

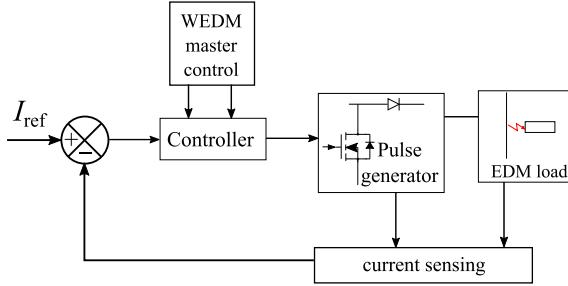


FIG. 4.26: Control schemes for single converter based topologies

However, topologies T1, T2 and T3 in Figs. 4.3(a), 4.4, 4.5 are the basic topologies. No specific control scheme is mentioned in the literature for T1 and T2. However, for T3, Ozaki and Tsuromoto [47] have suggested a control scheme where number of times a discharge occurs, is used as a feedback signal. If this number exceeds a safe limit, then t_{OFF} is increased such that the average value of current is reduced below the threshold and thus wire breakage can be avoided.

Adaptive voltage positioning (AVP) control is used for topology T8 (in Fig. 4.12). In AVP, a reference voltage is obtained by (4.19) where, k_v and k_i are the respective proportional gains. During the pre-breakdown stage, $i_o = 0$, therefore, $v_{ref} = k_v v_o(t)$. During sparking stage, the reference voltage is given by (4.20)

$$v_{ref}(t) = k_v \cdot v_o(t) + k_i \cdot i_o(t) \quad (4.19)$$

$$v_{ref}(t) = k_v \cdot V_{spark} + k_i \cdot i_o(t) \quad \dots \text{sparking stage} \quad (4.20)$$

Thus, this converter can toggle between current control and voltage control automatically. A detailed control system design is presented in [96].

4.5.3 Control schemes for dual converter based topologies

The dual converter based topologies usually have two control loops, one for voltage control and the other for current control, as shown in Fig. 4.27. Some of the peculiar control schemes are described below.

Topologies T9 (see Fig. 4.13) and T10 (see Fig. 4.15) implement RRC control besides the current mode control. The reason behind this is as follows. As EDM discharge is a stochastic process, RRC varies in each machining cycle. For a particular set of the electrode material and dielectric between the gap, the RRC varies from a minimum value S_{min} to a maximum value S_{max} as shown in Fig. 4.28. It has been proven by

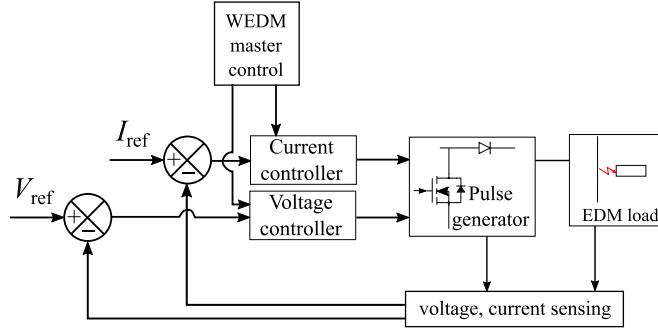


FIG. 4.27: Control schemes for dual converter based topologies

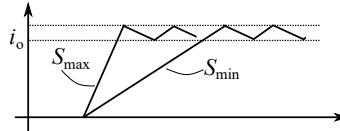


FIG. 4.28: Variation in rate of rise of spark current (RRC)

experiments that TEWR is minimum, when the spectrum of slopes $S = S_{\max} - S_{\min}$ is maximum [79]. By prior-experimentation the optimum RRC S_{ref} corresponding to a required TEWR is obtained. The RRC control loop takes the RRC averaged over n cycles, S_{avg} as the input and compares it with S_{ref} . The RRC is then varied to match S_{avg} with S_{ref} . In topology T9, this is done by changing the DC link voltage $V_{\text{in}1}$ and in topology T10, the circuit is operated at higher or lower RRC (as shown in Table 4.3) such that the averaged value is equal to S_{ref} .

Topology T11 (Fig. 4.17(a)) employs both voltage and current control. Topology T12 employs only current control whereas the breakdown voltage is provided by the HVS and its value depends on the ratio of the transformer in the topology.

4.5.4 Control schemes for resonant converter based topologies

As denoted in (4.4), the output current of the resonant converter based topologies is independent of load for $\omega = \omega_0$. During t_{ON} , the PE switches in the inverter in Fig. 4.20(a) are switched at frequency just greater than f_0 corresponding to ω_0 [90]. A simple current mode control is also suggested in [84], which is shown in Fig. 4.29. Here, the output current of the inverter is sensed and if it changes, the switching frequency of the inverter is set accordingly. The output current might change, due to change in t_{ON} or stochastic variation in the physical conditions at the gap.

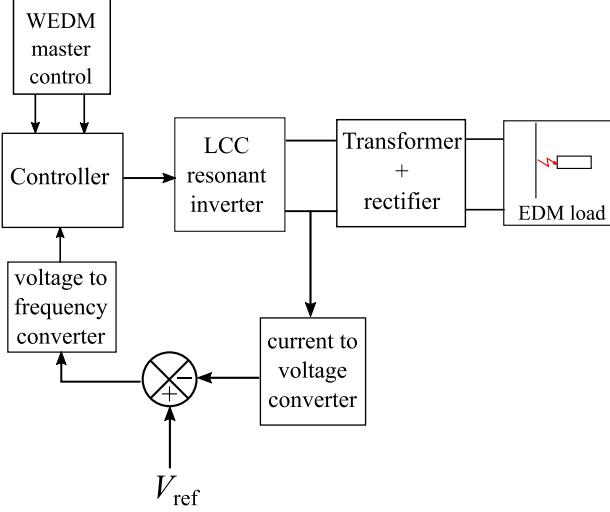


FIG. 4.29: Control scheme for resonant converter based EPG

4.5.5 Summary of Control Schemes

Control schemes for all the topologies are summarized in Table 4.6. The column ‘target’ mentions electrical or machining parameter which is the objective of the topology as proposed in the original articles. As T1 and T2 are the earliest of pulse generators, when the power electronics was not advanced, they do not have specific target.

A control complexity index (CCI) is assigned on the scale of 1 to 5 considering the number of feedback loops, corresponding sensor requirements and the computational complexity for implementing a particular scheme. For example, in [96], AVP control is suggested for topology T8, which is computationally more complex as compared to simple current programmed control. Hence, its CCI value is high and equal to 4. Topologies T9 and T10 also have a large CCI, because both require computation of RRC, besides two separate loops for voltage and current control.

This table can be utilized as a basis to choose a particular control scheme to achieve a specific target. Also, the schemes for one topology can be employed for another to achieve a similar target. For example, in [79], the authors have suggested control of RRC to keep TEWR minimum. This RRC-control can be implemented in topologies T6 and T7 as well.

TABLE 4.6: Control schemes for EPG topologies as suggested in the original articles

	Circuit description	Control Scheme	Target	CCI
T1	RC Pulse generator	No control scheme employed	NA	1
T2	Transistorized pulse generator with single switch	The switch is controlled by open loop control with inputs D_m and T_m .	NA	1.5
T3	Transistorized pulse generator with multiple switches	Number of discharges per unit time are sensed to control triggering signals of multiple switches. Number of switches to be used is decided by required spark current.	TEWR	2.5
T4	Interleaved buck converter with ERS	Current control is implemented for the modified buck converter. Due to interleaving of topologies, the converter can work with lower switching frequencies as well.	EFF, VOL	1.5
T5	H-bridge like converter	Peak current control is implemented. Ratio t_{OFF}/t_{ON} is kept as low as possible to increase MRR.	MRR	2.5
T6	EPG with unipolar interfacing circuit	Hysteresis current control is used for the modified buck converter. Switch Q_2 is controlled with duty ratio D_m and at frequency f_m by open loop control.	TEWR, MRR	2
T7	EPG with bipolar interfacing circuit	Control scheme similar to T6. Bipolar output prevents minor cracks in the workpiece.	TEWR, SR	2
T8	Pulsed power supply with AVP control	AVP control is implemented to adjust the current as per the stage of operation. Control scheme is more complex than a simple current control.	EFF	4
T9	Dual converter with DC-link-controlled RRC	There are two control loops. One loop uses RRC as the feedback variable. Input voltage is adjusted as per RRC to give optimum MRR. Current control is used to maintain the sparking current at a reference value. Open loop control is implemented for the interfacing circuit to control D_m and T_m .	TEWR	5
T10	Dual converter with switching-controlled RRC	RRC is controlled by selective triggering of a combination of switches instead of adjusting the DC link voltage. Control of D_m and T_m is similar to that for topology T9.	TEWR	4.5
T11	Dual converter with Single DC-link	Two feedback loops are present: current control loop for one converter and voltage control loop for the other. Open loop control is implemented for interfacing circuit to control D_m and T_m .	EFF	4
T12	HV dual converter with single DC-link	One feedback loop is present for current control. Ignition voltage magnitude is not controlled but it is decided by the transformer. D_m and T_m is controlled by open loop control.	High voltage for spark initiation	3.5
T13	Resonant converter	One feedback loop is present in which the output voltage is sensed and the operating frequency of the converter is changed so that the frequency is equal to resonant frequency at the time of sparking.	VOL	3.5

TABLE 4.7: Comparison of number of components

Topology	PE Switches	Diodes	Passive elements	DC Links
T1 (Fig. 4.3(a))	0	0	2	1
T2 (Fig. 4.4)	1	0	1	1
T3* (Fig. 4.5)	3	0	3	1
T4 (Fig. 4.7(a))	4	8	8	1
T5 (Fig. 4.8(a))	2	3	1	1
T6 (Fig. 4.10(a))	2	4	1	2
T7 (Fig. 4.11(a))	5	2	1	1
T8 (Fig. 4.12)	3	1	2	1
T9 (Fig. 4.13)	3	5	2	3
T10 (Fig. 4.15)	3	4	1	3
T11 (Fig. 4.17(a))	4	2	3	1
T12 (Fig. 4.18)	4	9	2	1
T13 (Fig. 4.20(a))	4	2	4	1

*T3 can have n number of switches depending on the current requirement.

TABLE 4.8: Voltage stress of the active switches

Topology	Q_1	Q_2	Q_3	Q_4	Q_5
T2	1.0				
T3	1.0	1.0	1.0		
T4	1.0				
T5	1.0	1.0			
T5-a	0.50	0.50	1.27		
T6	1.0	0.73			
T7	1.0	1.0	1.0	1.0	1.0
T8	1.0	1.0	1.0		
T9	0.32	0.32	1.0		
T10	0.27	0.27	0.73		
T11	1.0	1.0	1.0	0.27	
T12	1.0	1.0	1.0	1.0	
T13	1.0	1.0	1.0	1.0	

4.6 Component Count and Sizing

The number of components directly decide the size of EPG. The topologies along with the respective component count are listed in Table 4.7 where, PE switches, diodes, passive elements (R , L , C) and DC links are considered separately. A transformer is considered as a single component. Also, some topologies require more than one DC link. In such cases, the overall system of WEDM (see Fig. 1.7) requires the corresponding number of AC-DC converters. Hence, the *net* component count for the EPGs with multiple DC

links is more than that with a single DC link. This factor should be considered while selecting a particular topology, although it is not explicitly mentioned in Table 4.7.

Voltage stress of the active switches in a converter is an important parameter for the sizing of the PE switches [171]. Table 4.8 lists the voltage stress of the switches normalized with respect to the DC link voltage. It can be seen that the voltage stress of most of the switches in the converters is close to 1. In topology T5-a (Fig. 4.9) the voltage stress exceeds 1. This is because, when the switch Q_3 is OFF, the voltage across it is the summation of the DC-link voltage V_{in2} and the spark-voltage v_o i.e. $(V_{in2} + v_o)$. For the topologies with multiple DC-links the voltage stress is normalized against the largest DC-link voltage. For example for the topology T9 (Fig. 4.15), the values of DC-link voltages are as $V_{in1} = 30$ V, $V_{in2} = 5$ V, $V_{in3} = 100$ V. The values are normalized against the voltage V_{in3} .

Sizing of passive components i.e. inductors and capacitors is usually done by considering the allowable ripple content in current and voltage respectively. However, for EPGs, the output current and output voltage changes from 0 during t_{OFF} , to I_{ref} and V_{ref} during t_{ON} , respectively. Hence, besides the ripple around the reference values (V_{ref} and I_{ref}), the variation of current and voltage during the stage-transitions, should also be considered while sizing of the components.

Consider topology T6 (see Fig. 4.10(a)). Maximum change in current can occur when there is a transition from the pause stage to the sparking stage, i.e. when Q_2 is turned OFF. The inductor value can be determined using (4.21) which is derived by application of KVL to the loop: V_{in} - Q_1 - L_1 - D_4 -gap. It should be noted that, d_{Q1} is the duty ratio of switch Q_1 for *pause* stage and ΔI is the current ripple, which is almost equal to I_{ref} as current changes from 0 to I_{ref} .

$$L = \frac{(V_{in} - V_{Q1} - V_{Q2} - V_{D4})d_{Q1}T_{sw}}{\Delta I} \quad (4.21)$$

For dual-converter based topologies, it may not possible to exactly determine the load current for the converter VS. In such cases an engineering approximation can be made for the same. This point is explained with an example in Section 5.1

TABLE 4.9: Comparison of all the EPG topologies

	η (%)	CCI	COMP. COUNT	SUITABILITY
T1	35.14	1	3	No active devices are used, hence this is easy to implement. Consequently there is no control over the v_o , i_o , D_m , and T_m . It relies on resistance to limit i_o .
T2	9.91	1.5	3	D_m and T_m can be controlled by means of active PE switches. Otherwise, it is similar to T1.
T3	9.91	2.5	7	Similar to T2. The current capability is increased with use of multiple transistors. Here, t_{OFF} and number of transistors used at a time are controlled to avoid wire breakage in WEDM. Hence, this is suitable for WEDM. However, it uses resistances to limit the current and hence efficiency is poor.
T4	89.77	1.5	21	This topology is an extension of T3, but the ripple in i_o can be reduced with interleaving. Efficiency is quite on higher side due to ERS.
T5	27.14	2.5	7	No explicit L and C are used as filter elements, however it relies on L and C of the electrodes. MRR is improved by keeping ratio t_{OFF}/t_{ON} as low as possible. Therefore, it is more suitable for DEDM.
T6	72.54	2	9	Discharge current always starts from zero which results in low TEWR. Hence it is more suitable for DEDM.
T7	74.25	2	9	This topology is originally proposed for DEDM. As the output is bipolar, average output voltage is zero and hence minute cracks are prevented.
T8	85	4	7	AVP control scheme gives smooth transition from voltage control to current control. However, the scheme is complex to implement.
T9	29.08	5	13	RRC is controlled to achieve minimum TEWR - hence it is more suitable for DEDM. However, the control mechanism is complex and also three DC links are required. Here, RRC is controlled by adjusting DC link voltage
T10	44.76	4.5	11	Same as T9. Here, RRC is controlled by changing the combination of switches in operation and those not in operation.

	η (%)	CCI	Comp. Count	Suitability
T11	30.89	4.0	10	Here, two converters operate on a single DC link. It was originally proposed for drilling small holes in injection nozzles. However, it is suitable for both WEDM and DEDM.
T12	35.62	3.5	16	This is especially suitable for EDM where gap distance is more and hence high voltage is required for spark-initiation. However, the initiation voltage is decided by transformer turns ratio and no specific control scheme is suggested for this.
T13	87.28	3.5	11	This is originally proposed for portable onsite EDM. It is suitable for rough cutting applications where size of the machine is a constraint.

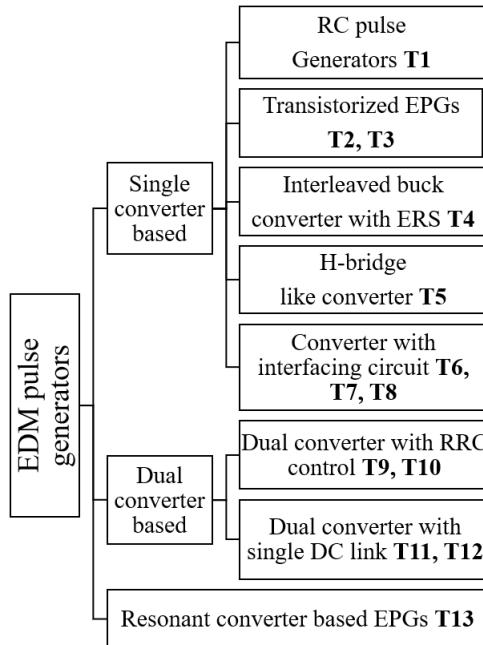


FIG. 4.30: Summary of topologies according to classification

4.7 Conclusion

EDM is a niche application that requires special class of pulse generators. However, they are not extensively covered in power electronics literature till date. This work has

covered 13 important topologies of EPGs, which are used either for DEDM or WEDM. Classification of these topologies is done into three categories, which can benefit modeling and design of EPGs from power electronics perspective. All the topologies are enlisted as per the classification in the tree diagram given in Fig. 4.30. The operation of these topologies is explained in detail for the three stages of operation of EDM process viz. pre-breakdown, sparking and pause. Simulation studies with MATLAB Simulink are reported with the EDM load of 10 A spark current and 1 kHz pulse repetition frequency.

Overall comparison of topologies from the perspective of efficiency, component count and control system complexity is summarized in Table 4.9. The last column (salient features and application) lists advantages and limitations of the topologies and also comments on suitability of the topology for a particular application.

This table can be used as a starting point during selection of a topology. For example, if the application demands high efficiency topology, it can be seen from the table that, topologies T4, T8, T13 are most suitable. On the contrary, for applications where TEWR and MRR are important compared to efficiency, topologies T6, T9 and T10 are more suitable. Also, Tables 4.6 and 4.9 together, can be used to modify a topology for a particular application. For example, topology T9 is originally proposed to achieve high MRR, by keeping ratio t_{OFF}/t_{ON} as low as possible. This fact can be employed for another topology e.g. topology T3. Sizing of components and control scheme for T3 can then be appropriately modified.

Chapter 5

EPG: Modeling and Efficiency Improvement

The details of modeling, design and efficiency improvement scheme for a specific pulse generator topology are discussed in this chapter. The discussion is supported by hardware results to verify the improvement in efficiency by the new scheme. This study can be used as a benchmark for design and hardware implementation of a particular pulse generator topology.

The EPG built in this work is for the miniature WEDM¹. Therefore, the EPG topology for this application should be such that all the electrical variables of WEDM process viz., V_{ref} , I_{ref} , D_m and T_m , can be controlled. Considering this, topology T11 (see Fig. 4.17 which is reproduced here in Fig. 5.1 for easy reference) is chosen, which is a dual-converter based pulsed generator proposed by Tastekin et al. [46]. This topology is originally proposed for micro-drilling of injection nozzles, an application wherein, the efficiency of the pulse generator is not a significant factor. Considering the present application, lesser efficiency of the pulse generator would add to the energy consumed in the wafer-manufacturing chain. Generic method to compute the efficiency is proposed

¹The work presented in this chapter is published as:

1. M. Kane, A. Khadse, H. Bahirat and S. V. Kulkarni, “Design and Control of Pulsed Voltage Supply for Electric Discharge Machining”, 2018 *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018*, pp. 1-6
2. M. M. Kane, A. Khadse, H. Chandwani, H. Bahirat and S. V. Kulkarni, “Modeling and Efficiency Improvement of a Pulse Generator for Wire Electric Discharge Machining,” in *Special issue on Pulsed Power Science and Technology, IEEE Transactions on Plasma Science*, vol. 48, no. 10, pp. 3350-3357, Oct. 2020

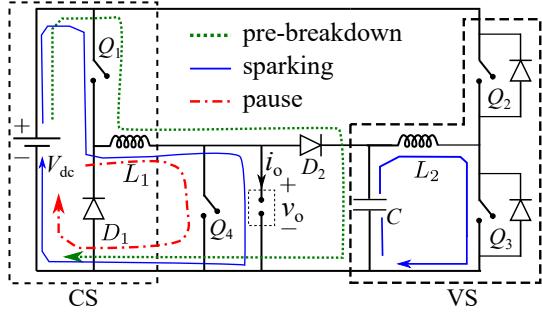


FIG. 5.1: Circuit diagram of T11 used for hardware implementation

in the previous chapter. In this chapter, an efficiency computation for this particular topology is illustrated in Section 5.2. With the original scheme proposed in [46], it is found that the efficiency is $\approx 31\%$ particularly for WEDM loads. Hence, a new scheme to improve the efficiency of converter to about 62% is proposed in Section 5.3 along with its advantages and limitations. Modeling of the converter in the frequency domain is discussed in detail with simulation results in Section 5.4.

5.1 Design of Pulse Generator

Operation of this topology is already explained in Section 4.3.2.2. Current through L_1 , Q_1 and D_1 is depicted in Fig. 5.2, where d_1T_m is the pre-breakdown stage, d_2T_m is the sparking stage, and d_3T_m is the pause stage. As denoted in Fig. 4.17(b), the current through L_1 flows through switch Q_4 during the pause stage. The output voltage of CS is equal to the drop across the ON state resistance of Q_4 . Therefore, the duty ratio of this stage is very small. Note that the duty ratio d_{CS} for the switch Q_1 is different for each stage as the feedback loop tries to maintain the current through L_1 at a constant value irrespective of the stage of operation. The duty ratio for the k^{th} stage is indicated by $d_{CS(k)}$. As the current at the output of the converter CS is constant throughout different stages of operation, the control-scheme which is proposed in the original paper [46] is called the constant current reference scheme (CCRS) in this work.

Sizing of L_1 , C , and L_2 needs to be done considering CCRS and the stage transitions of the pulse generator as pointed out in Section 4.6. The following target specifications are considered in this work: $V_{\text{ref}} = 100$ V, $I_{\text{ref}} = 10$ A, $f_{\text{sw}} = 50$ kHz, $f_m = 1$ kHz.

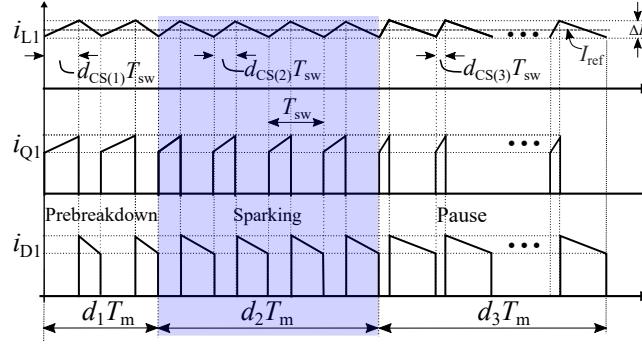


FIG. 5.2: Waveforms of i_{L1} , i_{Q1} , i_{D1}

5.1.1 Selection of L_1

Conventionally, the size of an inductor in a buck converter is decided by (5.1) [170], where V_o is the output voltage, D is the duty ratio of the switch, T_{sw} is the switching period, and ΔI is the allowed current ripple.

$$L = \frac{V_o(1 - D)T_{sw}}{\Delta I} \quad (5.1)$$

However, for converter CS, the output seen by the converter changes cyclically. Stage transition is like a step change in load and hence all the stage transitions need to be considered for the sizing of L_1 . It can be proved that the maximum ripple will occur in i_{L1} when switch Q_4 is turned OFF i.e. during the transition from the pause stage to the pre-breakdown stage, as shown in Fig. 5.3.

Two states are possible immediately after the transition: Q_1 is ON or Q_1 is OFF. When Q_1 is OFF, the current will flow through the loop $D_1-L_1-D_2-C$. If V_{D1} and V_{D2} are voltage drops in diodes D_1 and D_2 respectively, then L_1 can be calculated as

$$L_1 = \frac{(V_{D2} + V_{ref} + V_{D1})[1 - d_{CS(3)}]T_{sw}}{\Delta I} \quad (5.2)$$

Note that, here, $d_{CS(3)}$ is the duty ratio of Q_1 for the pause stage, as against a constant duty ratio D in (5.1) for a standard buck converter. Considering, $f_{sw} = 50$ kHz, $V_{ref} = 100$ V, and $\Delta I = 1$ A, $d_{CS(3)} = \frac{v_o(3)}{V_{in}} = 0.008$ (also explained in Section 5.2), $L_1 = 2$ mH is computed.

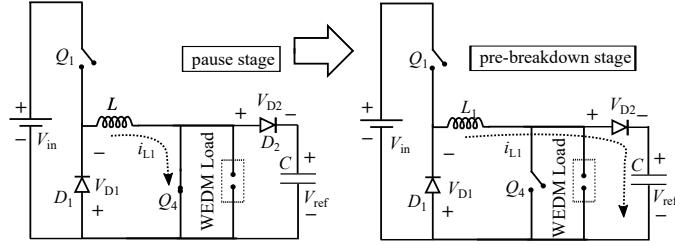


FIG. 5.3: Transfer of current from Q_4 to C

5.1.2 Selection of C

In the pause stage, the current flowing into C is almost zero. During the transition from the pause stage to the pre-breakdown stage, the current i_{L1} is diverted from Q_4 to C via D_2 . Hence, the current in capacitor C changes from near zero to I_{ref} . Consequently, there is a sudden inflow of additional charge $\Delta Q = I_{\text{ref}}d_{\text{CS}(3)}T_{\text{sw}}$. The voltage across C should have minimum ripple ΔV despite this change. The capacitor value can be calculated accordingly as follows:

$$C = \frac{\Delta Q}{\Delta V} = I_{\text{ref}} \frac{d_{\text{CS}(3)}T_{\text{sw}}}{\Delta V} \quad (5.3)$$

Considering $\Delta V = 2$ V, $C = 100 \mu\text{F}$ is selected.

5.1.3 Selection of L_2

There is no explicit resistive load connected at the output of the converter VS (Fig. 5.1). Due to the presence of diode D_2 , the current from L_2 cannot flow to the load. Therefore, ripple content in i_{L2} can be higher than that in i_{L1} . Considering $\Delta I = 2$ A and using (5.1), $L_2 = 47 \mu\text{H}$. A slightly oversized $L_2 = 100 \mu\text{H}$ is chosen as a conservative approach.

It should be noted that in the original paper by Tastekin et al. [46], the following values are selected for the components: $L_1 = 100 \text{ mH}$, $L_2 = 1.7 \text{ mH}$, $C = 960 \mu\text{F}$, for $V_{\text{ref}} = 200$ V, and $I_{\text{ref}} = 2.5$ A. It is clearly oversizing of the components as compared to the values selected here.

5.2 Efficiency Computation

The efficiency computation is already discussed in Section 4.4. The RMS or AVG values of current can be computed by an alternative way, i.e., by computing the *equivalent* duty ratios as explained below.

5.2.1 Computation of equivalent duty ratio

As the duty ratio of switch Q_1 changes in each cycle, as shown in Fig. 5.2, an equivalent duty ratio is given by (5.4).

$$EQ(d_{\text{CS}}) = d_1 \times d_{\text{CS}(1)} + d_2 \times d_{\text{CS}(2)} + d_3 \times d_{\text{CS}(3)} \quad (5.4)$$

$$\text{where, } d_{\text{CS}(k)} = \frac{v_{o(k)}}{V_{\text{dc}}} \quad \text{for } k = 1, 2, 3 \quad (5.5)$$

Here, $v_{o(1)} = V_{\text{ref}}$, $v_{o(2)} = I_{\text{ref}}R_{\text{sp}}$, and $v_{o(3)} = I_{\text{ref}}R_{\text{sw}}$ are the output voltages for the respective stages [178], where, R_{sp} is the WEDM-spark resistance and R_{sw} is ON-state resistance of the switch.

5.2.2 Calculation of RMS/average current

For the converter CS, expressions for the RMS/average values of currents can be derived from waveforms in Fig. 5.2 as follows:

$$\begin{aligned} \text{RMS}(i_{L1}) &= \sqrt{I_{\text{ref}}^2 + \frac{\Delta I^2}{12}} \\ \text{RMS}(i_{Q1}) &= \text{RMS}(i_{L1}) \times \sqrt{EQ(d_{\text{CS}})}, \quad \text{AVG}(i_{D1}) = I_{\text{ref}}(1 - EQ(d_{\text{CS}})) \end{aligned} \quad (5.6)$$

For the converter VS, as explained in Section 4.3.2.2, the current through L_2 mainly consists of current required to discharge capacitor C . As the pre-breakdown period $d_1 T_m \ll T_m$ and it is stochastic in nature [25], an exact expression for the RMS value of the current through L_2 and C would be quite complicated. Hence, taking a conservative approach, i_{L2}^{RMS} is taken as $1/10 \times i_{L1}^{\text{RMS}}$. The expressions for the current through various

elements of the converter VS are given in (5.7).

$$\begin{aligned} \text{RMS}(i_{L2}) &= 1/10 \times \text{RMS}(i_{L1}), & \text{RMS}(i_C) &= \text{RMS}(i_{L2}) \\ \text{RMS}(i_{Q2}) &= \text{RMS}(i_{L2})\sqrt{EQ(d_{VS})}, & \text{RMS}(i_{Q3}) &= \text{RMS}(i_{L2})\sqrt{1 - EQ(d_{VS})} \end{aligned} \quad (5.7)$$

RMS value of current through Q_4 is given by (5.8)

$$\text{RMS}(i_{Q4}) = \text{RMS}(i_{L1}) \times \sqrt{d_3} \quad (5.8)$$

5.2.3 Computation of losses

The efficiency computation is already explained in detail in Section 4.4. Ideally, the EPG topologies are implemented with MOSFET switches. A typical MOSFET for example, IRFP4137PbF, has $R_{sw} = 70 \text{ m}\Omega$, $t_r = 20 \text{ ns}$ and $t_f = 23 \text{ ns}$ [175]. Here, $I_{ref} = 10 \text{ A}$, $V_{ref} = 100 \text{ V}$, $V_{dc} = 105 \text{ V}$, $d_1 = 5\%$, $d_2 = 15\%$ and $d_3 = 80\%$. Following the above steps, the efficiency comes out to be 30.89%. The values used for the duty ratios d_1 , d_2 and d_3 are found to be appropriate for cutting silicon ingots from the experiments conducted earlier with BM400 as explained in Chapter 3.

However, the conduction and switching losses would be different for IGBTs and MOSFETs [174, 179]. The formulae to be used are given below.

$$P_{cond} = \begin{cases} [\text{RMS}(i_{sw})]^2 R_{sw} & \dots \text{for MOSFET} \\ V_{CEO} \times \text{AVG}(i_{sw}) + R_{CE}[\text{RMS}(i_{sw})]^2 & \dots \text{for IGBT} \end{cases} \quad (5.9)$$

where,
 R_{sw} : ON state resistance of MOSFET
 i_{sw} : current through the switch
 V_{CEO} : ON state zero-current collector emitter voltage
 R_{CE} : collector-emitter ON state resistance

$$P_{swch} = \begin{cases} 0.5V_{sw}^{\text{OFF}}I_{sw}^{\text{ON}}(t_r + t_f)f_{swm} & \dots \text{for MOSFET} \\ E_{sw} \left(\frac{i_{sw}^{\text{pk}}}{I_c^{\text{ref}}} \right)^{k_i} \left(\frac{V_{in}}{V_{CE}^{\text{ref}}} \right)^{k_v} \left[1 + T_c (T_j - T_j^{\text{ref}}) \right] f_{swm} & \dots \text{for IGBT} \end{cases} \quad (5.10)$$

where,	V_{sw}^{OFF} :	Voltage drop across switch in OFF state
	I_{sw}^{ON} :	ON state current through MOSFET
	t_r :	Rise time of current through the switch
	t_f :	Fall time of current through the switch
	f_{swm} :	Switching frequency for the switch
	E_{sw} :	$E_{ON} + E_{OFF}$ for IGBT, E_{rr} for reverse recovery diode
	i_{sw}^{pk} :	Peak current through the switch
	I_c^{ref} :	Reference collector current from the datasheet
	V_{CE}^{ref} :	Collector to emitter reference voltage from datasheet
	k_i :	Exponent of current dependency of losses for IGBT
	k_v :	Exponent of voltage dependency of losses for IGBT
	T_c :	Temperature coefficient of switching loss
	T_j :	Chip temperature
	T_j^{ref} :	Reference chip temperature

Originally, Tastekin et al. [46] have used the following specifications: $V_{in} = 200$ V, $V_{ref} = 180$ V and $I_{ref} = 1.5$ A, $f_{sw} = 10$ MHz, and $D_m = 50\%$. For these values, the efficiency can be computed to be equal to $\approx 2\%$. As stated before, the application considered in [46] is that of micro-drilling of injection nozzles, which is a type of die-sinking EDM. However, a much higher efficiency is expected in the case of WEDM, when it is an important component in the solar PV manufacturing chain. Hence, a novel scheme to improve efficiency is proposed as follows.

5.3 Efficiency Improvement by Pulsed Current Reference Scheme (PCRS)

From the operation of the converter it is clear that, current through L_1 , D_1 , Q_1 and Q_4 during the *pause* stage contributes to losses only and does no useful work. These losses can be reduced by using a new control scheme called as the pulsed current reference scheme (PCRS).

5.3.1 Description of PCRS

As the name suggests, the reference current is pulsed in nature, contrary to the constant reference in CCRS, as shown in Fig. 5.4. A reference value I_{ref1} is used for the sparking

stage and $I_{\text{ref}2}$ is used for the pause stage, such that, $I_{\text{ref}1}$ is the required sparking current (I_{spark}) and $I_{\text{ref}2} < I_{\text{ref}1}$. It should be noted that $I_{\text{ref}2}$ is not reduced to zero but some finite value. This is because i_{L1} needs to follow fast dynamics of this I_{ref} at a rate equal to or higher than f_m which is $\approx 1\text{-}10$ kHz.

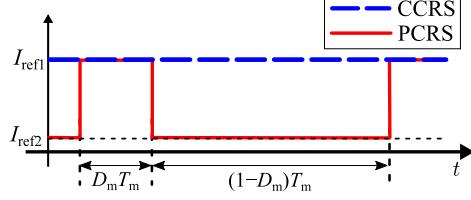


FIG. 5.4: Reference current for PCRS and CCRS

By neglecting transients during the change of stages, expressions for the RMS/average values of currents can be shown to be:

$$i_{L1}^{\text{RMS}} = \sqrt{\left(I_{\text{ref}1}^2 + \frac{\Delta I_1^2}{12}\right)(d_1 + d_2) + \left(I_{\text{ref}2}^2 + \frac{\Delta I_2^2}{12}\right)d_3} \quad (5.11)$$

$$\text{RMS}(i_{Q1}) = \sqrt{\left(I_{\text{ref}1}^2 + \frac{\Delta I_1^2}{12}\right) \times [d_{\text{CS}(1)}d_1 + d_{\text{CS}(2)}d_2] + \left(I_{\text{ref}2}^2 + \frac{\Delta I_2^2}{12}\right) \times d_{\text{CS}(3)}d_3} \quad (5.12)$$

$$\text{RMS}(i_{Q4}) = \sqrt{\left(I_{\text{ref}2}^2 + \frac{\Delta I_2^2}{12}\right) \times d_3} \quad (5.13)$$

$$\text{AVG}(i_{D1}) = I_{\text{ref}1}\{[1 - d_{\text{CS}(1)}]d_1 + [1 - d_{\text{CS}(2)}]d_2\} + I_{\text{ref}2}[1 - d_{\text{CS}(3)}]d_3 \quad (5.14)$$

Here, ΔI_1 is the current ripple during the sparking stage and ΔI_2 is current ripple during the pause stage. When (5.11)-(5.14) are compared with (5.6) and (5.8), it is clear that i_{L1}^{RMS} , i_{Q1}^{RMS} and i_{Q4}^{RMS} and i_{D1}^{AVG} are significantly less, if PCRS is used in place of CCRS, primarily because $I_{\text{ref}2} < I_{\text{ref}1}$. Hence, the power loss in Q_1 , D_1 , Q_4 and L_1 also decreases, resulting in increased efficiency.

The efficiencies for the two schemes are calculated analytically by the procedure outlined in Sections 4.4, 5.2 and the comparison is presented in Fig. 5.5. $I_{\text{ref}1} = 5$ A to 20 A, $I_{\text{ref}2} = 0.05 \times I_{\text{ref}1}$ and $D_m = 10\%$ to 80%. Note that the reference current during the pause stage is considered as 5% of that during the sparking stage as an engineering consideration for maximum improvement in efficiency. It is clear that for lower values of D_m , as used in WEDM [23], there is almost 30-40% improvement in efficiency irrespective of the sparking current.

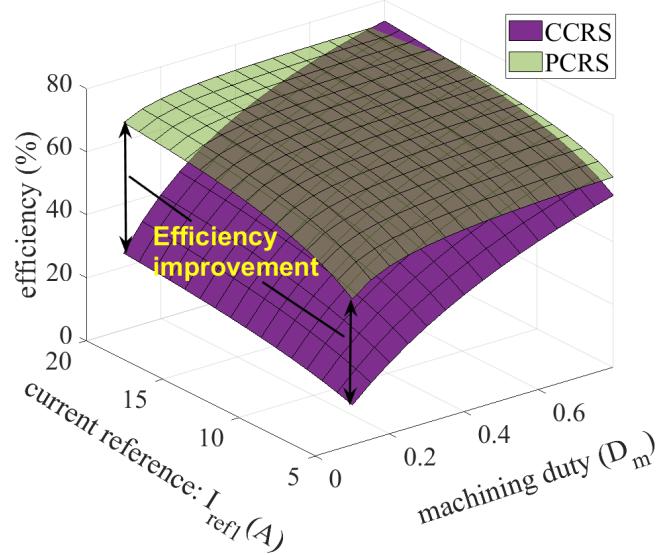


FIG. 5.5: Comparison of efficiency with CCRS and PCRS

5.3.2 Efficiency improvement vs allowable ripple in I_{spark}

Fig. 5.4 shows that, in PCRS, i_{L1} needs to follow fast dynamics. Sizing of inductor L_1 should be done as per this requirement. For the load specifications as considered in Chapter 4, i.e., $T_m = 1 \text{ ms}$ and $D_m = 20\%$, $D_m T_m = 200 \mu\text{s}$, which means that i_{L1} should change within only few 10s of μs . Therefore, (5.2) should be modified as:

$$L_1 = \frac{(V_{D2} + V_{\text{ref}} + V_{D1})[1 - d_{\text{CS}(3)}]T_{\text{sw}}}{I_{\text{ref1}} - I_{\text{ref2}}} \quad (5.15)$$

It can be noted that, the denominator is greater than that in (5.2). Hence, the size of L_1 is reduced, which will lead to increased ripple in i_{L1} . The ripple during the sparking stage is as given in (5.16).

$$\Delta I = \frac{(V_{\text{in}} - V_{\text{spark}})d_{\text{CS}(2)}T_{\text{sw}}}{L_1} \quad (5.16)$$

With $I_{\text{ref1}} = 10 \text{ A}$, $I_{\text{ref2}} = 0.5 \text{ A}$, and using (5.15), L_1 can be calculated to be $214 \mu\text{H}$. However, there is always a parasitic inductance of the wire and other connecting circuitry in WEDM [23]; hence, $L_1 = 100 \mu\text{H}$ is selected.

As an added advantage, when the size of L_1 is reduced, r_{L1} also reduces, resulting in further reduction of losses. From (5.15) and (5.16), it is clear that, when I_{ref2} is decreased, the size of L_1 also decreases and ripple in the sparking current increases. Also, from (5.11)-(5.14), when I_{ref2} is reduced, RMS/average values of currents decrease

resulting an increase in efficiency. Thus, there is a trade-off between increase in efficiency and decrease in ripple in sparking current.

5.3.3 Significance of high efficiency for wafer manufacturing

The efficiency of EDM or WEDM in general is being considered recently from the viewpoint of sustainable manufacturing [160, 180]. EPGs consume anywhere from 10% to 17% of energy consumed by the WEDM installation. The efficiency is crucial considering the application to wafer manufacturing especially if the wafers are used by the PV industry. As seen in Section 4.4.4, for many pulse generator topologies, the efficiency is very low $\approx 20\text{-}30\%$. If the efficiency is improved by 30%, there will be considerable saving in the energy bill of the plant. This would also contribute to reduction in overall production cost of solar wafers.

This is illustrated with a case study in Table 5.2. From the specifications of the load in Fig. 4.1, the power consumed over single pulse is very less $\approx 20\text{ W}$. The power consumed by load would increase if D_m increases. For the case study, the maximum value of $D_m = 70\%$ is considered. Therefore, maximum output power is 70 W. When WEDM would be employed for cutting wafers in the form of MWEDM, there should several hundred wires cutting an ingot simultaneously. The wafer production plant would also run for several hours per day. The minimum and maximum number of wafers produced per day is taken equal to the present production of multi-wire saw as given in [5]. It can be seen that, this would result in huge power consumption. When the efficiency is improved from 30% to 60% (as it is in this case), the energy consumption reduces to half of the original. Considering average energy cost of Rs. 9 per kWh, there would be average saving of Rs. 495,382.65/- per month as indicated in Table 5.2. Therefore, efficiency improvement of EPGs is certainly beneficial for ingot-slicing application, considered in this thesis.

5.4 Modeling and Simulation

To check the stability and to design a feedback controller, converter modeling is done in the frequency domain using averaged small signal transfer functions (SSTFs) [170]. It should be noted that there are two distinct switching frequencies in the circuit: the

TABLE 5.2: Potential savings by improvement in efficiency

Parameter	Minimum	Maximum	Mean
Slicing rate (mm/min) [18, 58, 181, 182]	0.4	1.67	1.04
Power (W)	20	70	45
Length of wafer/ingot (mm)	25	675	350
Time for one cut (minutes)	62.5	404.2	233.3
Wafer produced per day [5] ²	6500	16100	8238.72
Total energy required (kWh)	135.42	7592.07	3863.74
Energy cost (Rs./kWh)	9	9	
Cost per day (Rs./day)	1,218.75	68,328.59	34,773.67
Reduction in energy bill per day by improvement in efficiency (Rs.)	609.38	34164.30	17386.84
Saving per month (Rs.)	17,062.5	956,600.30	495,382.30

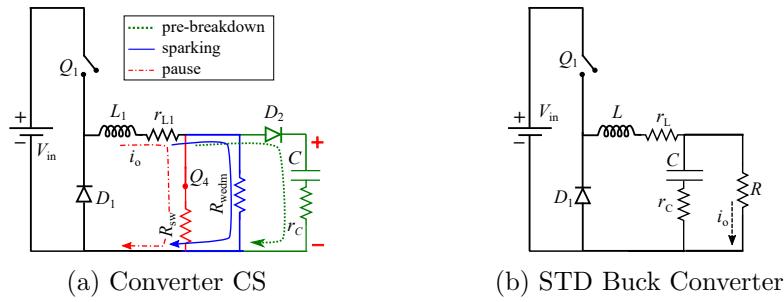


FIG. 5.6: Converter CS and STD buck converter

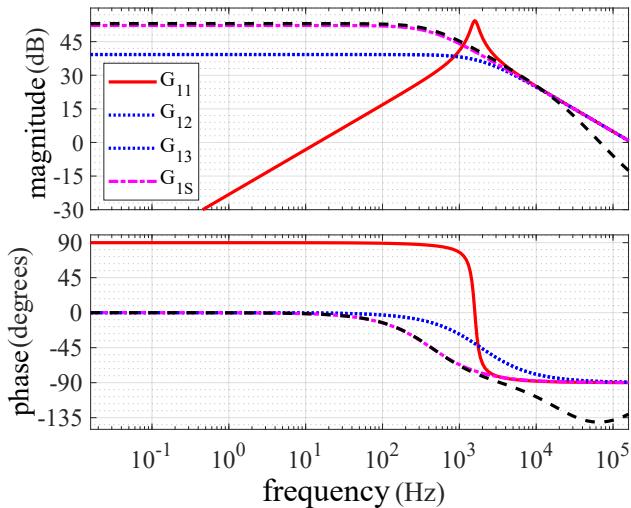
switches Q_1 , Q_2 , and Q_3 are controlled by feedback loops, with switching frequency of f_{sw} , and the switch Q_4 is switched at the frequency f_m . As $f_m \ll f_{\text{sw}}$, the converters CS and VS can be analyzed independent of each other. However, the load seen by the converters changes for each stage of operation. Hence, SSTFs are derived for each stage of the converter and they are compared with their standard (STD) counterparts. This technique can be applied to any pulse generator designed for the EDM load. For this section, subscript numbers are dropped from L_1 and L_2 for brevity of mathematical expressions. The frequency response plots are shown for $L_1 = 100 \mu\text{H}$, $L_2 = 15 \mu\text{H}$, and $C = 100 \mu\text{F}$, $r_{L1} = 10 \text{ m}\Omega$, $r_{L2} = 10 \text{ m}\Omega$, $r_C = 10 \text{ m}\Omega$.

5.4.1 Converter CS

The converter CS is similar to a STD buck converter, as shown in Fig. 5.6, except that there is no filter capacitor in the converter CS and the load changes cyclically as indicated in Fig. 5.6(a). Considering that the output of this converter is current i_{L1} , SSTF $G_1 = \widehat{i_{L1}}/\widehat{d_{\text{CS}}}$ is found for each stage of the converter CS (G_{11} , G_{12} , and G_{13} ,

TABLE 5.3: Transfer functions: converters CS, VS vis-à-vis STD counterparts

Converter CS and STD buck converter			
G_{11}	G_{12}	G_{13}	G_{1S}
$\frac{V_{in}s}{L(s^2 + \alpha_1 s + \omega_0^2)}$	$\frac{V_{in}}{L(s + \alpha_2)}$	$\frac{V_{in}}{L(s + \alpha_3)}$	$\frac{V_{in}\omega_0^2(r_C C s + 1)}{R[s^2 + (\alpha_1 + \frac{1}{CR})s + \omega_0^2]}$
Converter VS and STD two quadrant converter			
G_{21}	G_{22}	G_{2S}	
$\frac{V_{in}\omega_0^2(r_C C s + 1)}{s^2 + \alpha_1 s + \omega_0^2}$	$\frac{V_{in}\omega_0^2(r_C C s + 1)}{s^2 + \alpha_1 s + \omega_0^2}$	$\frac{V_{in}\omega_0^2(r_C C s + 1)}{s^2 + (\alpha_1 + \frac{1}{CR})s + \omega_0^2}$	
$\alpha_1 = \frac{r_C + r_L}{L}, \alpha_2 = \frac{R_{sp} + r_L}{L}, \omega_0^2 = \frac{1}{LC}, \alpha_3 = \frac{R_{sw} + r_L}{L}$			


 FIG. 5.7: Bode plot of G_{11} , G_{12} , G_{13} and G_{1S}

respectively), and it is compared with the SSTF of a STD buck converter (G_{1S}) in Table 5.3. Here, the hat: $\hat{\cdot}$ represents small variation in the signal. As there is only one energy storage element in the converter CS for the second and third stages of machining, G_{12} and G_{13} are first order transfer functions, whereas G_{1S} is a second order SSTF. Bode plots for the transfer functions are shown in Fig. 5.7. It can be noted that both G_{11} and G_{1S} are of second order. However, only G_{11} exhibits resonance because the damping provided by the load resistance is absent for this stage as against that in G_{1S} . The phase margins (PMs) are - $G_{11} : -90.1^\circ$, $G_{12} : 90.6^\circ$, $G_{13} : 90.1^\circ$, $G_{1S} : 53.8^\circ$. G_{11} crosses the unity gain i.e. 0 dB line twice and it has a negative PM. However, in such cases, the stability criterion based on the Nyquist plot should be invoked and a conclusion regarding stability cannot be drawn with the Bode plot alone [183]. As seen in Fig. 5.8,

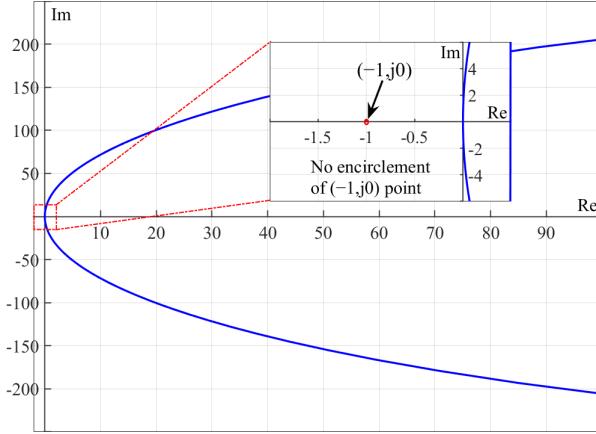


FIG. 5.8: Nyquist plot of G_{11}

Nyquist plot for G_{11} does not encircle $(-1, j0)$ point and hence the system is stable.

It can be noted that $\alpha_1 = 200$, $\alpha_2 = 10100$, $\alpha_3 = 800$ for the converter CS. α_1 is directly proportional to the damping factor whereas, α_2 and α_3 represent the magnitude of poles of the system. Therefore, it can be seen that the converter CS has its poles sufficiently negative.

5.4.2 Converter VS

The converter VS is similar to a STD two-quadrant converter (see Fig. 5.9). However, it has no explicit resistive load connected across its output. The SSTF $G_2 = \hat{v}_o/\hat{d}_{VS}$ for each stage of the converter VS (G_{21} , G_{22} , G_{23}) and STD two quadrant converter (G_{2S}) is given in Table 5.3, where d_{VS} represents duty ratio Q_2 . Note that, for the pre-breakdown stage, the converter VS is considered as a two-input one-output system with I_{ref} as the second input as shown in Fig. 5.9(a). Also, the topology of the converter VS is the same for stages 2 and 3. Hence, $G_{23} = G_{22}$.

Bode plots for the transfer functions are shown in Fig. 5.10: PMs are - $G_{22} : 15.76^\circ$, $G_{2S} : 17.75^\circ$. It can be noted that $\alpha_1 = 1330$. Here, the value is more compared to that for the converter CS because $L_2 \ll L_1$. Fig. 5.10 shows that the magnitude of the resonant peak is more for G_{22} as compared to that for G_{2S} , although the resonant frequencies are the same. This is expected because the magnitude is inversely proportional to the damping factor ζ [171], which is given for G_{22} and G_{2S} in (5.17).

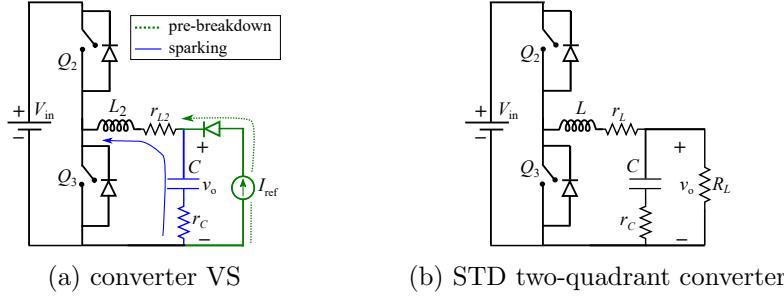


FIG. 5.9: Converter VS and STD two-quadrant converter

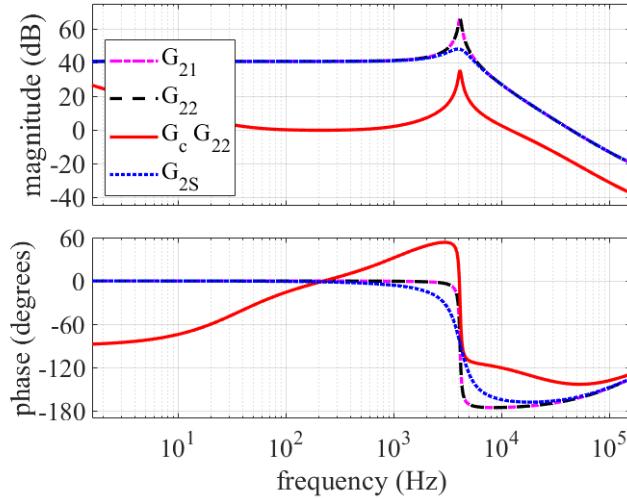


FIG. 5.10: Bode plot of G_{21} , G_{22} , $G_c \cdot G_{22}$ and G_{2S}

$$\zeta|_{G_{22}} = \frac{\alpha_1}{2\omega_0} \quad \text{and} \quad \zeta|_{G_{2S}} = \frac{\alpha_1}{2\omega_0} + \frac{\omega_0}{2R} \quad (5.17)$$

5.4.3 Compensator design

As the cutting happens during the second stage only, compensator design is done only for G_{12} and G_{22} . The necessity of a compensator can be seen from the low PMs of the transfer functions. Such low PMs will adversely affect the system damping as follows. The *closed loop* damping factor ζ is related to the open loop PM ϕ follows [171]:

$$\zeta = \frac{\sin \phi}{2\sqrt{\cos \phi}} \quad (5.18)$$

Fig. 5.11 shows plot of ϕ vs ζ , which clearly highlights that the damping is good if the PM is $60^\circ - 70^\circ$. On the other hand if the PM is very less, the system may exhibit

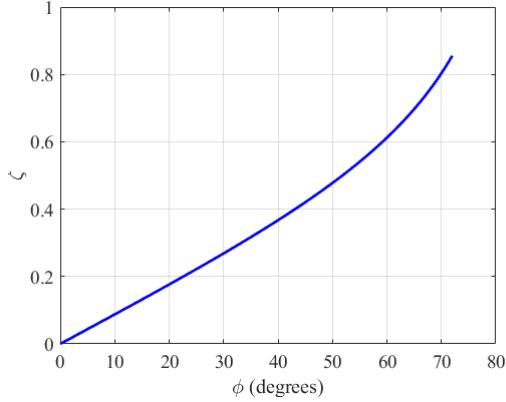


FIG. 5.11: Plot of phase margin ϕ vs damping factor ζ

an overshoot in its step response [183]. In the pulse generator, a step change in the load happens every cycle. Hence, if proper compensation is not provided for the PM, an overshoot can happen every cycle.

To avoid this, a lead-lag compensator G_c is designed and the Bode plot for the compensated system $G_c G_{22}$ is given in Fig. 5.10. It is evident that the phase margin is improved from 15.76° for G_{22} to 57.01° for the compensated system.

Transfer function G_{12} has PM = 90.6° , which provides sufficient damping for the system. Hence, a separate compensator is not designed for this converter and only P controller is used for it.

5.4.4 Simulation results

The simulation studies are done with MATLAB Simulink with both the schemes CCRS and PCRS. PCRS simulation is done for $I_{\text{ref}1} = 10$ A, $I_{\text{ref}2} = 0.5$ A and for *both* values of inductor $L_1 = 100 \mu\text{H}$ and 2 mH. For CCRS, $L_1 = 2$ mH and $L_2 = 100 \mu\text{H}$ is used. Fig. 5.12 shows i_{L1} and i_{Q4} to illustrate the necessity of resizing the inductor to implement PCRS. When $L_1 = 2$ mH, i_{L1} cannot follow the reference current in PCRS, which results in almost same waveforms of i_{L1} for both PCRS and CCRS. Consequently, the RMS value of the i_{L1} will be same, which means that the efficiency improvement cannot be obtained with $L_1 = 2$ mH.

Fig. 5.13 shows the load voltage and load current waveforms, which are the same except for the increased ripple of 1.8 A with $L_1 = 100 \mu\text{H}$ as compared to 0.1 A with $L_1 = 2$

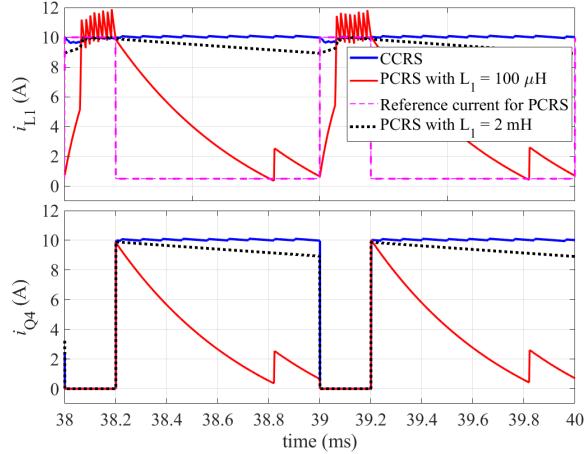


FIG. 5.12: Simulated waveforms of i_{L1} and i_{Q4}

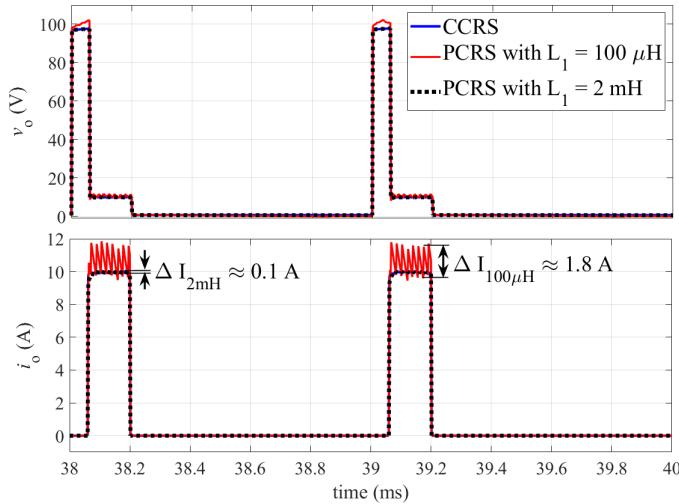


FIG. 5.13: Simulated waveforms of v_o and i_o

mH. The values of the ripple agree with those calculated by (5.16) with $V_{in} = 105$ V, $V_{spark} = 10$ V, $d_{CS(2)} = 0.095$ and $T_{sw} = 20 \mu\text{s}$. The experimental verification of the improvement in efficiency is given in next section.

5.5 Experimental Results

Semikron module SKM145GB066D is used for the legs Q_1-D_1 and Q_2-Q_3 . The circuit composed of Q_4-D_2 is realized using Semikron module SKM75GB12T4. Controller TMS320F28069 of Texas Instruments is used for employing the control schemes. The WEDM load is emulated using a resistor and MOSFET IRFP9243 in series, as illustrated by R_{sp} and Q_L in the inset of Fig. 5.14(a), which shows various parts of the hardware

setup. The load switch Q_L is turned ON with duty ratio d_2 and switching period T_m to emulate the sparking. For experiments, $f_{sw} = 50$ kHz, $D_m = 20\%$, $d_1 = 5\%$, $V_{ref} = 100$ V.

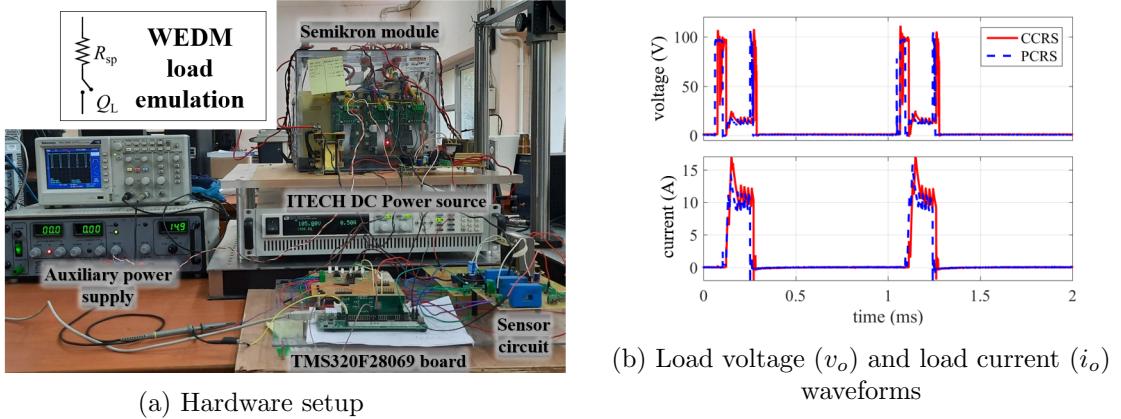


FIG. 5.14: Experimental setup and results

Efficiency computation is done by the procedure mentioned in Section 4.4. P_{cond} and P_{swch} are calculated by using (5.9) (5.10) along with the typical output characteristics given in the datasheets [184, 185]. Fig. 5.15 shows the plot of efficiency vs reference current (I_{ref}) for different values of reference voltage (V_{ref}) for CCRS. Both analytically computed values and experimentally obtained values are shown in the plot. It can be seen that the values agree with each other closely. The analytical values are slightly higher as various parasitic elements like inductances and resistances of wires are not considered in the analytical computations.

Fig. 5.14(b) shows a comparison of CCRS and PCRS with the load voltage and current waveforms for $I_{ref} = 10$ A in CCRS and $I_{ref1} = 10$ A, $I_{ref2} = 0.5$ A in PCRS. It can be observed that the new scheme does not change behavior of the output voltage and current waveforms significantly. The waveforms also match with the simulation output shown in Fig. 5.13. Experiments are also conducted for a range of values of V_{ref} and I_{ref} and the comparison efficiency obtained with the two schemes is shown in Fig. 5.16. The efficiency improvement is significant for higher values of I_{ref} . The MRR in WEDM is directly proportional to the sparking current [23]. Hence, for a constant D_m , it is clear that higher efficiency can be achieved with higher MRR as well. However, the surface roughness of the wafer needs to be investigated in such a case [23].

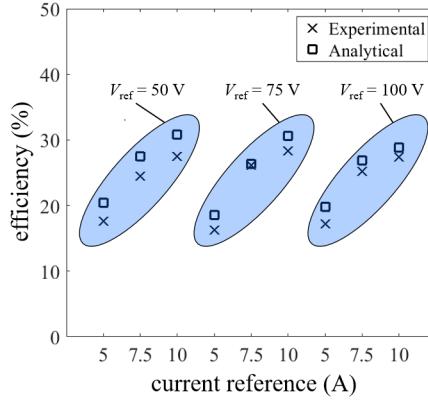


FIG. 5.15: Comparison of efficiencies obtained by analytical and experimental methods

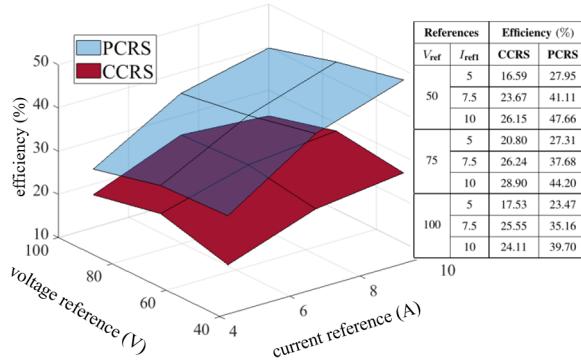


FIG. 5.16: Comparison of efficiencies: PCRS vs CCRS

Further, it can be seen that improvement in efficiency is more in the case of a lower values of V_{ref} . Therefore, this scheme is more suitable for cutting materials where the breakdown voltage for the gap between the wire and the workpiece is lower.

5.6 Conclusion

A pulse generator topology originally proposed for EDM based microdrilling is discussed at length considering issues in modeling and efficiency computation, which are not addressed in [46]. In particular, the following aspects are discussed considering the application of the topology for exploring optimum ways to cut silicon blocks with the mini-WEDM setup developed.

Appropriate sizing of passive components is presented considering the pulsed nature of the load, which can help to reduce the overall size of the pulse generator. It is shown by a detailed computation that when the constant current reference scheme, as proposed in [46] is used, the efficiency is about 31%. Lower the efficiency, more will be the losses in

the wafer manufacturing chain, which are of concern especially in solar industry. Hence, a new pulsed current reference scheme is proposed to improve the efficiency to about 62%. Resizing of some of the components is required for this scheme which is also useful for size reduction however, there is an increase in current ripple in the output.

Considering the spark load, a frequency domain modelling is illustrated with a separate transfer function for each stage of operation of WEDM. Experimental results are provided for the following specifications: 50-100 V open circuit voltage, 5-10 A current and 1 kHz pulse repetition frequency. The techniques discussed here can be utilized for other power electronics based EPGs designated for other applications as well.

Chapter 6

Development of Miniature WEDM

Design of customizable and miniature WED machine is explicated through description of design of various subsystems. Results of cutting of metal as well as semiconductor samples are also given at the end. The kerf loss in the semiconductor cut with the mini-WEDM is comparable to that cut with a commercial machine. The machine can be taken up for further development and commercialization.

6.1 Background

Commercial WED machines are large in size and costly. They usually occupy a size of at least $10 \times 10 \times 10$ ft³ and hence require a dedicated room. The cost of the machines ranges anywhere from INR 2 lakhs to 2 crores (\approx USD 25,000 to 300,000). The process parameters or settings cannot be varied beyond the ratings prescribed by the makers of the machine. For example, when the dielectric fluid was changed in the BM400 WEDM (cf. Chapter 3) available at Machine Tools Lab, IIT Bombay, it was found that the workbench and various parts of dielectric tank suffered corrosion. Such incidents add to the maintenance time and cost of the machine and puts the complete capital investment at stake.

It is already stated that the WEDM is a complex system with many interconnected subsystems as shown in Fig. 1.7. Therefore, if one wishes to apply say a higher V_{OC} or

to use a bipolar pulse generator in place of a unipolar one, it is not easy to retrofit a new EPG with the existing system. It would incur both huge cost and time. This puts a limit on the variation of the electrical parameters viz., voltage, current, polarity, pulse ON time, pulse repetition frequency, etc.

The limits to tweak the existing systems in commercial WEDM has two repercussions:

1. **Restrictions on the study of physics of the process:** The physics of WEDM is not clearly understood till date. In order to investigate the physics a researcher might be interested to use a variation which is very difficult in a commercial machine. For example, if the commercial machine can apply only peak current control, the effect of hysteresis current control cannot be seen on the spark behavior.

Further, it is also difficult to probe the spark location in the commercial WEDM machines, because, the sensors cannot be placed near the spark due to high temperature and the dielectric fluid flow.

2. **Limits to find optimum set of process parameters:** For any new material, an optimum set of process parameters is usually found by experimental design. However, the factor space of the design of experiments is limited by the discrete levels available. One cannot vary the parameters on a continuous scale to get an optimum set of parameters. Also, one cannot set a parameter beyond the maximum and minimum level given by the machine maker.

A customizable WEDM can alleviate these limitations and can serve two purposes: (a) To understand the physics of the process and (b) To vary the process parameters so that an optimum set of parameters can be found out. With this view, a fully customizable miniature WEDM (mini-WEDM) machine is designed and fabricated. In this chapter¹, the design and initial experimental results are described.

¹Some portion of this chapter is accepted for publication as:
M. M. Kane, Kamlesh Joshi, Nitin Tiwari, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, "Experiments with Miniature Wire EDM for Silicon," in *Procedia CIRP*, an Elsevier journal, affiliated with CIRP, The International Academy for Production Engineering), Vol. 95, 2020, pp. 296-301, ISSN 2212-8271.

Also, a **patent** is applied for the machine:

Makarand M. Kane, Kamlesh Joshi, Nitin Tiwari, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, "Customizable Miniature Wire Electric Discharge Machine", Indian patent, Appl. No. 202021032434, 29 Jul, 2020

TABLE 6.1: Target specifications for the mini-WEDM

Parameter	Value
Workpiece dimension	10 cm × 10 cm × 3.5 cm
Max. value of pulsed voltage	200 V
Max. pulse repetition frequency	10 kHz
Max. value of pulsed current	20 A
Overall size of machine	120 cm × 60 cm × 60 cm
Orientation of cutting wire	Vertical
Minimum step of CNC motion	1 μ m

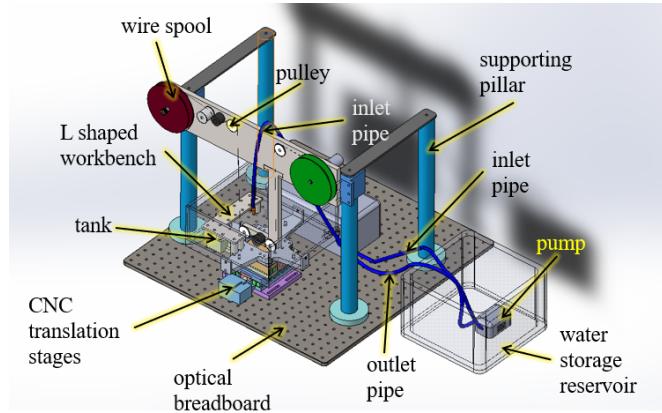


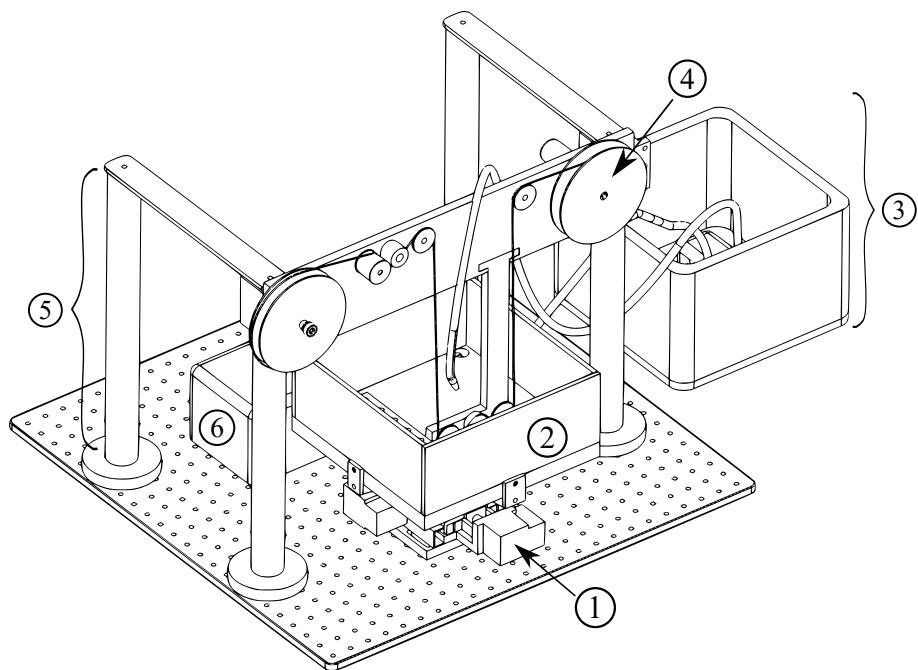
FIG. 6.1: Wire-feed system, CNC and tank + workbench system

6.2 Design: Targets and Process

The design targets were fixed as given in Table 6.1, after careful consideration of various options. For example, horizontal orientation of wire was also considered as an alternative. However, if the wire is horizontal, the workpiece would be required to move in vertical direction. This would require 2D translation stages to be mounted perpendicular to the ground, which would make design further complicated. Hence, the orientation of wire was considered to be vertical. It is difficult to elucidate all such considerations and permutations happened *during* the design process. However, some points are mentioned in the following sections. Fig. 6.1 shows a 3D colored drawing of the designed system. Figs. 6.2 and 6.3 show the isometric view of the setup. These figures are shown here to clarify the position and function of each subsystem in the complete system.

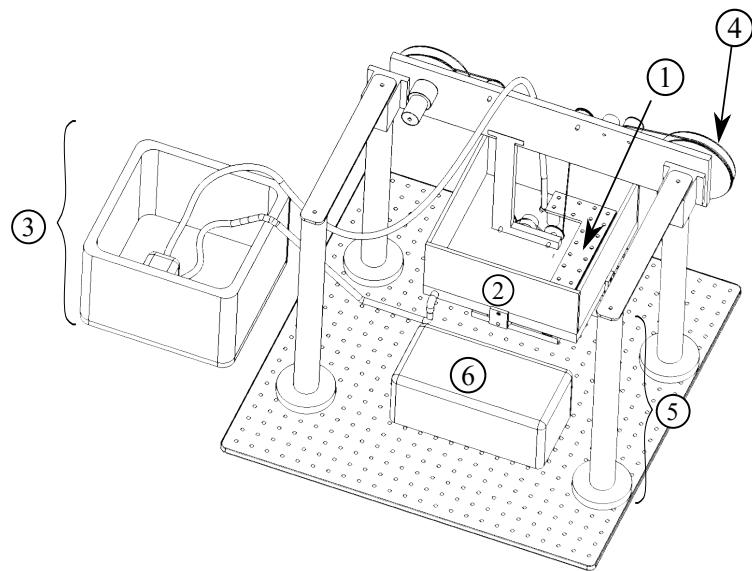
6.3 Design of Subsystems

There are five major subsystems in the mini-WEDM:



1: translation stages	4: wire feed subsystem
2: tank + workbench	5: support structure for 4
3: dielectric system	6: electronic control system

FIG. 6.2: Complete mechanical assembly: view 1



1: workbench	4: wire feed subsystem
2: tank	5: support structure for 4
3: dielectric system	6: electronic control system

FIG. 6.3: Complete mechanical assembly: view 2

TABLE 6.2: Specifications of the Holmarc MTS 90-115 translation stages

Parameter	Value
Maximum travel	5 cm
Least count of CNC travel	0.125 μm
Axes of motion	x and y



FIG. 6.4: Holmarc motorized translation stages 90-115 (image source [187])

1. CNC subsystem
2. Workbench and dielectric tank
3. Wire feed mechanism
4. Dielectric circulation system
5. Pulse generator

Design of each subsystem is described in the following subsections.

6.3.1 CNC translation stages

CNC stands for Computer Numeric Control, which is a computerized motion control of the workpiece with respect to the tool [186]. Considering targets in Table 6.1, Motorized Translation stages “MTS 90-115” from Holmarc OptoMechatronics Pvt. Ltd. are selected. Specifications of the translation stages are given in Table 6.2 and its photo is shown in Fig. 6.4. The stages are controlled by a dedicated software (from Holmarc Mechatronics Pvt. Ltd.) which can accept the external trigger pulses. In this work, the trigger pulses are given by TMS320F28069 microcontroller used to control the pulse generator.

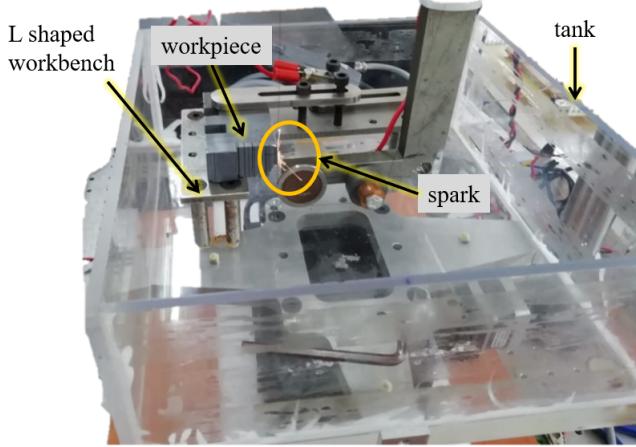


FIG. 6.5: L-shaped workbench inside the tank

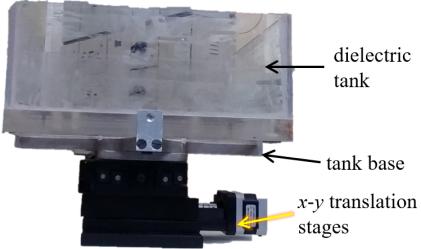


FIG. 6.6: Tank and CNC system

6.3.2 Workbench and dielectric-tank

The tank is made of acrylic and has dimensions $250 \times 250 \times 115$ mm, enumerated as “2” in Fig. 6.3. An L-shaped metallic workbench (enumerated as “1” in Fig. 6.3) is mounted inside the tank. Fig. 6.5 shows the L-shaped workbench is mounted inside the tank along with a silicon workpiece fixed on the workbench. The tank is mounted on the translation stages with tank-base as shown in Fig. 6.6.

6.3.3 Wire-feed mechanism

Any wire-feed mechanism consists of one or more wire-storage spool/drum [24]. In this work, two wire-spools are designed, one would act as unwinding spool and the other spool will wind the wire, after it passes through the spark area. Initial design consisted of two motorized spools. However, this would make the control system more complex as precise control of two motors would be involved. Therefore, a design consisting of single motorized spool was designed. In order to validate the concept, a dummy system



FIG. 6.7: Dummy wire-feed system for validation of concept

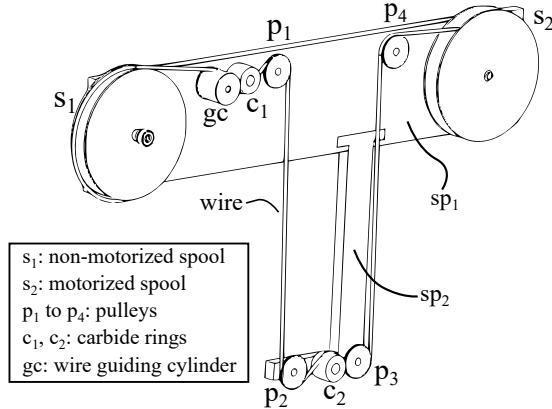


FIG. 6.8: Wire feed system

was designed as shown in Fig. 6.7. After successful operation of the system, the actual system was designed and fabricated.

The finalized design of wire feed system is shown in Fig. 6.8. It consists of a non-motorized spool (s₁), a motorized spool (s₂), four pulleys (p₁ through p₄), two carbide rings (c₁ and c₂), and a wire guiding cylinder (g_c). When the motor is turned ON at a pre-set voltage, it runs at a pre-determined speed. As a result, the wire unwinds from s₁; it passes through path g_c-c₁-p₁-p₂-c₂-p₃-p₄ and winds onto s₂. The carbide rings are used to provide an electrical terminal connection to the wire as shown in Fig. 6.9. It should be noted that two carbide rings are provided: one at the top and another at the bottom, to which negative terminal of the pulse generator is connected. This is done to minimise the inductance and to equalise the forces acting on the wire [23].

The supporting structure for the wire-feed system consists of four pillars as shown in Fig. 6.2 and two supporting structures sp₁ and sp₂, as marked in Fig. 6.8. Pulleys p₁ and p₄, spools s₁ and s₂, carbide brush c₁, and guiding cylinder g_c are mounted on sp₁. The pulley p₂, carbide rings c₂ and c₃ are mounted on sp₂. Both sp₁ and sp₂ are made of mild steel because the structures might be subject to vibration. Molybdenum wire of 180 μm OD is used in this setup.

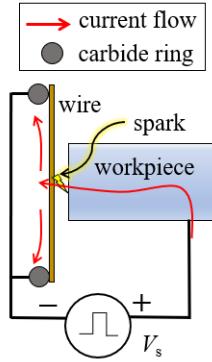


FIG. 6.9: Schematic of terminal connection to carbide ring

6.3.4 Dielectric circulation system

The dielectric circulation system is shown in Figs. 6.1 to 6.3. It provides flushing of dielectric fluid in the gap between the wire and the workpiece. It is necessary mainly (a) to remove the swarf (debris particles), which can otherwise bridge the gap and hence short circuit the electrodes and (b) to provide cooling. The Khaitan Aqua 60, 220 V, 50 Hz, 18 W pump is used for the fluid circulation. The dielectric fluid is circulated in the following path: tank-outlet pipe-water reservoir-pump-inlet pipe-nozzle-spark gap-tank. Presently, deionized water is used as a dielectric fluid, with relative dielectric constant or electric permittivity $\epsilon_r = 80$ [188]. However, it should be noted that the fluid can be changed in case one wants to use a different dielectric for research purpose.

6.3.5 Pulse generator

A pulse generator is necessary to apply voltage pulses across the gap between the wire and the workpiece electrode. The design, modeling and control of the pulse generator is already explained in Chapter 5. It should be noted that any other circuit topology can be easily connected to provide the necessary voltage pulses. This facility enables users to experiment with various types of supply voltages like sinusoidal, pulsed DC, trapezoidal, etc.

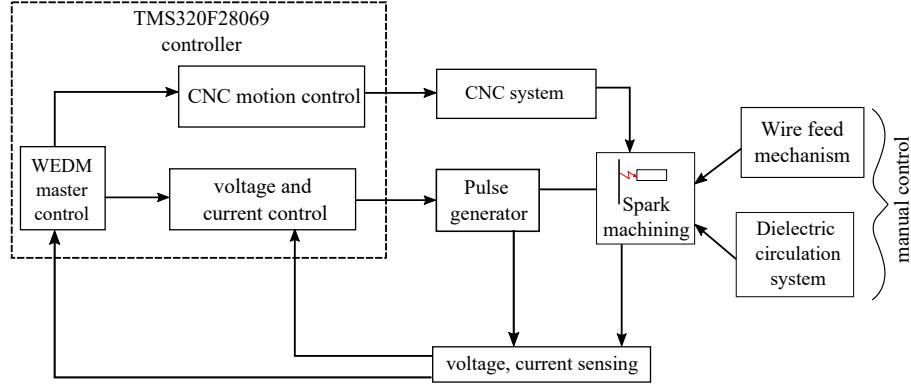


FIG. 6.10: Schematic of implemented WEDM control system

6.4 Control of Mini-WEDM

The commercial WEDM systems implement at least four major control systems (as indicated in Fig. 1.7):

1. CNC mechanism to control motion of workpiece
2. EPG voltage and current control system
3. Dielectric circulation control
4. Wire feed control

However, in the mini-WEDM setup, two control systems: EPG voltage and current control and CNC control are implemented on the microcontroller as shown in Fig. 6.10. The manual control is provided for the other two systems: wire speed control and dielectric flow control. The control systems are described below:

1. **EPG voltage and current control:** The voltage and current control system for EPG is already explained in Chapter 5.
2. **CNC motion control:** Block diagram for this control system is given in Fig. 6.11 and the algorithm flowchart is given in Fig. 6.12. Here, x is position of the tool electrode. First, the gap voltage is sensed and fed to a low pass filter. The filter output V_{filt} is compared with the servo voltage (V_{servo}). The servo voltage is set equal to value of averaged/filtered value of ideal gap voltage. From Fig. 1.6, ideal value of V_{servo} is given by

$$V_{\text{servo}} = V_{\text{ref}}d_1 + V_{\text{spark}}d_2 + 0 \quad (6.1)$$

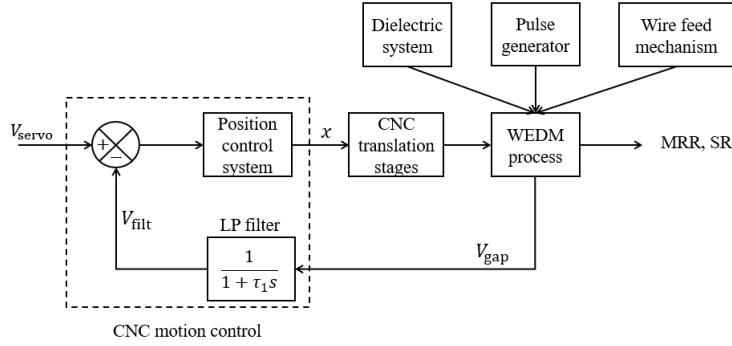


FIG. 6.11: CNC motion control system

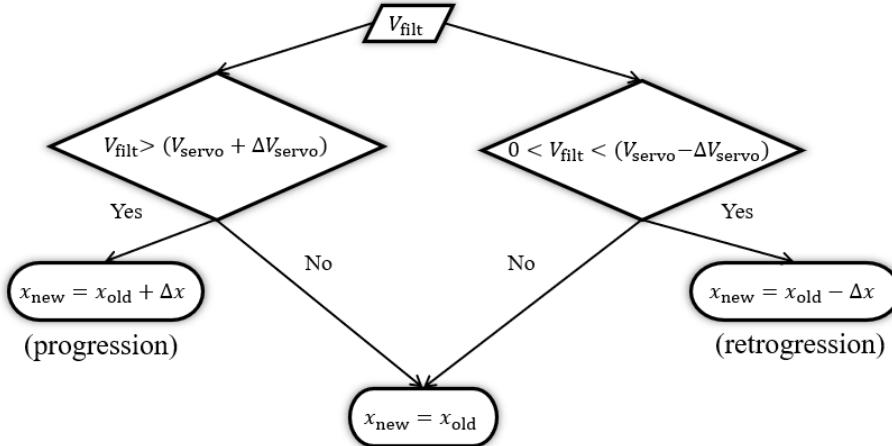


FIG. 6.12: Flowchart for position control algorithm of tool electrode

Typical value of the voltage V_{spark} is 35 to 45 V [24]. For the mini-WEDM the value is determined by experimentation.

The decision to advance the workpiece (denoted by *progression* step in Fig. 6.12) or to retract (denoted by *retrogression* step in Fig. 6.12) the workpiece is taken depending on the comparison of V_{filt} and V_{servo} . When ‘open circuit’ is detected, the workpiece is advanced so that the gap length reduces and the sparking is again initiated. When the ‘sparking’ state is detected, the position of the workpiece is not changed. When the ‘short circuit’ is detected, the workpiece is retracted. The three cases of the algorithm are explained in Table 6.3.

TABLE 6.3: Cases in position control algorithm for CNC control

Condition	Gap state	Decision
$V_{\text{filt}} > V_{\text{servo}} + \Delta V_{\text{servo}}$	Open Circuit	$x_{\text{new}} = x_{\text{old}} + \Delta x$
$V_{\text{filt}} < V_{\text{servo}} - \Delta V_{\text{servo}}$	Short Circuit	$x_{\text{new}} = x_{\text{old}} - \Delta x$
$V_{\text{filt}} \in (V_{\text{servo}} - \Delta V_{\text{servo}}, V_{\text{servo}} + \Delta V_{\text{servo}})$	Sparking	$x_{\text{new}} = x_{\text{old}}$

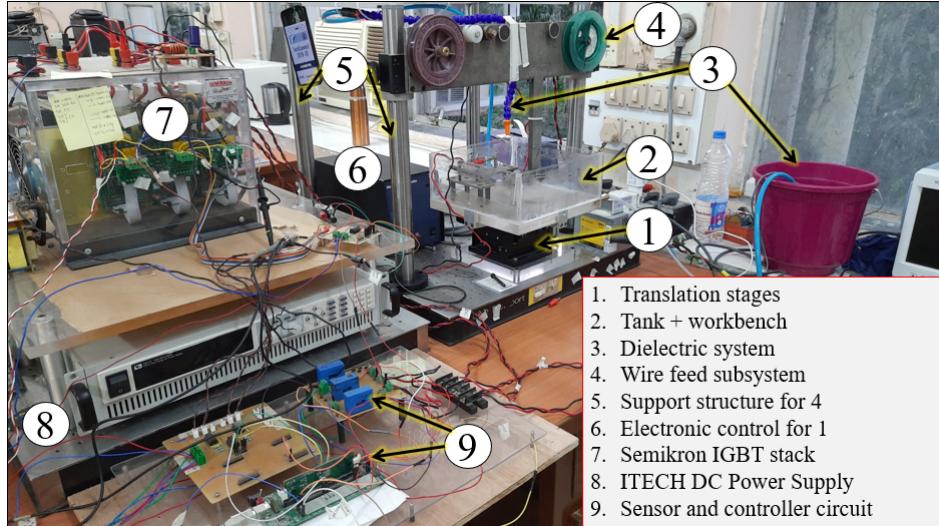


FIG. 6.13: Complete mini-WEDM setup

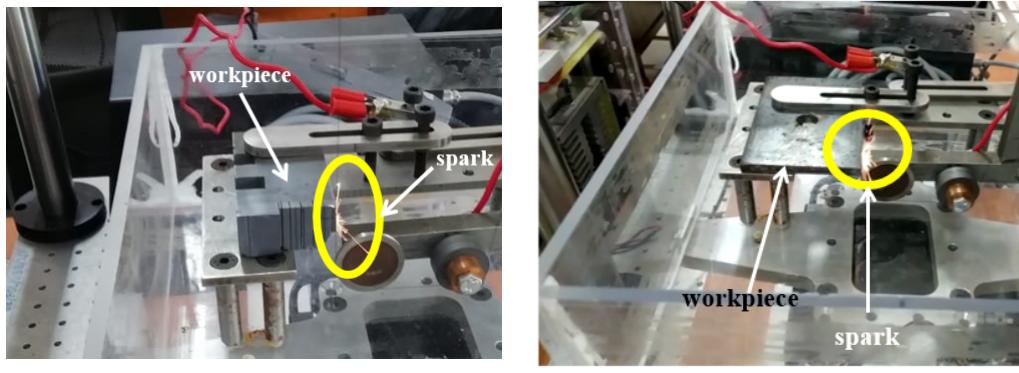
3. **Wire speed control:** In the present system, there is a spring washer along with a nut provided at the non-motorized spool s_1 . This provides the breaking torque (T_b). The speed of the motor is decided by the voltage supplied to the motor by its power supply (V_m). Therefore, by adjusting the two parameters i.e. T_b and V_m , the wire speed can be changed manually.
4. **Dielectric flow control:** The flow rate of deionized water can be controlled by changing the input voltage to the pump used to circulate the water.

6.5 Experimental Results

The image of complete setup is given in Fig. 6.13, it can be seen that the setup is fabricated as per the conceived design in Figs. 6.1-6.3.

6.5.1 Dry WEDM

Initially, these experiments are conducted without the dielectric system in operation and hence it is referred to as dry WEDM [17]. The images of sparks taken while cutting the silicon and steel workpiece without the dielectric are shown in Fig. 6.14. The sparks in the case of steel are seen to be brighter than that for silicon. This observation agrees with the observation made with BM400. The reference or open circuit voltage is set to 75 V, the reference current is set to 7.5 A, and the pulse repetition frequency to 1 kHz.



(a) Silicon

(b) Steel

FIG. 6.14: Spark while cutting without dielectric

Fig. 6.15 shows voltage and current pulse train recorded for cutting without the dielectric. Three main categories of pulses can be observed: (a) open (b) near-short and (c) sparking. The ratio of duration of open pulses to the total duration is $0.009/0.22 \approx 3.8\%$. This is satisfactory performance indicating that only 3.8% of pulses are ‘open’ and the remaining 96.2% pulses are utilized for cutting.

If enlarged version of the pulses are observed, they can be further categorized into four types as shown in Fig. 6.16(a): (a) Open (b) Spark-1 (c) Spark-2 and (d) Near short. The open pulse is observed when the dielectric in the inter-electrode gap fails to break down. The spark current is zero during this stage. This type of pulse gives little information about the nature of the spark.

The feedback loop implemented in the controller tries to maintain the current at $I_{ref} = 7.5$ A, however, the current may not remain constant throughout the sparking stage. This is due to the fact that the equivalent impedance of the WEDM-load as seen by the pulse generator is variable for each pulse because of the irregularities in the spark gap. Hence, two types of sparking pulses are observed: *Spark-1* and *Spark-2*. In *Spark-1*, there is significant overshoot in the current value and in *Spark-2*, there is minimal overshoot in current. The overshoot is expected because $L_1 = 100 \mu\text{H}$ is used. However, the variation in the overshoot value may occur due to various reasons such as presence of debris, reduced length of spark gap due to vibrations of wire, non-uniform wire diameter etc. The overshoot can increase surface roughness of the workpiece. The last pulse type is near short circuit as shown in Fig. 6.16(a). It occurs when ignition delay time is more than t_{ON} and in such cases current overshoots twice as large as the reference value of

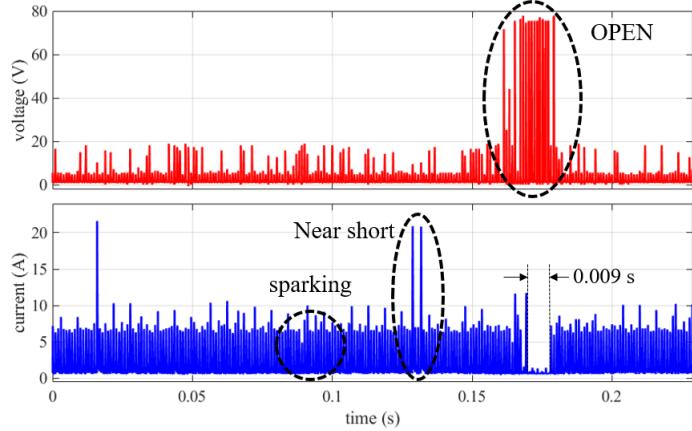


FIG. 6.15: Pulse train of voltage and current with dry WEDM for steel

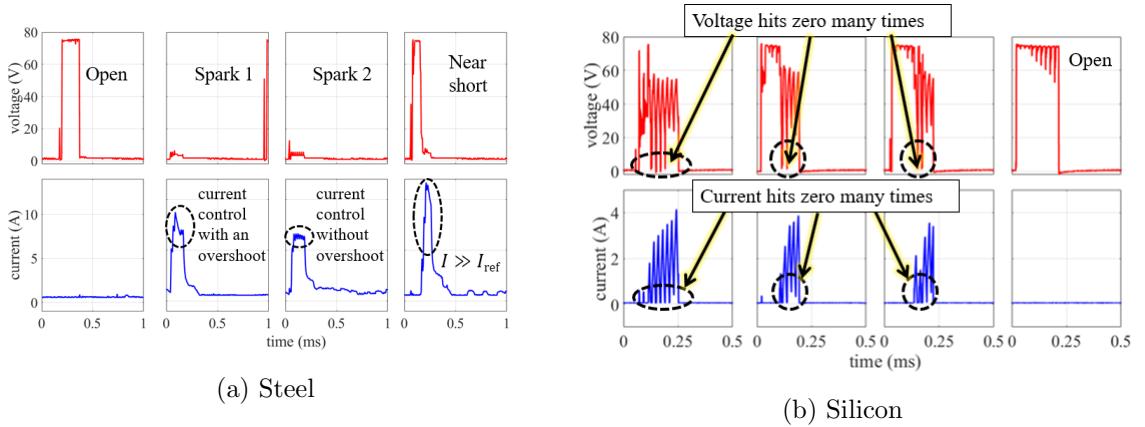


FIG. 6.16: Major types of voltage and current waveforms in dry WEDM

current. The term near short is assigned to distinguish it from a sustained short circuit. An algorithm implemented in the controller avoids sustained short circuit.

Voltage and current waveforms while cutting silicon workpiece are shown in Fig. 6.16(b). It is seen that the voltage and current drop to zero several times during a single pulse. This is mainly because the swarf or debris particles which remain in the gap since the dielectric flushing is absent [107]. The spark voltage is higher for silicon (≈ 50 V) than that for steel (≈ 5 V). This agrees with the results obtained earlier with a commercial WEDM noted in the Chapter 3.

The waveforms tell us that dry WEDM is not effective because the current cannot follow the reference accurately. Also, the debris in the gap can cause several small-duration short circuits during the sparking stage.

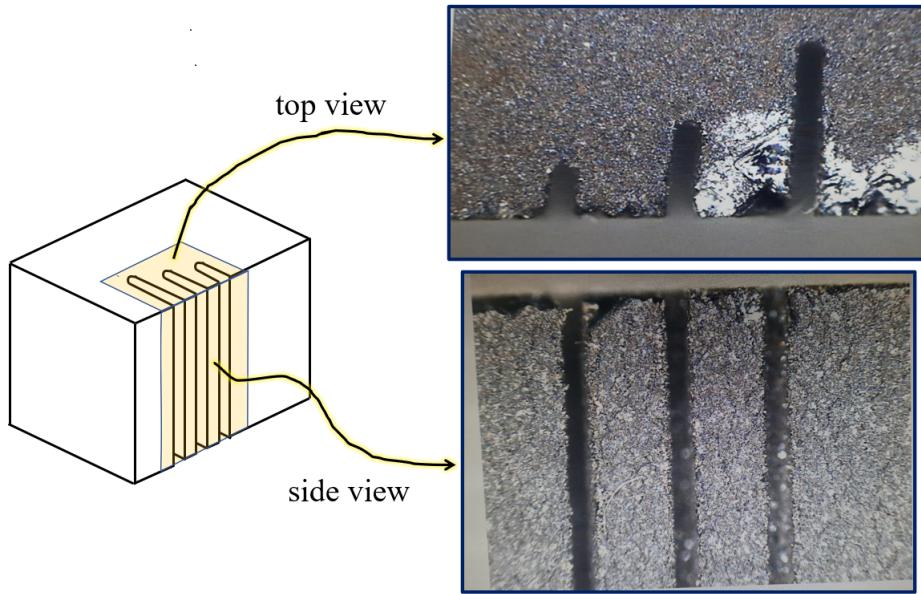


FIG. 6.17: Cut part schematic view and enlarged view obtained by Rapid Eye Microscope

6.5.2 Cutting with dielectric

Silicon workpiece of size $10\text{ cm} \times 2.2\text{ cm} \times 5\text{ cm}$ was cut using the mini-WEDM. Three distinct cuts are made on the side of the workpiece which are schematically shown in Fig. 6.17. An open circuit voltage reference was set to 50 V and current reference was set to 5 A.

6.5.2.1 Voltage and current waveforms

The voltage and current waveforms are recorded with Yokogawa DL850E Scope corder and Yokogawa 701933 current probe and they are given in Fig. 6.18. We observe mainly two types of pulses: (a) Open (b) Sparking. The open pulse is observed when the dielectric in the inter-electrode gap fails to break down. The spark current is zero during this stage. This type of pulse gives little information about the nature of the spark.

The pulses can be categorized as ‘sparking’ pulses when there is some non-zero current recorded as shown in Fig. 6.18. It should be noted that if the sparking current exceeds a certain limit the pulse generator is shut down i.e., triggering pulses for the IGBTs are removed. This avoids the near-short pulses which were recorded with dry-WEDM. As stated in the previous section, the sparking pulses can be categorized further into:

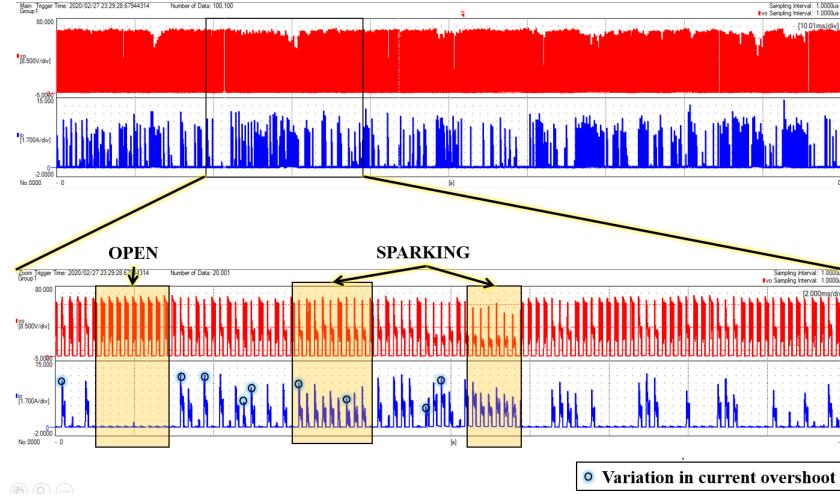


FIG. 6.18: Waveform of spark voltage and current

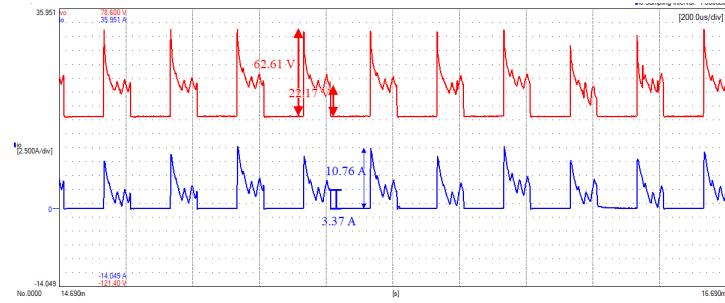


FIG. 6.19: Enlarged version of spark voltage and current pulses for silicon

spark-1 and sparking-2. However, due to variation in the overshoot magnitude of current overshoot is (indicated in Fig. 6.18), this categorization is not done. The variation can be attributed to any one of the several phenomena: (a) There is no accurate control over wire tension, which leads to wire-vibrations. Therefore, the gap-length varies for each pulse, which changes the dynamic impedance of the gap as seen by the pulse generator. (b) The flow rate of the liquid may also be varying. Also due to the control algorithm implemented, the gap conditions would vary a little for each pulse. (c) The workpiece is not exactly at the center of the wire location. Therefore, the current in the wire might divide unequally between the two sections of the wire. This can cause further non-uniformity in the gap environment.

It can be seen that the current waveform is almost uniform for several consecutive pulses as shown in Fig. 6.19. The difference in magnitude of overshoots is also seen in Fig. 6.20, where the overshoot ranges from 6.09 A to 13.21 A. This implies that the current control needs to be improved. This is also associated with lower value of inductor in the pulse generator. This is explained in detail in Chapter 5.

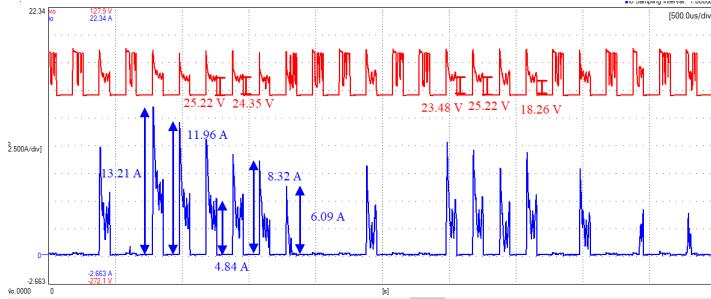


FIG. 6.20: Difference in magnitudes of overshoots during machining

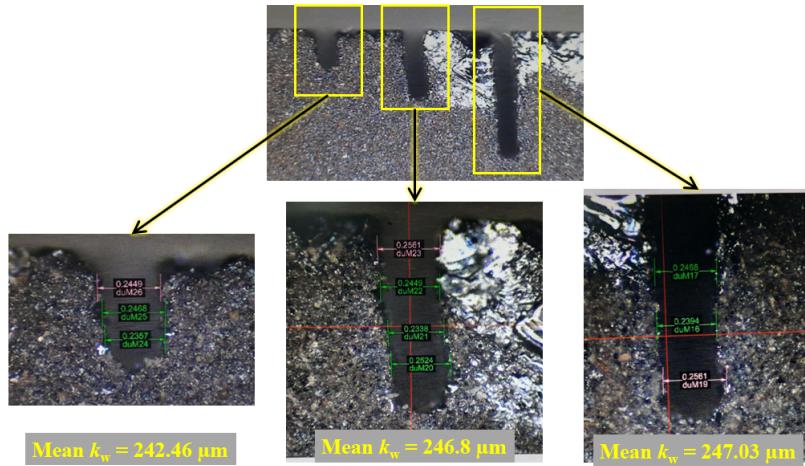


FIG. 6.21: Kerf loss measured using RapidEye Microscope

6.5.2.2 Kerf loss analysis

To measure the kerf loss, the cut block of silicon is observed with RapidEye Microscope and the resulting images are shown in Fig. 6.21. It is seen that the kerf width is about 240-250 μm . This means that the gap between the workpiece and the wire, i.e. the maximum amplitude of wire-vibrations is of the order of 30-35 μm . Miyake et al. [189] have stated that for an acceptable surface quality the gap width needs to be of the order of 20 μm . This can be achieved by better tension control and better dielectric circulation system.

Comparison with the commercial machine: BM400

The kerf loss is comparable to the one obtained by the commercial machine BM400 mentioned in Chapter 3. The kerf loss readings for BM400 measured by Joshi et al. [19] are taken for comparison here. Eight different factor settings have been used to do the experiments for observation of kerf loss with the BM400 machine. Four different cuts are made and the measurements were taken with Rapid eye measuring instrument at 35 different locations for each cut. Therefore, in total, 1120 kerf loss measurements are

TABLE 6.4: Comparison of kerf loss: BM400 and mini-WEDM

Machine \ Kerf loss	Min (μm)	Max (μm)	Average (μm)
BM400	202.3	269.0	227.64
Mini-WEDM	231.9	283.9	252.62

taken in the exercise. Table shows a comparison of minimum, mean and maximum value of the kerf loss obtained with the BM400 machine and the mini-WEDM machines.

The kerf loss in mini-WEDM is more than the one obtained with the BM400 machine, however, the loss values are comparable to each other. This is expected because the tension control mechanism in the mini-WEDM is manual in nature. Hence, there are wire vibrations in the mini-WEDM which are more than that in the BM400 machine. Also, as the scope of this work is to design and fabricate a working prototype of the machine, all the combination of V_{OC} , I_{ref} , etc. are not explored in the case of mini-WEDM. There would exist a set of parameters for which the kerf loss would be better than or at least as good as the kerf loss obtained with the commercial BM400 machine.

6.6 Utility of the Machine

Due to complete customizability, the machine is useful for doing experimental research on cutting of new type of materials. For example, WEDM is being investigated as an efficient alternative to cut semiconductor materials like silicon, SiC, etc., whose electrical conductivity ($10\text{-}100 \text{ S/m}$) is several orders of magnitude lower than that of the metals (10^7 S/m) [60]. The other properties of these materials like melting point, hardness, etc., also vary to a great extent from those of the metals. This machine can be used to find an optimum set of process parameters which are useful specifically for such new materials. As this machine is smaller in size and substantially lower in cost as compared to WED machines in the market, it is useful for small scale industries and for small engineering institutes/colleges, for whom it is not possible to purchase and maintain the large-size WED machines available in the market.

6.7 Discussion and Future Improvements

Improvements possible to be done in the subsystems of mini-WEDM are as follows.

1. **Pulse Generator:** Presently, the pulse generator uses Semikron IGBTs and not MOSFETs. The experimental results indicate that the t_{ON} for cutting silicon should be of the order of several 10s of μs . To achieve this, the switching frequency should be of the order of 500 kHz to 1 MHz. This is not possible with IGBT switches as the delay is of the order of 100s of ns [170, 179]. Therefore, appropriate MOSFETs should be chosen for development of next version of the pulse generator. Also, the controller implemented now is a simple PI controller. It should be replaced with an appropriate lead-lag compensator for a better control. The other pulse generator topologies for example the one with a bipolar output can be explored for various types of materials.
2. **Wire-feed Mechanism:** There is no tension control in wire-feed mechanism. If both spools are motorized, then the tension control can be implemented without affecting the other parts of the wire feed mechanism.
3. **Dielectric Circulation System:** A pump of higher power rating can improve the flow rate of dielectric fluid. The flushing system can also be improved with a better design. To further improve the system, the control of dielectric flow rate can be implemented. The flow rate affects the hydrodynamic forces on the wire, as well as, it affects the gap conditions.
4. **Other parts:** The motion of Holmarc translation stages, is controlled by the micro-motion software, which waits for the trigger generated by the TMS320F28069 microcontroller. The complete control can be programmed on microcontroller eliminating the PC interface.

Chapter 7

MWEDM: Wire-wire Forces and Novel Electrical Supply Schemes

This chapter is based on the theme of calculation of electrical forces in WEDM, particularly in MWEDM used for production of multiple wafers simultaneously. In the case of a single wire EDM, it is shown that the electrostatic force is stronger than electromagnetic force for semiconductors workpiece. A detailed treatment of wire-wire forces is presented for the first time by analytical method as well as FEM. Considering the wire as string under tension, an estimate of wire-deflection is presented along with an algorithm to design a new MWEDM. Further, to alleviate the problem of wire-deflection, novel electrical supply schemes along with the necessary EPG topologies are presented especially for MWEDM.

In general, four types of forces are known to be present in WEDM: (a) Reaction force (b) Hydrodynamic force (c) Electrostatic force and (d) Electromagnetic force [32]. Reaction force appears due to expansion of bubble at the gap breakdown event. As the wire and the workpiece are always in liquid dielectric environment, the liquid exerts *drag* as continuous sparking happens in the gap. This is the hydrodynamic force acting on the wire. The electrostatic force is present during ignition delay time or when there is no sparking and just ‘open’ pulses appear across the gap, as illustrated in Sections 6.4 and 6.5. Electromagnetic force appears due to eddy currents generated in the workpiece.

These forces are important from viewpoint of geometrical accuracy in WEDM. Mainly they affect the accuracy as follows: (a) Unintended concavity appears in case of straight

line cuts [116]. (b) The roughness might increase even if there is no ‘concavity’ on the surface [81] (c) Geometrical accuracy of corner cuts is affected [115]. For the semiconductor ingot slicing application, the analysis of forces is important, as it can affect the flatness of the cut wafers.

This chapter is organized as follows. The fundamentals of forces of electrical origin are discussed in next section. Analysis of forces for single wire EDM is treated in brief in Section 7.2. Section ?? is dedicated to a detailed discussion of forces in MWEDM. An estimation of wire-deflection and an algorithm for design of WEDM for silicon is given Section 7.3. To overcome the problem of wire-vibrations due to electromagnetic forces, novel electric supply schemes are proposed specially for MWEDM. The necessity of such schemes is described in Section 7.4. Two new schemes: PNPN and P0P0 are described in the subsequent sections. Results of FEA of forces in MWEDM are presented in Section ??.

7.1 Fundamentals of Forces of Electrical Origin in WEDM

Fundamental equations governing the forces of electrical origin and the duration of their appearance in the WEDM parlance are explained below [32].

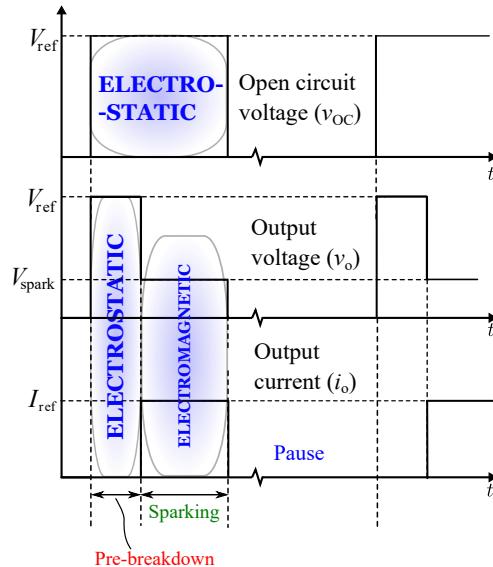


FIG. 7.1: Occurrence of forces w.r.t. stages in WEDM voltage and current waveforms

1. **Electrostatic Forces:** These forces exist during the pre-breakdown period and during the ‘open’ pulses, when the spark current is zero, as indicated in Fig. 7.1. The basic equation governing these forces is

$$\mathbf{f}_{\text{ES}} = q\mathbf{E} \quad (7.1)$$

where, q is the charge on the wire or the workpiece and \mathbf{E} is the electric field intensity¹. However, for a given problem geometry, the value of q may not be known exactly. In such cases, the electrostatic force is computed from energy stored in the surrounding medium. The electrostatic energy (U_{E}) stored in the field between two electrodes with potential difference V , is given by

$$U_{\text{E}} = \frac{1}{2}CV^2 = \frac{1}{2}\epsilon_0|\mathbf{E}|^2 \quad (7.2)$$

The force is the derivative of energy with respect to distance x given by:

$$f_{\text{ES}} = -\frac{dU_{\text{E}}}{dx} \quad (7.3)$$

2. **Electromagnetic Forces:** There are two types of forces in this category. First is the Lorentz force component given by [190]:

$$\mathbf{f}_{\text{EM}} = q\mathbf{v} \times \mathbf{B} \quad (7.4)$$

where, \mathbf{v} is the velocity of the charge q placed in the magnetic field with flux density \mathbf{B} .

In the case of WEDM, a time varying current flows through the wire during the sparking stage. As a consequence, eddy currents are induced in the workpiece. These eddy currents produce magnetic field. The current carrying wire is located in that induced magnetic field and hence it experiences force. The force *density* can be given by

$$\text{force density} \quad \mathbf{F}_{\text{EM1}} = \mathbf{J}_{\text{free}} \times \mathbf{B} \quad (7.5)$$

Here, the subscript ‘free’ denotes that it is free current density.

¹For brevity, the subscripts “ES” and “EM” used in this section are not continued in the subsequent sections. The type of force can be easily recognized from the context.

Even if the current is not time varying, there could be a second component of electromagnetic force: the magnetization force, which arises when the workpiece is made up of magnetic materials (i.e. with $\mu_r \gg 1$). The magnetization force density is given by [190]:

$$\mathbf{F}_{EM2} = -\frac{1}{2}\mathbf{H} \cdot \mathbf{H} \nabla \mu + \nabla \left(-\frac{1}{2}\mathbf{H} \cdot \mathbf{H} \frac{\partial \mu}{\partial \rho_m} \rho_m \right) \quad (7.6)$$

where, ρ_m is the mass density of the material and μ is the magnetic permeability. The first term in (7.6) refers to the force arising due to a gradient in the permeability i.e. when there is spatial variation in magnetic permeability. In the case of WEDM, this happens whenever there is a high permeability workpiece or any other part of the WED machine made of high permeability material, in the vicinity of the wire. The second term in (7.6) indicates the forces arising due to change in density of the material. This term is also known as magnetostriction force density [190]. This term is neglected in electromagnetic simulation where temperature changes and subsequent change of state of the material are not considered.

The electromagnetic force exists mainly when finite spark current is flowing through the wire. Therefore, this force is exerted during the sparking stage in the WEDM operation as shown in Fig. 7.1.

7.2 Analysis of Forces in a Single Wire EDM

In the case of a single wire EDM, the analysis of forces is done by several researchers as already listed in Section 2.6. All the results reported till date pertain to metals and no analysis is done for semiconductors. The following subsections present analysis of forces for the case single wire EDM of semiconductors.

7.2.1 Electrostatic force

Obara et al. [33] and Han et al. [34] have investigated electrostatic force on the wire with a simple 2D geometry (wire and a ground plane) as shown in Fig. 7.2(a). They have used the closed form analytical solution in (7.7) to compute the force, where V is

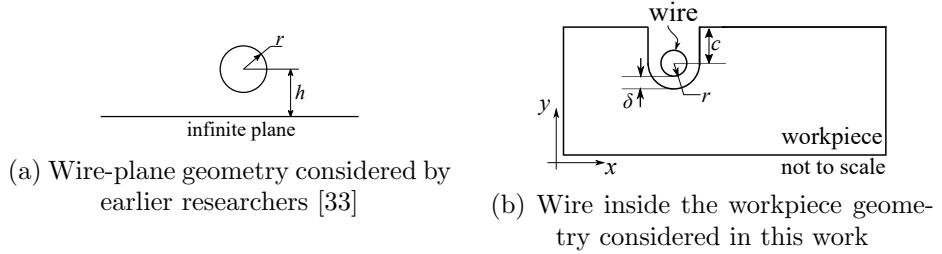


FIG. 7.2: Problem geometry

the potential difference between the wire and the workpiece.

$$F = \frac{\pi \epsilon V^2}{r \sqrt{\left(\frac{h}{r}\right)^2 - 1} \ln^2 \left(\frac{h}{r} + \sqrt{\left(\frac{h}{r}\right)^2 - 1} \right)} \quad (7.7)$$

However, this formula is valid only when the wire is not inside the workpiece. When the wire goes inside the workpiece the geometry is different as shown in Fig. 7.2(b). In this case, there is no simple closed form solution hence the force needs to be computed by FEA.

Before performing FEA, it is necessary to check the voltage across the gap between the wire and the workpiece, especially in the case of semiconductors. A schematic picture of the WEDM setup is shown in Fig 7.3. When the workpiece is metallic, it is clear that, the voltage V_{AB} (voltage between points A and B) = V_s . When the workpiece is semiconductor, it is necessary to check if the voltage across the gap is equal to the supply voltage. A silver contact is made at point A and voltage across points A and B is measured for several values of voltage V_s . In each case it is found that, $V_{AB} = V_s$.

The force values are found by varying the distance of center of wire from the edge of the workpiece i.e. ‘c’ as shown in Fig. 7.2(b). The negative values of c represent the cut length. The results of the electrostatic FE simulations (using COMSOL multiphysics) are shown in Fig. 7.4. Homogenous Dirichlet boundary conditions are used i.e. the problem domain is bounded by a circle which is at a distance four times the length of the workpiece, and $V = 0$ is assigned on that boundary. Triangular mesh is used and mesh independent study is also performed to ensure that the results are correct. It can be seen that the x component of the force (F_x) is negligible as compared to the y component F_y of the force. Therefore, the resultant force is in the y direction only i.e., the direction of force is towards/away from workpiece only, even after the wire travels inside the workpiece. The star markers indicate the values of force computed by

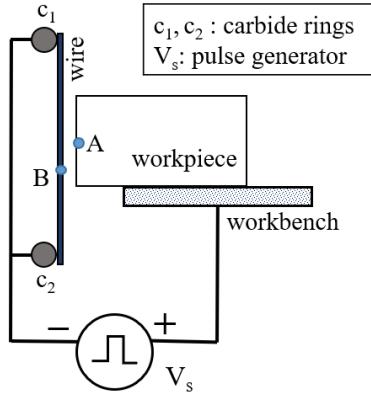


FIG. 7.3: Schematic picture showing points of voltage supply and points between which the spark is formed

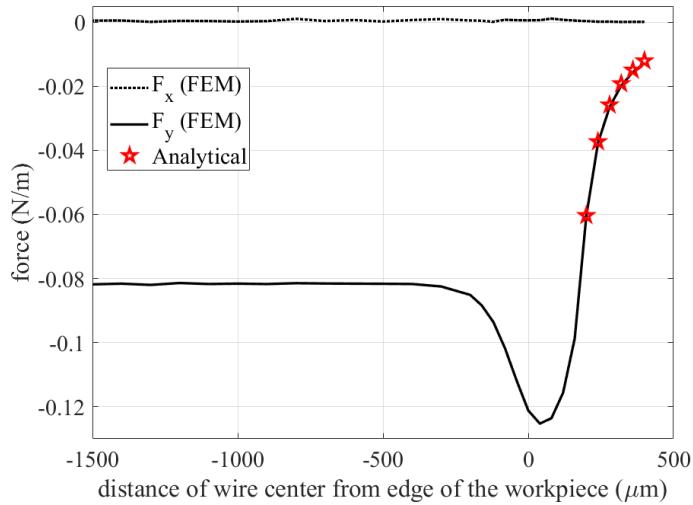


FIG. 7.4: Variation of electrostatic force with distance of wire center from edge of the workpiece

analytical expression in (7.7) for six representative points, where the wire is outside the workpiece. The values match closely with those computed by FE simulations, as shown in Fig. 7.4. However, as the wire travels inside the workpiece, the magnitude of force increases as seen from the FEA results in Fig. 7.4 - the magnitude of force for $c = -500$ to $-1500 \mu\text{m}$ is 0.08 N/m , whereas that for $c = 200 \mu\text{m}$ to $500 \mu\text{m}$ the magnitude is around 0.02 N/m to 0.06 N/m . Therefore, when the wire is inside the workpiece, the force exerted does not conform to the analytical expression in (7.7). Therefore, the closed form solution in (7.7), used by the earlier researchers, is inadequate to estimate the exact value of the electrostatic force.

7.2.2 Electromagnetic forces

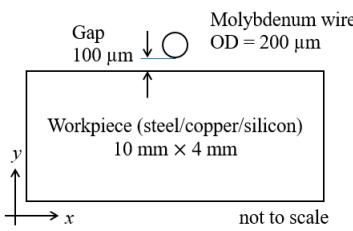
As explained in Section 7.1, the electromagnetic forces are exerted on the wire when time varying current flows through the wire or the workpiece is made up of a ferromagnetic material. In this section, the electromagnetic force for a single wire EDM is discussed. First, the force exerted on a metallic workpiece is considered.

7.2.2.1 Force on metallic workpiece

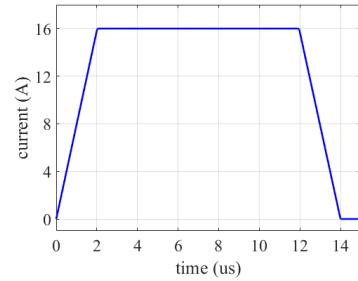
Earlier researchers [112] have used the problem geometry shown in Fig. 7.5(a) and the trapezoidal current excitation with rise time and fall time equal to $2 \mu\text{s}$, as shown in Fig. 7.5(b). As a test case, the same geometry and current excitation is used for force computation. The force magnitudes obtained by FEA are shown in Fig. 7.6. It can be seen that the results match closely with each other.

Considering the direction of co-ordinate axes and position of the wire with respect to the workpiece shown in Fig. 7.5(a), positive value of F_y would indicate repulsive force and vice versa. Therefore, during rise time of current, the force is repulsive for copper while it is attractive for steel. Whereas during fall time, the force becomes repulsive for copper and it is attractive for steel. This can be explained as follows. The relative permeability of steel is $\mu_r = 100$. Therefore, the dominant component of force in the case of steel workpiece is the magnetization force. However, in the case of copper, the dominant component of force is due to interaction of current induced in the workpiece due to time varying current in the wire. The direction of force is governed by (7.4). The direction of induced current however is governed by the Lenz's law. It states that the induced current would produce magnetic field which would oppose the cause i.e. the magnetic field which is responsible for inducing the current.

Now, let the direction of current in the wire be in the positive z direction. When the current is rising, the magnetic field is anticlockwise and it is increasing, i.e. $dB/dt > 0$. Therefore, the direction of induced current would be in the negative z direction so that it would produce the magnetic field in clockwise direction, i.e. in the positive x direction at the location of wire. From (7.4), as \mathbf{v} is in the positive z direction and \mathbf{B} is in the positive x direction, the force would be in the positive y direction. The opposite would be the case when the current is falling. Thus, the direction of force seen in Fig. 7.6(a) is

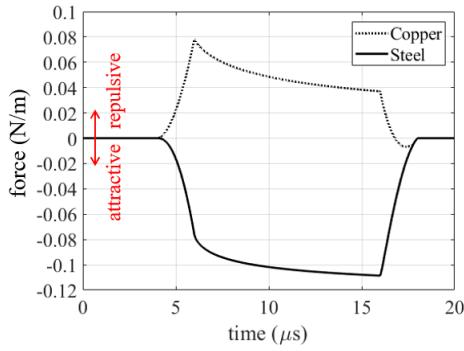


(a) Geometry with wire above the workpiece

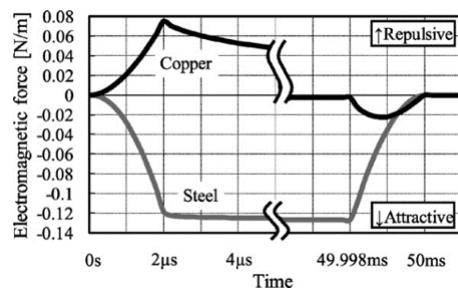


(b) Trapezoidal current excitation

FIG. 7.5: Problem definition used by earlier researchers [112]



(a) Force obtained by FE analysis



(b) Force results in literature (image source: [112])

FIG. 7.6: Comparison of results obtained by FE analysis with published results

as expected. This point is again explained for the case of exponential current excitation in detail in Section ??.

7.2.2.2 Force on silicon workpiece

The relative permeability of silicon is measured by vibrating sample magnetometer and it is found that for silicon $\mu_r \approx 1$ as described in Appendix A. Therefore, it is expected that the nature of force in the case of silicon workpiece would be similar as that in the case of copper or any other non-magnetic material. However, it should be noted that electrical conductivity of silicon depends upon the dopant concentration. It varies from around 0.1 S/m to 3.33×10^3 S/m [191]. Therefore, for silicon, the force magnitude is dependent on the dopant concentration. The FE analysis is performed for three conductivity values, $\sigma = 0.1, 32.77$, and 3333.33 S/m. Fig. 7.7 shows the plot of force values for the trapezoidal current excitation with three values of conductivity. By comparing these values with those in Fig. 7.6, it can be seen that the magnitude of force in the case of silicon is two orders of magnitude lesser than that in the case metals. Also,

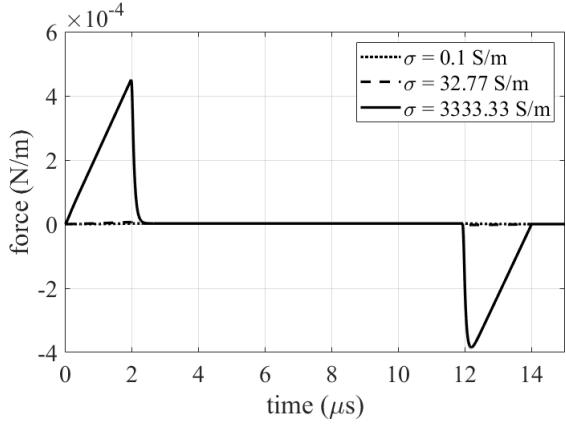


FIG. 7.7: Electromagnetic force in the case of silicon workpiece with different values of electrical conductivities

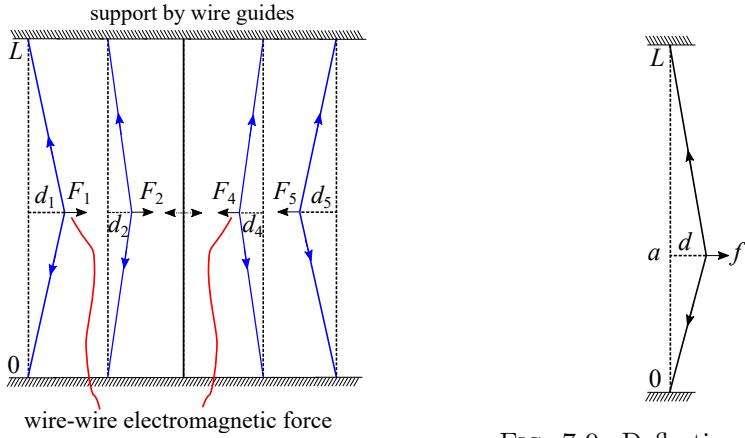


FIG. 7.8: Schematic of deflection of wires due to wire-wire force

FIG. 7.9: Deflection of string under action of force

the force is lesser in magnitude than the electrostatic force in Fig. 7.4. From Figs. 7.4, 7.6, and 7.7, it can be inferred that the electromagnetic forces are dominant in the case of metallic workpiece whereas, electrostatic forces are dominant in the case of silicon workpiece.

7.3 Estimation of Wire Deflection

Deflection for a 5-wire EDM is shown schematically in Fig. 7.8, where d_1 , d_2 , d_4 , d_5 are deflections of the wires due to forces F_1 , F_2 , F_4 , F_5 , respectively. The net force F_3 is zero as equal and opposite forces are exerted by wires on both sides. In this work, a simple model of string of length L under initial tension T is used as shown in Fig. 7.9(b), as used in [192]. The deflection d of the string due to force f is given in (7.8). If the workpiece is exactly at the midpoint of the length of the wire ($a = L/2$),

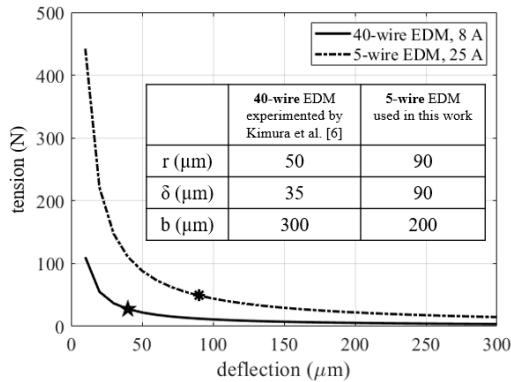


FIG. 7.10: Required tension vs allowed deflection for 40-wire EDM and 5-wire EDM

required tension to keep the initial deflection within a tolerance level reduces to a simple expression given in (7.8). This equation gives a preliminary estimate of the deflection caused in the wires due to the force

$$d = \frac{fa(L - a)}{LT} \quad (7.8)$$

If $a = \frac{L}{2}$, $T = \frac{fL}{4d}$

7.3.1 Validation with published results

Kimura et al. [37, 118] have stated that much higher wire tension is required in order to limit the kerf width. The specifications in their paper are as follows: $I_{\max} = 8$ A, maximum kerf width = 209 μm , width of workpiece = 80 mm, $n = 40$, $\delta = 35$ μm , $L = 195$ mm. Hence, the maximum allowable deflection should be around 35 μm . In [37, 118], use of track shaped wires is suggested in order to sustain the high tension required. The width of the wire is 100 μm and length is 200 μm . Substituting these in equation (7.8) gives maximum value of force 0.015 N. Fig. 7.10 shows the tension required for various deflection values using equation (7.8). The tension required for a deflection of 40 μm is around 27 N, which is shown by star-marker (*), which agrees well with value 28 N reported in [118]. Hence, the procedure outlined in this work satisfies the experimental result already reported.

The plot also shows tension values required for case of 5-wire EDM considered in the earlier sections, with $I_m = 25$ A. Considering allowable deflection equal to spark-gap length of 90 μm , the tension required is around 49 N (shown by * marker), which is much larger than that required for 40-wire EDM with $I_m=8$ A. This is expected because

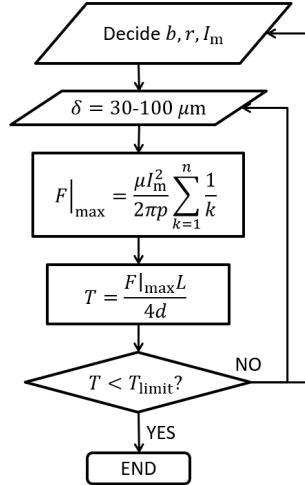


FIG. 7.11: Algorithm to design an MWEDM considering electromagnetic forces

the forces on wires are directly proportional to the square of current as per equation (??).

7.3.2 Algorithm to design MWEDM

The above estimate can be used to design the structural dimensions of the an MWEDM setup. An algorithm is given in Fig. 7.11 and described below.

1. Select a value of required wafer thickness b . The radius of wire r can be appropriately chosen. Decide the maximum spark current I_m .
2. The spark gap width δ can be appropriately chosen to be any value between 30-100 μm depending on the setup and expected kerf loss.
3. After choosing n , the net force on each wire can be calculated by (??).
4. For a given ingot size, the length of wire L can be decided, which is the distance between two wire guides. Expression in (7.8) can then be used to calculate the required tension, depending upon the maximum tolerable deflection d .
5. The required tension can be put in (7.9) to check whether the tension is within the limit imposed by tensile strength σ of the wire with cross sectional area S_A .

$$\text{Check, if } T < T_{\max} \quad \text{where, } T_{\max} = \sigma S_A \quad (7.9)$$

6. If value of tension required is too large, tweak the choices of I_m , L , δ and d made in earlier steps so that the tension value is practically realizable.

7.4 Necessity of Novel Electrical Supply Schemes

Previous sections discussed the deflection of wires due to wire-wire forces in MWEDM. Few researchers have reported this problem [37, 118] earlier. Bamberg and Rakwal [55] have stated that, in order to contain the deflection and vibrations of wires within permissible limits, tension as high as 85%-90% of the failure strength of the wires needs to be applied in MWEDM [14]. The following problems may arise due to high tension and wire vibrations:

1. **Wire-breakage:** Due to the high tension close to the failure strength of the wire, there is a risk of wire breakage, which may hinder the production and reduce the throughput of wafers
2. **Increase in kerf losses:** If lesser tension is applied, wire deflection would increase, which would subsequently increase the kerf loss.
3. **Limit on minimum wafer thickness:** More the amplitude of vibrations, more will be the lower limit on the allowed wire-pitch. Hence, the vibrations impose a limit on the minimum thickness of the wafers which can be cut with MWEDM.
4. **Wafer to wafer variation of surface roughness:** In the present scheme the wires at the end experience the maximum deflection, whereas the wires in the middle experience the least deflection. Due to this, the corresponding wafers at the end may be the worst affected and the surface roughness for those wafers would be more than that of the others.

Point 1 above indicates that if a higher tension is used, there would be process hindrance and the effective value of MRR would reduce. Point 2 indicates that, if a lesser tension is applied, the SR would increases, i.e. flatness of the cut surface needs to be sacrificed. Therefore, there is a trade-off between the decreased MRR and increased SR, due to the wire-wire forces in MWEDM.

Previous researchers [37, 118] have proposed the following mechanical arrangements besides high tension to reduce the wire vibrations: use of track shaped wires, providing side support for the wires, keeping the wire guides as close to the workpiece as possible, etc. However, there are two shortcomings of the above arrangements:

1. **Remedial nature of schemes:** The mechanical schemes can only contain (i.e. maintain within limits) the deflections once they are produced. Hence, these schemes can be considered as remedial in nature. They cannot *prevent* or reduce the forces produced by the current flowing in the wires.
2. **Aging and vibrations:** The mechanical arrangements can themselves be subject to vibrations and/or wear and tear due to prolonged usage/ aging of the equipment.

Therefore, two novel electrical supply schemes and the required pulse generator topologies are proposed.

1. First scheme²
2. Second scheme³

7.5 Conclusion

The nature of electrical forces in WEDM is elaborated in this chapter. Earlier literature considered only two types of forces: (a) Electrostatic and (b) Electromagnetic and only for metallic workpieces. The electromagnetic forces can be further classified into Lorentz forces and magnetization forces. The magnetization force is present only if the workpiece is made up of magnetic material. Quantification of the forces for metals is done for a single wire EDM and the results match with the ones published earlier in [114].

It is seen that the electromagnetic forces are weaker than the electrostatic forces in the case of silicon, which is opposite to that of the metals. This is mainly because the

²A patent is filed for this scheme as:

Makarand M. Kane, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, “Electrical Supply Schemes for Multi-wire Electric Discharge Machine”, Indian Patent, Appl. No. 202021041051, 22 Sep, 2020

³A patent is filed for this scheme as:

Makarand M. Kane, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, “Electrical Supply Scheme with time-interleaving for Multi-wire Electric Discharge Machine”, Indian Patent, Appl. No. 202021044094, 09 Oct, 2020

conductivity of silicon is six to seven orders of magnitude lesser than that of the metals. It is found that the electromagnetic force is significant only in the case of heavily doped silicon, whose conductivity is of the order of 10^3 S/m.

The electrical forces in the case of MWEDM are treated in detail. The forces in a single wire EDM are between the wire and the workpiece. It is reported for the first time that there are strong forces of attraction between wires in MWEDM. These forces are analyzed thoroughly using FEM simulations of 2D geometry.

An analytical expression is derived to compute the electromagnetic forces exerted by the wires on each other. The expression is verified by FEA for two cases 5-wire EDM and 10-wire EDM with p-type silicon as workpiece. Experimentally measured material properties and current excitation is used in simulations. Transient FEA shows that the wire-workpiece forces exerted due to eddy currents in the workpiece are much smaller in magnitude than the wire-wire forces. This phenomenon can be attributed to lower electrical conductivity and non-magnetic nature of silicon. The comparison of order of electromagnetic force components in WEDM for silicon workpiece is also presented.

A method is given to estimate the possible deflection of wire due to this force using model of string under tension. Further, a design algorithm is also provided to design a new MWEDM with the existing electrical supply scheme.

Chapter 8

Conclusion and Future Scope

The research reported in this thesis is focused on the adaptation of WEDM for slicing of semiconductor ingots, considering application to solar PV and microelectronics industries. This chapter summarizes the work done and major findings. Potential impact of each component of work along with the future scope of research and development is also enumerated at the end.

8.1 Summary of the work done

Major components of the work done can be summarized as follows:

1. **Electrical characterization of spark-erosion of silicon and steel:** Comparative study of spark-erosion of silicon vis-à-vis that of steel is done based on pulse parameters of voltage and current pulses of sparks. This study is mainly performed to bring out the differences from electrical perspective, thus extending the knowledge of physics of the process for silicon. The following relations are observed for WED machining of silicon and steel.

$$V_{sp}^{(Si)} > V_{sp}^{(St)} \quad \text{and} \quad I_{sp}^{(Si)} < I_{sp}^{(St)} \quad (8.1)$$

Effect of workpiece thickness on the voltage and current behavior is also investigated. When the thickness of workpiece increases, the spark current increases for silicon, however this phenomenon is not observed in the case of steel. This

is important especially for ingot slicing application, where the thickness of the workpiece changes continuously.

Especially, it is shown that the current required for machining is not decided by the electrical conductivity of silicon. It is qualitatively explained by the Shockley equation governing the voltage and current characteristics of a forward biased diode. It is shown that, the spark-semiconductor junction plays an important role in deciding the current and voltage during spark-erosion of silicon.

2. **EDM pulse generators:** The work done in this domain can be divided into two parts

(A) **Classification and comparative study:** Classification of EPGs till date is mainly restricted to only two types of pulse generators. Therefore, a systematic and elaborate study of 13 important topologies is presented for the first time from power electronics perspective. Classification of topologies is done based on their structure. The control schemes, efficiency, component count and voltage stress are considered for the comparative study. It is shown that the voltage and current ripples arising during the stage transitions should be considered while design of these pulse generators. Three stage operation and existence of two dominant frequencies in the computation of efficiency of EPG is considered for the first time. These two issues are discussed in detail in Chapter 4.

(B) **Modeling and efficiency improvement:** The pulse generator for the WEDM is built using the topology proposed by Tastekin et al. [46]. Modeling of the pulse generator in the frequency domain is done using averaged state-space formulation. In this thesis, a novel control scheme, PCRS, is proposed instead of the conventional scheme, CCRS. The scheme can improve the efficiency of the pulse generator from 31% to 62%. For a sample case, it is shown that, the efficiency improvement can save | 900,000/- ($\approx \$ 12150/-$) per month for a wafer manufacturing plant. The pulse generator hardware is built using Semikron IGBT modules and TMS320F28069 microcontroller from Texas Instruments. The new control scheme is tested using an emulated model of EDM-spark.

3. **Design and fabrication of customizable miniature WEDM:** A fully customizable miniature WEDM machine is designed and built. A dedicated pulse generator is also built for the WEDM. The miniature WEDM consists of five subsystems: a pulse generator, a wire feed mechanism, a dielectric circulation system,

a CNC system, and a workbench + dielectric tank. The design and fabrication of all the components is described in Chapter 6. The WEDM fits in the size $120 \times 60 \times 60$ cm and can easily fit on a tabletop. The maximum workpiece travel is 5 cm and minimum CNC step is $0.125 \mu\text{m}$. The pulse generator can provide pulses with maximum frequency of 10 kHz, maximum voltage of 200 V and maximum current of 10 A. Experiments have shown that the kerf loss achievable by the machine is within permissible limits (around $240 \mu\text{m}$ kerf with a wire of OD $180 \mu\text{m}$). The kerf loss is comparable to that obtained with a commercial machine. It can be reduced further with some improvements in the machine.

4. **Multi-wire electric discharge machine:** The contributions in this domain can be categorized in two domains:

(A) **Analysis of the wire-wire forces:** Forces of electrical origin cause wire deflection and consequently affect the surface quality. Analysis of these forces is done using 2D FE analysis in COMSOL Multiphysics, particularly when the workpiece is made of silicon. As the electrical conductivity of silicon ($\approx 10\text{-}100 \text{ S/m}$) is six to seven orders of magnitude lesser than that of metals ($\approx 10^6\text{-}10^7 \text{ S/m}$), it is seen that the electromagnetic forces in the case of silicon workpiece are much smaller than that in the case of metallic workpiece.

As far as slicing of semiconductors for PV and microelectronics industries is concerned, it is found that the wire-wire forces in MWEDM are more significant than the wire-workpiece forces. A closed form expression for these forces is derived in this thesis and it is verified by 2D FE analysis for the cases of 5-wire and 10-wire EDM. All the previous researchers have used trapezoidal waveform as current excitation. However, this study has used exponentially rising current waveforms, which are observed in experimental studies. Deflection of wires under the action of wire-wire force is estimated by considering the wire as a string under tension.

(B) **Novel electrical supply schemes:** Earlier researchers have reported that in implementation of multi-wire EDM the wire tension required is of the order of 85 to 90% of the failure strength of wires. This tension can cause wire-breakage, which can hinder the process and reduce the overall throughput. One of the significant reasons of this requirement is strong wire-wire electromagnetic forces of attraction. Two novel electrical supply schemes: PNPN and P0P0 are proposed such that the wire-wire forces are reduced to about 20-40% of the force exerted in

the case of conventional schemes. In the conventional WEDM, usually the wires are at negative potential (cathode) and the workpiece is at positive potential (anode). The PNPN scheme is novel in the sense that the wires are at positive and negative potential whereas workpiece is at zero potential. The pulse generator topologies are also proposed for the schemes so that the wires are excited properly in the MWEDM.

8.2 Potential Impact of the Work

Every component of the research presented in this thesis enables WEDM to be used effectively on commercial scale for slicing of semiconductor ingots. Some components have the potential to make an immediate impact and the others can make a long term impact. Besides this field, the research has also contributed to the advancement of knowledge of WEDM process and electromagnetic forces in WEDM in general.

The studies of spark-erosion of silicon, based on CVC of sparks are useful to understand the process in a better way. This will help to design novel WEDM machines dedicated for silicon. In particular, the non-linear diode based model can be better utilized for multi-physics simulation of WEDM studies.

Chapter 4 has given classification and comparative study of EDM pulse generators from power electronics perspective. This study is useful for researchers in power electronics domain to develop pulse generators for EDM/WEDM. This is the first of its kind study of EPGs from power electronics perspective. Issues regarding the sizing of components and efficiency computation, which are crucial for EPGs because of their peculiar operation, are also elucidated in this. This can be useful for building new energy efficient EPGs which are important from viewpoint of sustainable manufacturing.

Investigations into MWEDM are very important from viewpoint of acceptance of WEDM as a commercially viable wafer manufacturing technique in place of conventional wire-sawing. The issue of wire-wire forces and subsequent wire-vibrations are important considering high surface quality expected for semiconductor wafers cut for solar PV and microelectronics applications. Therefore, the novel electrical supply schemes will prove to be useful for developing MWEDM systems with minimal wire-vibrations.

8.3 Future Scope

In order to adapt the WEDM completely so that it can be used by industry for slicing semiconductor ingots, the following points indicate future scope of development and research that can be done on each of the above fronts.

1. **Experimentation with customized WEDM:** The customized miniature WEDM can be utilized to do further investigations for slicing silicon wafers. On one hand, the developed machine can be used to closely observe and probe spark-erosion of silicon which is difficult with commercially available WED machines. Also, an EPG which can produce waveforms other than pulsed DC waveform can be coupled with the machine to study silicon cutting with different types of waveforms. On the other hand, the machining performance parameters viz., MRR, SR and TEWR can be studied with variation of wire material, dielectric fluid and other input settings.
2. **Development of MWEDM:** A prototype MWEDM can be fabricated with the novel schemes proposed in this work. The hardware implementation can bring out certain issues which might be missed in the simulation studies.
3. **Modeling of pulse generator:** Modeling of pulse generator considering non-linear nature of the load can be carried out, for example with the methods proposed by Vasca [193] and Sunito [194]. This can be helpful for controlling the EPGs in a better way.
4. **Equivalent circuit model of spark-erosion:** The present work discusses the representative circuit of WEDM sparks as seen from the pulse generator. A more accurate equivalent circuit model of sparks produced during the WEDM of silicon can be devised based on works such as [195, 196].
5. **Complete coupled-field modelling of electromagnetic forces:** In the present work, the forces are computed independently using electromagnetic FEA and then the model of string under tension is used. A completely coupled structural-electromagnetic field analysis can yield frequency of forces and hence modes of vibration of wire.

Author's Publications

Journal Papers

1. M. M. Kane, A. Khadse, H. Chandwani, H. Bahirat and S. V. Kulkarni, "Modeling and Efficiency Improvement of a Pulse Generator for Wire Electric Discharge Machining," in *Special issue on Pulsed Power Science and Technology, IEEE Transactions on Plasma Science*, vol. 48, no. 10, pp. 3350-3357, Oct. 2020.
2. M. M. Kane, A. A. Phanse, H. J. Bahirat and S. V. Kulkarni, "Classification and comparative study of EDM pulse generators," in *IET Power Electronics*, vol. 13, no. 14, pp. 2943-2959, Nov. 2020, doi: 10.1049/iet-pel.2020.0205.
3. M. M. Kane, S. V. Kulkarni, H. J. Bahirat, S. S. Joshi, "Analysis of Electrical Forces in Multi-wire EDM for Semiconductors," in *Procedia CIRP*, (an Elsevier journal, affiliated with CIRP, The International Academy for Production Engineering), Vol. 95, 2020, pp. 302-307, ISSN 2212-8271
4. M. M. Kane, Kamlesh Joshi, Nitin Tiwari, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, "Experiments with Miniature Wire EDM for Silicon", in *Procedia CIRP*, (an Elsevier journal, affiliated with CIRP, The International Academy for Production Engineering), Vol. 95, 2020, pp. 296-301, ISSN 2212-8271.
5. M. M. Kane, K. Joshi, H. J. Bahirat, M. Phadke, S. V. Kulkarni, S. S. Joshi, "Comparative Electrical Characterization of Spark-erosion of Silicon with Steel as a Base and its Implications on Equivalent Circuit", Mat. Sci. in Semiconductor Processing, under review (minor revision required)

Patents

1. Makarand M. Kane, Kamlesh Joshi, Nitin Tiwari, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, “Customizable Miniature Wire Electric Discharge Machine”, Indian Patent, Appl. No. 202021032434, 29 Jul, 2020.
2. Makarand M. Kane, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, “Electrical Supply Schemes for Multi-wire Electric Discharge Machine”, Indian Patent, Appl. No. 202021041051, 22 Sep, 2020.
3. Makarand M. Kane, S. V. Kulkarni, Himanshu Bahirat, Suhas S. Joshi, “Electrical Supply Scheme with time interleaving for Multi-wire Electric Discharge Machine”, Indian Patent, Appl. No. 202021044094, 09 Oct, 2020.

Conference Proceedings

1. M. Kane, A. Khadse, H. Bahirat and S. V. Kulkarni, “Design and Control of Pulsed Voltage Supply for Electric Discharge Machining”, *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India*, 2018, pp. 1-6
2. M. M. Kane, A. Jadhav, M. Kumar, S.V. Kulkarni, S.S. Joshi, “Machining Behavior of Silicon in Wire EDM for PV Applications”, *EU PVSEC, European PV Solar Energy Conference and Exhibition*, Amsterdam, 25 - 29 September 2017, pp 333 – 338

Appendix A

Measurement of material properties

A.1 Measurement of Electrical Conductivity

A.1.1 Conductivity of steel

The electrical conductivity of steel is measured by using four probe tests [197, 198]. For steel, the test is performed with Keithley Nanovoltmeter (V_m) and Microampere current source (I_s), at MEMS Department, IIT Bombay. The schematic of the setup is shown in Fig. A.1. The voltage and current readings are given in the Table A.1. The distance between voltage probes is 5 mm. The area of cross section is 100 mm^2 . From this, the resistivity of the steel sample is calculated as $2.16 \times 10^{-7} \Omega \text{ m}$ and its conductivity is $4.63 \times 10^6 \text{ S/m}$.

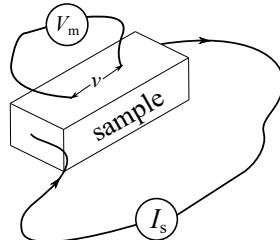


FIG. A.1: Four probe test for resistivity measurement

TABLE A.1: Results of four probe test of steel

I (mA)	V (mV)	R (Ω)
31.08	0.00032	1.029×10^{-5}
52.76	0.00060	1.137×10^{-5}
93.67	0.00092	9.821×10^{-6}
122.57	0.00131	1.068×10^{-5}
149.96	0.00167	1.113×10^{-5}
194.36	0.00222	1.142×10^{-5}

TABLE A.2: Test results of 4-probe measurements

Sample 1		Sample 2	
V (mV)	I (mA)	V (mV)	I (mA)
4.47	1.588	3.95	1.587
3.89	1.587	4.41	1.578
3.97	1.589	2.57	1.588
3.72	1.587	2.86	1.588
3.92	1.588	4.08	1.586
		4.13	1.588
		3.5	1.587
		3.7	1.588

A.1.2 Conductivity of silicon

As the current conduction process in semiconductors is different from that in metals, the four probe test for semiconductors need special probe-contacts and equipment [199]. In the present research, the measurement is done by using four-probe test setup (Model 280TSI, Make “4D Technology”) available at IIT Bombay Nano Fabrication facility. The readings are given in Table A.2. The resistivity (ρ) in $\Omega\text{-cm}$ of silicon is calculated as follows, where $s = 0.2$ cm is the distance between the probes.

$$\rho = \frac{V}{I} 2\pi s \quad (\text{A.1})$$

From the recorded readings, the resistivity of silicon is found to be $3.0554 \Omega\text{-cm}$ (i.e. conductivity is 32.77 S/m).

A.2 Measurement of Magnetic Permeability

Magnetic permeability of the silicon workpiece is measured by Vibrating Sample Magnetometer(VSM) available at Department of Physics, IIT Bombay (Model name: Physical Property Measurement System Make: Quantum Design, Inc.). Fig. A.2 shows the output of VSM test of silicon sample in the form of **M-vs-H** plot. There are 1992 sample

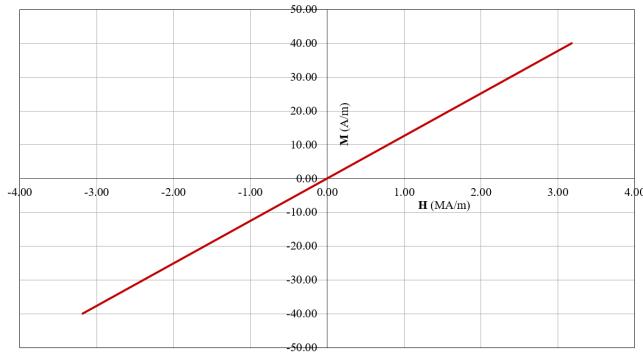


FIG. A.2: \mathbf{M} vs \mathbf{H} plot for a polysilicon workpiece tested with VSM from Quantum Design Inc.

points in the plot. The $\mathbf{M} - \mathbf{H}$ loop is almost a straight line. The susceptibility can be calculated as average of the ratios $\frac{|\mathbf{M}|}{|\mathbf{H}|}$. The susceptibility of the sample is found to be 2.41×10^{-7} . Therefore relative permeability of the sample is $\mu_r \approx 1$.

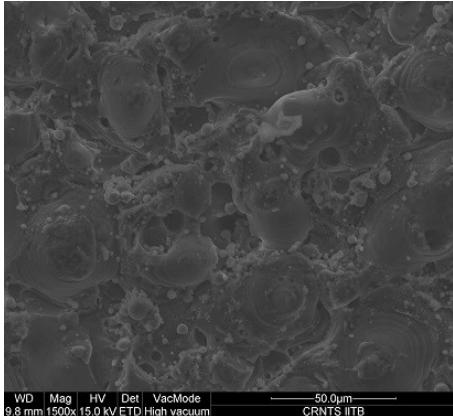
Appendix B

Post-machining Analysis of Surface Quality and Impurities

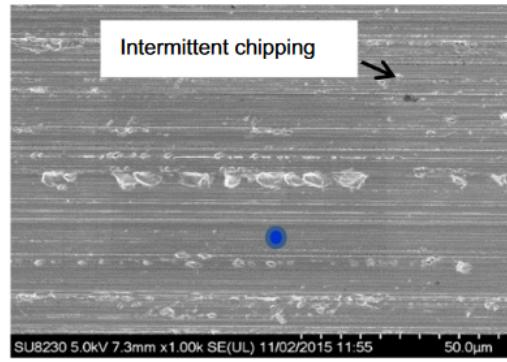
For machining of metals, the surface roughness is measured with roughness average (Ra), TTV, etc. [29]. In the case of semiconductor wafers, the surface quality is also checked using additional methods like scanning electron microscopy (SEM), Inductively Coupled Plasma Atomic Emission Spectroscopy (ICPAES), etc [19]. In this work, the focus is on the electrical characteristics of the spark. However, for the sake of completeness, surface quality analysis is during the initial phase of the research¹. It is reported in this appendix.

SEM is widely used in literature to study the surface morphology of crystalline silicon solar cells. Energy Dispersive X-ray spectroscopy (EDX) is then used as a tool to ‘detect’ elemental contamination on the cut surface. Whereas ICPAES is used to ‘quantify’ the percentage of contamination in the wafers. Thus, SEM denotes the contamination due to cutting process which are easily removable and ICPAES denotes the contamination which may have penetrated the workpiece (silicon) due to cutting process.

¹These results are published in: M. M. Kane, A. Jadhav, M. Kumar, S.V. Kulkarni, S.S. Joshi, “Machining Behaviour of Silicon in Wire EDM for PV Applications”, *EU PVSEC, European PV Solar Energy Conference and Exhibition, Amsterdam*, 25 - 29 September 2017, pp 333 - 338.



(a) SEM-EDX image of silicon surface in as-cut condition



(b) Images of Silicon surface obtained with wire-saw (image source: [200])

FIG. B.1: Comparison of cut surfaces of silicon with Wire-EDM and Wire-saw

B.1 Surface Quality of Cut Surface

The SEM image of a silicon piece in as-cut condition is shown in Fig. B.1(a). It can be compared with SEM image of a wafer cut by diamond-wire saw [200] shown in Fig. B.1(b). The chipping and sawing marks are seen on the wafers cut by wire-saw, while they are absent in the wafers cut by WEDM. Instead, Fig. B.1(a) shows some re-solidified layer of material after implosion of WEDM plasma.

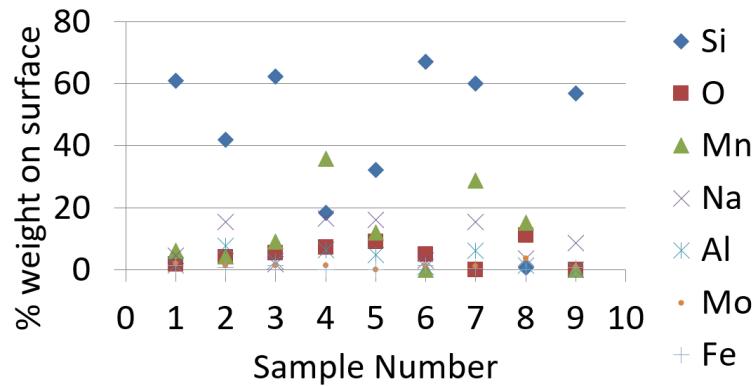


FIG. B.2: SEM-EDX results of surface of silicon cut by wire EDM.

TABLE B.1: Results of ICPAES analysis

Element	Sample (% weight)
Boron (B)	0.0041
Barium (Ba)	0.0015
Calcium (Ca)	0.3111
Chromium (Cr)	0.0036
Copper (Cu)	0.0053
Iron (Fe)	0.1489
Potassium (K)	0.0154
Magnesium (Mg)	0.025
Manganese (Mn)	0.0018
Sodium (Na)	0.0278
Strontium (Sr)	0.0004
Zinc (Zn)	0.0027
Molybdenum (Mo)	0.008
Chlorine (Cl)	1.0195
Silicon (Si)	98.4248

B.2 Impurities in Cut Surface

Surface of the cut samples (10 nos) is scanned at several places using EDX to see the contamination. The results are shown in Fig. B.2. It is seen that the significant impurities are manganese, sodium and aluminium. These contamination on surface can be removed easily by usual etching process used in wafer manufacturing. ICPAES results of cut samples (in as cut conditions) are shown in Table B.1. It is clear that, the contamination introduced in the samples are very less in percentage. They can be removed by further processes like lapping, etching, polishing, etc.

Appendix C

Expressions for RMS and Average Values

Derivations for expressions for RMS and average values of currents in chapter 5 are given in this appendix. Particularly, expressions in (5.6)-(5.8) and (5.11)-(5.14) would be derived.

C.1 Some basic derivations

Before deriving the equations, it is instructive to take a look at RMS value of a DC current with average value I_{avg} and ripple ΔI as shown in Fig. C.1. It also shows that

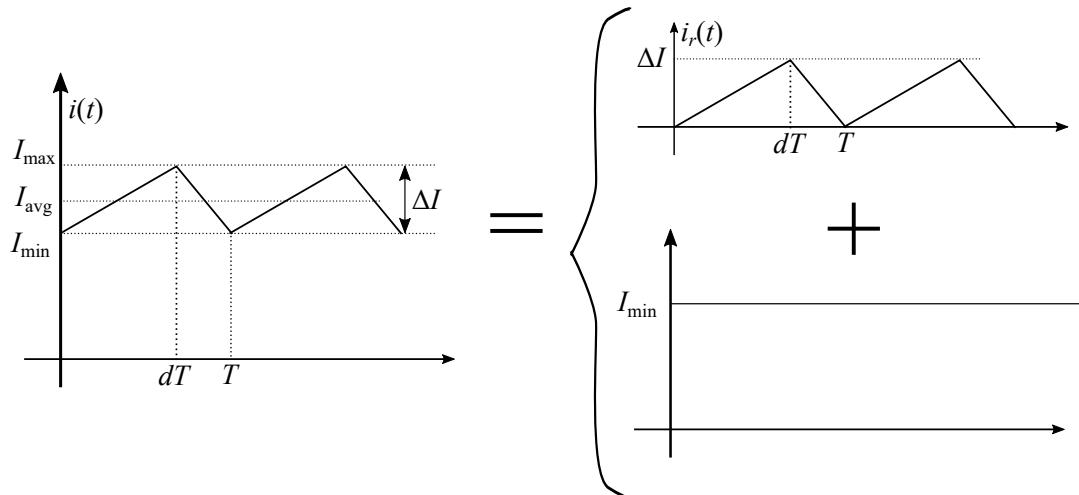


FIG. C.1: DC current with a ripple ΔI

$i(t)$ can be split into two components: I_{\min} is the pure DC component, $i_r(t)$ is the ripple component.

$$i(t) = I_{\min} + i_r(t) \quad (\text{C.1})$$

First, let us look at RMS value of $i_r(t)$.

$$\begin{aligned} [\text{RMS}(i_r(t))]^2 &= \frac{1}{T} \int_0^{dT} \left[\frac{\Delta I}{dT} \right]^2 dt + \frac{1}{T} \int_{dT}^T \left[\frac{-\Delta I}{(1-d)T} (t-T) \right]^2 dt \\ &= \frac{\Delta I^2}{T} \left[\frac{dT}{3} + \frac{(1-d)T}{3} \right] = \frac{\Delta I}{3} \end{aligned} \quad (\text{C.2})$$

Now, the RMS value of $i(t)$ can be derived.

$$\begin{aligned} [\text{RMS}[i(t)]]^2 &= [\text{RMS}[I_{\min} + i_r(t)]]^2 \\ &= \frac{1}{T} \int_0^T [I_{\min} + i_r(t)]^2 dt \\ &= I_{\min}^2 + \frac{1}{T} \int_0^T [2I_{\min}i_r(t) + i_r^2(t)] dt \\ &= I_{\min}^2 + 2I_{\min} \frac{\Delta I}{2} + \frac{\Delta I^2}{3} \quad \text{the last term is RMS}[i_r(t)] \\ &= I_{\min} (I_{\min} + \Delta I) + \frac{\Delta I^2}{3} = I_{\min} \cdot I_{\max} + \frac{\Delta I^2}{3} \\ &= \left(I_{\text{avg}} - \frac{\Delta I}{2} \right) \left(I_{\text{avg}} + \frac{\Delta I}{2} \right) + \frac{\Delta I^2}{3} \\ &= I_{\text{avg}}^2 + \frac{\Delta I^2}{12} \end{aligned} \quad (\text{C.3})$$

C.1.1 RMS and Average values for piecewise linear waveforms

For a periodic waveform $y(t)$ with n piecewise linear segments y_1, y_2, \dots, y_n , for durations D_1T, D_2T, \dots, D_nT the RMS value of the signal is given by [171]:

$$\text{RMS value} = \sqrt{\sum_{k=1}^n D_k [\text{RMS}(y_k)]^2} \quad (\text{C.4})$$

Similarly, average value of such waveform is given by:

$$\text{AVG value} = \sum_{k=1}^n D_k \text{AVG}(y_k) \quad (\text{C.5})$$

C.2 Derivation of expressions for CCRS

The expression for $\text{RMS}(i_{L1})$ in (5.6) the same as that in (C.3). Note that i_{Q1} can be considered as piecewise linear waveforms which conducts for duration $(d_{\text{CS}(1)}d_1 + d_{\text{CS}(2)}d_2 + d_{\text{CS}(3)}d_3)T_m$ (see Fig. 5.2). Therefore, using (C.4), $\text{RMS}(i_{Q1})$ would be

$$\begin{aligned}\text{RMS}(i_{Q1}) &= \sqrt{\left[I_{\text{ref}} + \frac{\Delta I}{12}\right]^2 (d_{\text{CS}(1)}d_1 + d_{\text{CS}(2)}d_2 + d_{\text{CS}(3)}d_3)} \\ &= \text{RMS}(i_{L1})\sqrt{EQ(d_{\text{CS}})} \quad (\text{C.6})\end{aligned}$$

Similarly, considering the fact that average value of $i(t)$ in Fig. C.1 is I_{ref} , D_1 conducts for the duration $(1 - EQ(d_{\text{CS}}))$, and using (C.5), it can be shown that,

$$\text{AVG}(i_{D1}) = I_{\text{ref}}(1 - EQ(d_{\text{CS}})) \quad (\text{C.7})$$

C.3 Derivation of expressions for PCRS

In the case of PCRS, there are two reference levels I_{ref1} and I_{ref2} . Therefore, current through L_1 consists of a pulsed DC waveform as shown in Fig. 5.4, where I_{ref1} is the average value for duration $(d_1 + d_2)T_m$ and I_{ref2} for duration d_3T_m . It is assumed that the ripple in two cases is ΔI_1 and ΔI_2 respectively. From (C.4), the RMS value of i_{L1} would be given by sum of squared RMS values of the respective durations, multiplied by the corresponding duty ratios.

$$\therefore \text{RMS}(i_{L1}) = \sqrt{\left(I_{\text{ref1}}^2 + \frac{\Delta I_1^2}{12}\right)(d_1 + d_2) + \left(I_{\text{ref2}}^2 + \frac{\Delta I_2^2}{12}\right)d_3} \quad (\text{C.8})$$

Similarly, switch Q_1 conducts for the duration $(d_{\text{CS}(1)}d_1 + d_{\text{CS}(2)}d_2)T_m$ within the time interval $(d_1 + d_2)T_m$ and for the duration $d_{\text{CS}(3)}d_3T_m$ within d_3T_m .

$$\therefore \text{RMS}(i_{Q1}) = \sqrt{\left(I_{\text{ref1}}^2 + \frac{\Delta I_1^2}{12}\right) \times [d_{\text{CS}(1)}d_1 + d_{\text{CS}(2)}d_2] + \left(I_{\text{ref2}}^2 + \frac{\Delta I_2^2}{12}\right) \times d_{\text{CS}(3)}d_3} \quad (\text{C.9})$$

With similar argument, it is easy to show that, the average value of diode current is given by

$$\text{AVG}(i_{D1}) = I_{\text{ref1}} \{ [1 - d_{\text{CS}(1)}]d_1 + [1 - d_{\text{CS}(2)}]d_2 \} + I_{\text{ref2}}[1 - d_{\text{CS}(3)}]d_3 \quad (\text{C.10})$$

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