ECE322
Prof. Ahmed Madian
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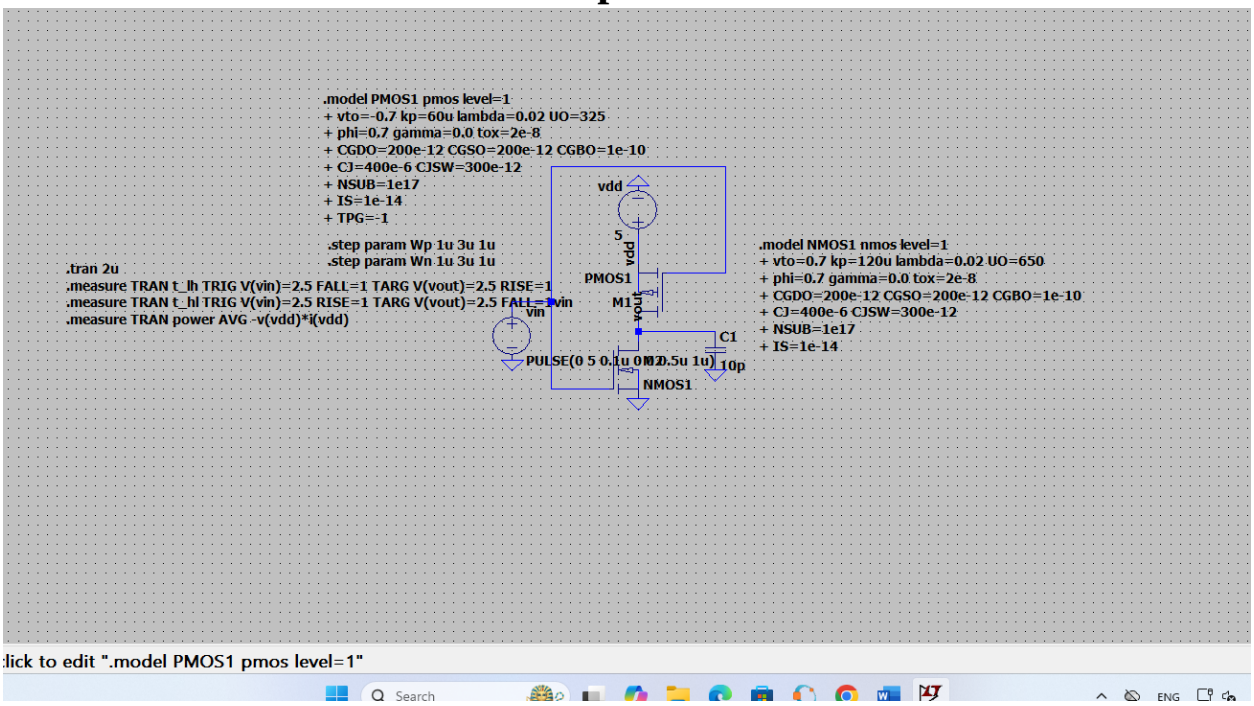
Day:		**Slot Number:**	

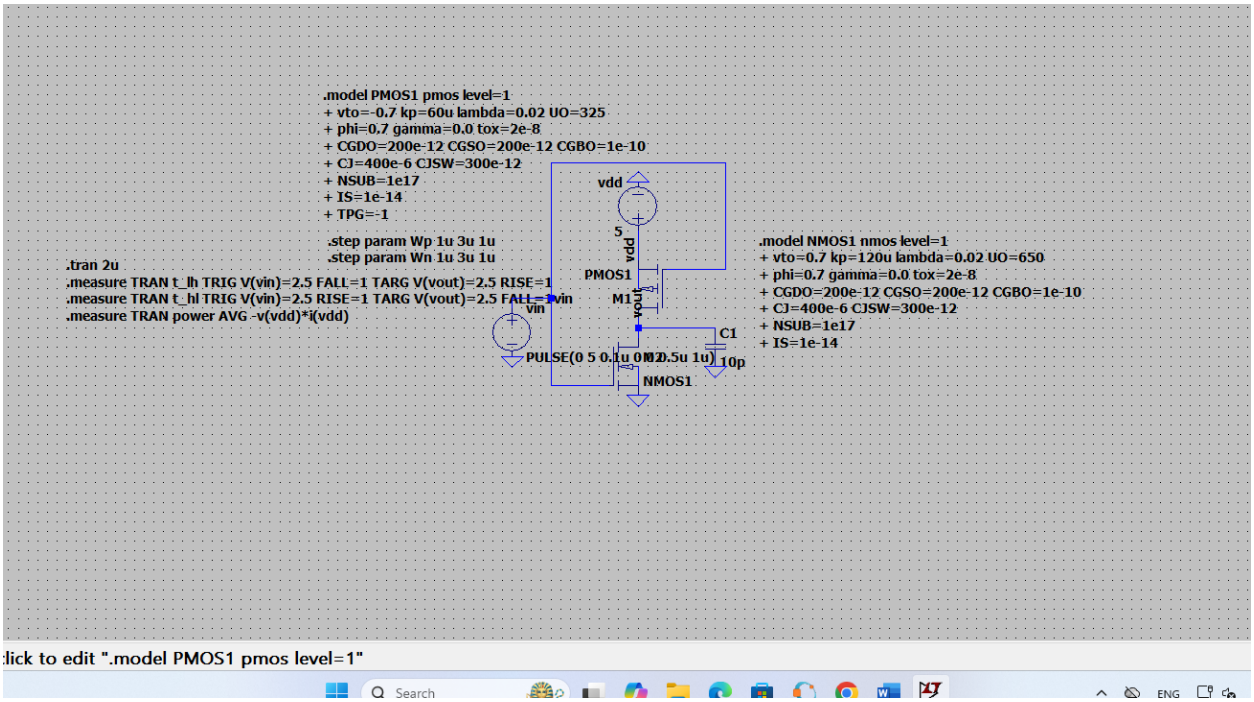
Lab 5

Requirements:

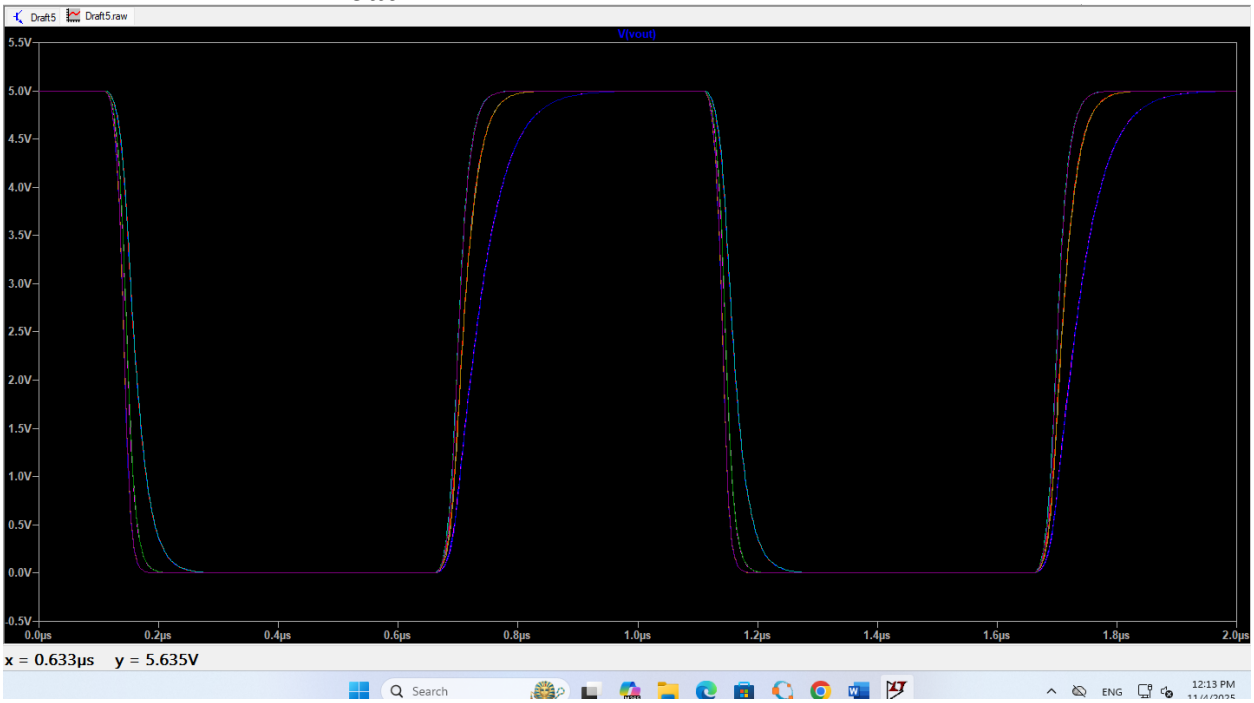
1) The Circuit Schematic from LTspice.



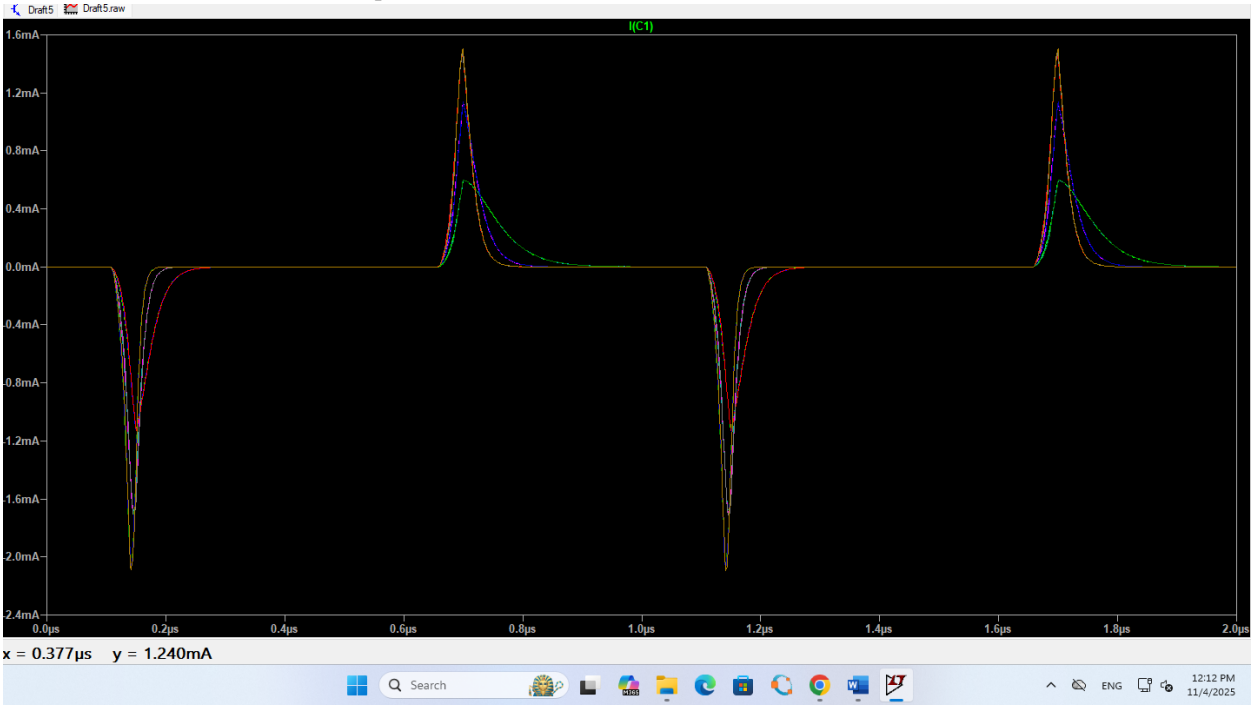
2) Screenshot of all the directives inserted.



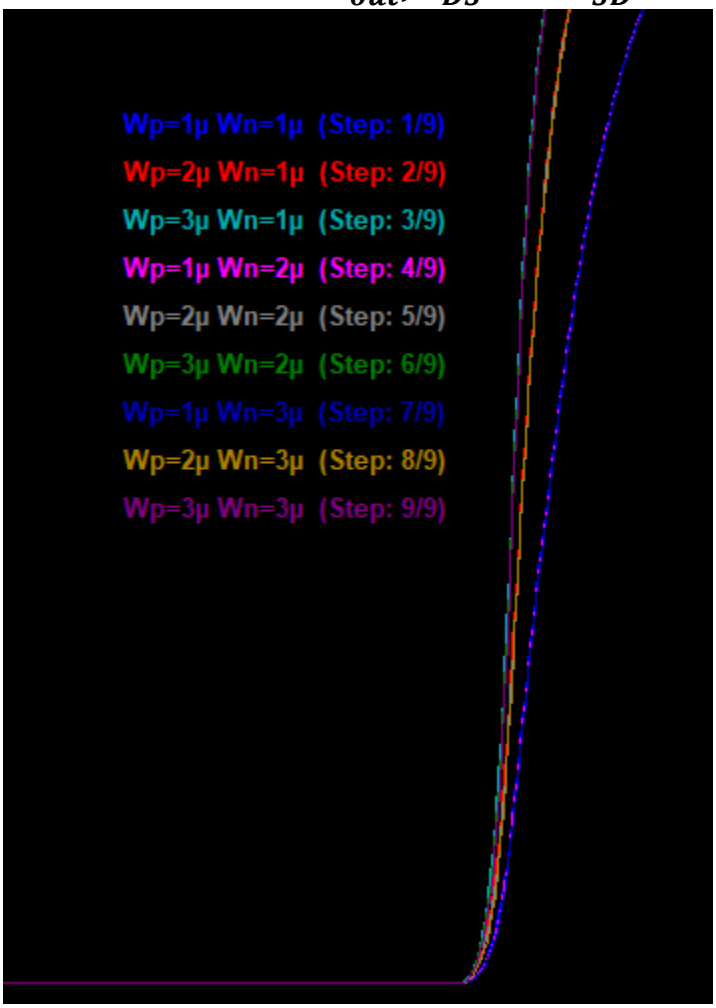
3) Transient Plot of V_{out}.



4) Transient Plot of I_{cap}.



5) Transient Plot of V_{out}, I_{DS} and I_{SD}.



6) Screenshot of the spice log with the results.

```
Measurement: t_lh
  step             t_lh                FROM                TO
     1             5.51181368683e-08   6.7500000025e-07    7.30118137119e-07
     2             3.30387663963e-08   6.74999999195e-07   7.08038765591e-07
     3             2.55458295318e-08   6.74999999486e-07   7.00545829018e-07
     4             5.5547477668e-08    6.74999999001e-07   7.30547476669e-07
     5             3.34385284774e-08   6.75000000467e-07   7.08438528945e-07
     6             2.59258628869e-08   6.74999999244e-07   7.00925862131e-07
     7             5.59105520194e-08   6.74999999173e-07   7.30910551192e-07
     8             3.37792394535e-08   6.74999999429e-07   7.08779238882e-07
     9             2.62516191003e-08   6.7499999982e-07    7.01251618921e-07

Measurement: t_hl
  step             t_hl                FROM                TO
     1             3.28098785479e-08   1.25e-07            1.57809878548e-07
     2             3.30430292737e-08   1.25e-07            1.58043029274e-07
     3             3.32496278333e-08   1.25e-07            1.58249627833e-07
     4             2.12277500837e-08   1.25e-07            1.46227750084e-07
     5             2.14601176366e-08   1.25e-07            1.46460117637e-07
     6             2.16679563455e-08   1.25000001062e-07   1.46667957408e-07
     7             1.6191863218e-08    1.25000000596e-07   1.41191863814e-07
     8             1.64546835819e-08   1.25000001192e-07   1.41454684774e-07
     9             1.6699377796e-08    1.25000000959e-07   1.41699378755e-07

Measurement: power
  step             AVG(-v(vdd)*i(vdd)) FROM                TO
     1             0.000252937333097   0                   2e-06
     2             0.000255576875793   0                   2e-06
     3             0.000257803057872   0                   2e-06
     4             0.000255212106297   0                   2e-06
     5             0.000259805856874   0                   2e-06
     6             0.000263792932307   0                   2e-06
     7             0.000257033234328   0                   2e-06
     8             0.000263289393567   0                   2e-06
     9             0.000268751702322   0                   2e-06
```

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Questions:

1) **What are the values of Wp and Wn to ensure symmetric delay ($t_{hl} = t_{lh}$)?**
   0.03303u
2) **What do t_{hl} and t_{lh} depend on from the results in 6)?**
   THL depends of wn and TLH depends on wp,

3) **From the plot in 5), what is the small current running through the other transistor called?**
   Short circuit

4) **Calculate the PDP for the symmetric step in 1) and step 4.**

   Step 2: 8.1056*10^-12
   Step 4: 9.79693*10^-12