**IR Design**

If (=”0”) {

Check for:

If “0” 🡪 LDD

If “1” 🡪 STD

} Else {

Check for:

If “00” 🡪 ADD/ SUB/ AND/ OR/ CALL/ Int

Else If “01” 🡪 NOT/ NEG/ INC/ DEC/ RLC/ RRC/ MOV

Else If “10” {

Check for:

If “0” 🡪 LDM/ SHL/ SHR/ NOP

If “1” 🡪 RET/ RTI/ PUSH/ POP

} Else If “11” {

Check for:

If “0” 🡪 JMP/ JC/ JZ/ JN

If “1” {

Check for:

If “0” 🡪 SETC/ CLRC

If “1” 🡪 IN/ OUT

}

}

}

**3-Operands instructions:**

1. ADD, SUB, OR, AND

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Rdst1 | 3 bits  Rsrc1 | 3 bits  Rsrc2 | 5 bits  OpCode |

1. CALL

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Rdst | 3 bits  111 | 3 bits  110 | 5 bits  OpCode |

**2-Operand instructions:**

1. Move instruction

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Rdst | 3 bits  Rsrc1 | 3 bits  Zeros | 5 bits  OpCode |

1. Normal 1-Operand

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Rdst | 3 bits  Rdst | 3 bits  Zeros | 5 bits  Opcode |

1. Memory instruction
   1. Load

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 4 bits  Rdst | 10 bits  EA | 0 |

* 1. Store

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0 | 4 bits  “0”+EA[9:7] | 3 bits  Rsrc | 7 bits  EA[6:0] | 1 |

1. PUSH

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Zeros | 3 bits  Instruction operand (Rdst) | 3 bits  110 | 5 bits  OpCode |

1. POP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Instruction operand (Rdst) | 3 bits  Zeros | 3 bits  110 | 5 bits  OpCode |

1. Immediate value instruction

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Rdst | 6 bits  Zeros | 5 bits  OpCode | IV is in the next word |

**1-Operand instruction:**

1. Jump

|  |  |  |  |
| --- | --- | --- | --- |
| 1 | 4 bits  Rdst | 6 bits  Zeros | 5 bits  Opcode |

1. RET/RTI

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Zeros | 3 bits  Zeros | 3 bits  110 | 5 bits  OpCode |

1. OUT

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Zeros | 3 bits  Instruction operand (Rdst) | 3 bits  Zeros | 5 bits  OpCode |

1. IN

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Instruction operand (Rdst) | 3 bits  Zeors | 3 bits  Zeros | 5 bits  OpCode |

**0-Operand Instruction:**

|  |  |  |
| --- | --- | --- |
| 1 | 10 bits  Zeros | 5 bits  Opcode |

**INT**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 4 bits  Zeros | 3 bits  010 | 3 bits  110 | 5 bits  OpCode |