Solution:

Multiply-Accumulate circuit (MAC) with Dadda reduction scheme to multiply two 16-bit unsinged integer operands and add it to a 32-bit unsigned accumulator is implemented in VHDL and simulated using **Quartus Prime lite 18.1** edition.

Brent Kung adder implemented in Assignment-3 is used for final addition in MAC reduction

MAC with Dadda reduction dot diagram is given in the following Figure 1 to Figure 2

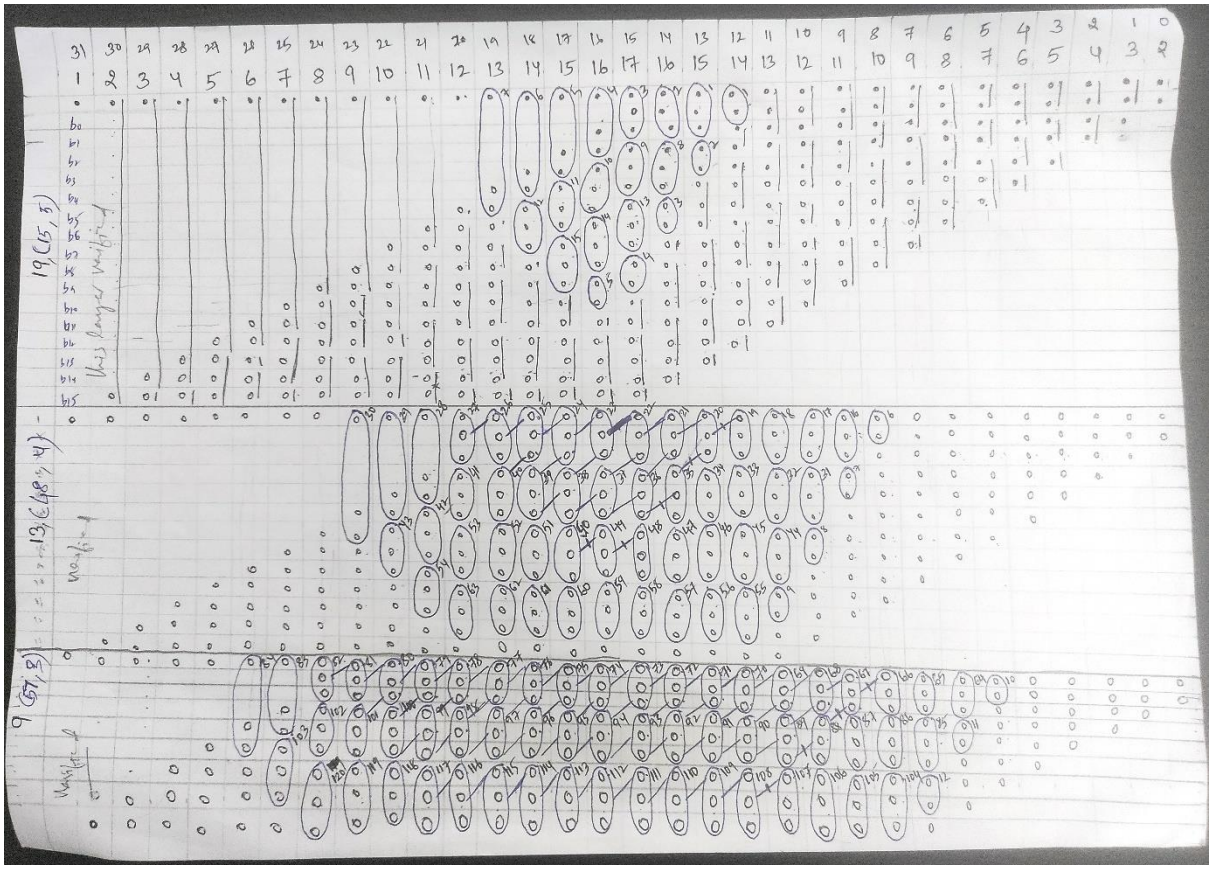

Figure 1 MAC Dadda reduction dot diagram (first 3 layers)

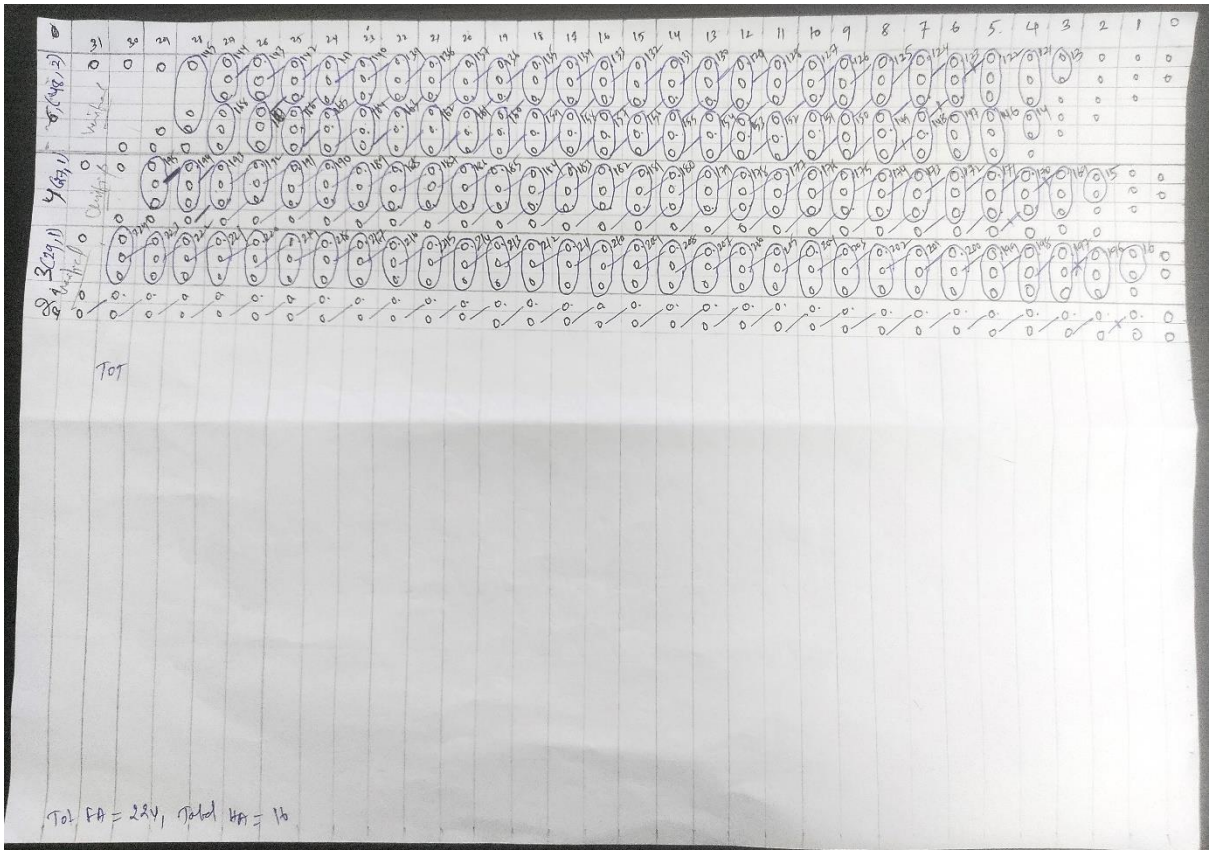

Figure 2 MAC Dadda reduction dot diagram (last 4 layers)

Input File

Input file contents are shown in theFigure 3.

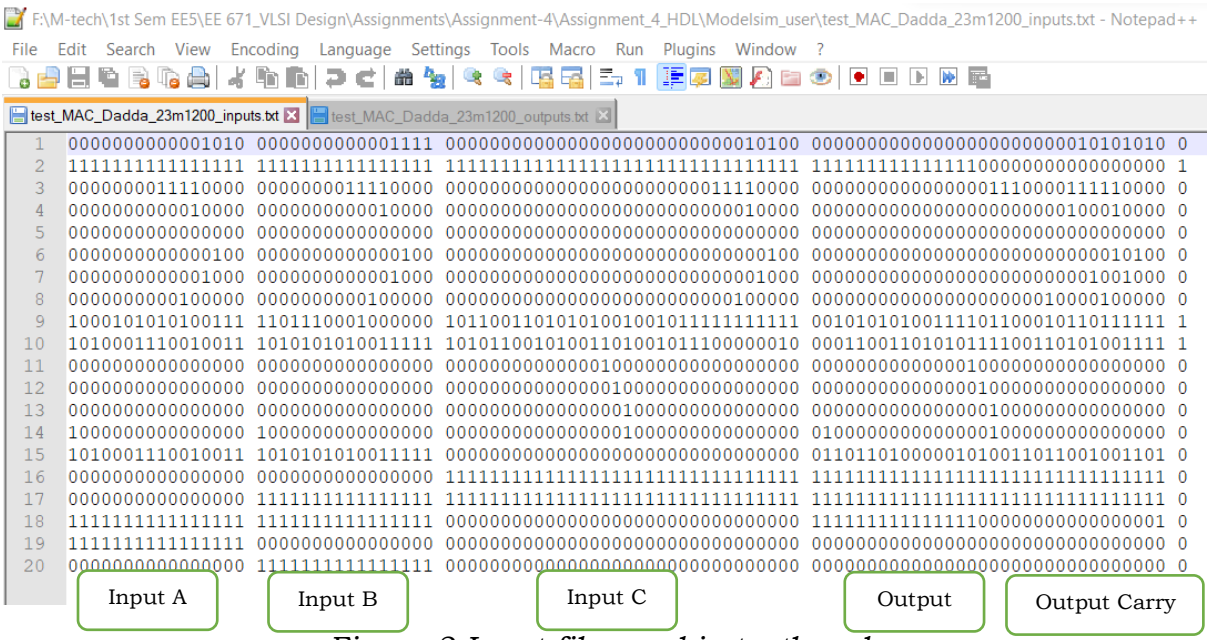

Figure 3 Input file used in testbench

Output File

Output file contents are shown in theFigure 4.

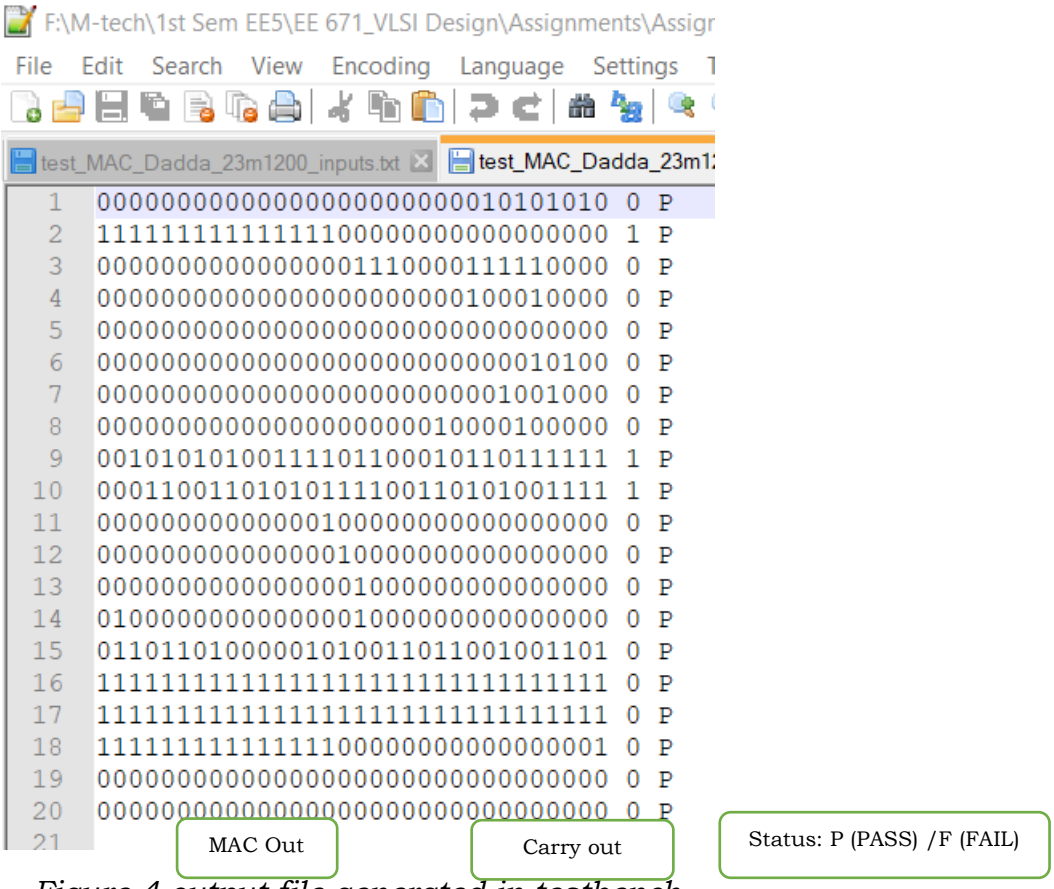

Figure 4 output file generated in testbench

Simulated result in waveform is shown in the Figure 5

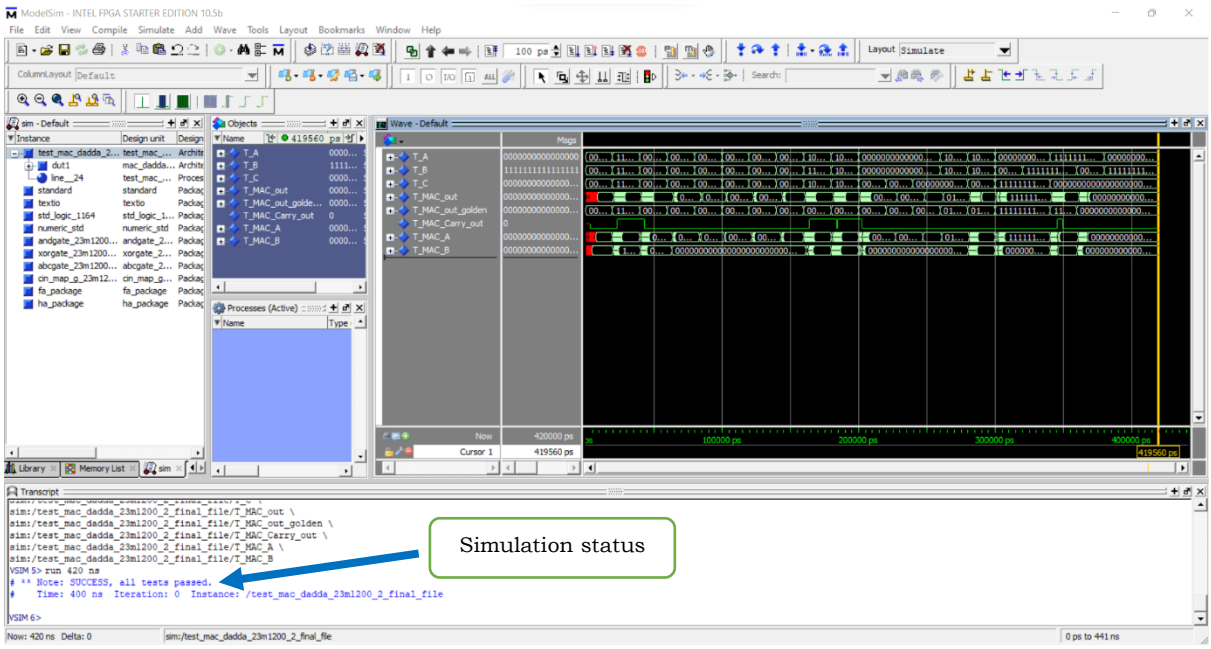

Figure 5 Simulated waveform of stimuli

Note: VHDL program files are attached separately.