Asynchronous FIFO

Synthesis Report:

Flow Status	Successful - Wed Aug 14 18:57:30 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	asyncfifo
Top-level Entity Name	asyncfifo
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	49
Total pins	24
Total virtual pins	0
Total block memory bits	128
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Simulation Result: