Single Cycle MIPS CPU

Synthesis report:

Flow Summary

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Flow Status	Successful - Wed Aug 14 22:03:13 2024
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	MIPS_VHDL
Top-level Entity Name	MIPS_VHDL
Family	Cyclone IV E
Device	EP4CE22F17C6
Timing Models	Final
Total logic elements	7,853
Total registers	4240
Total pins	34
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	1
Total PLLs	0

Simulation result: