THE UNIVERSITY OF ADELAIDE
AUSTRALIA

School of Electrical & Electronic Engineering
Adelaide, South Australia, 5005

ELEC ENG 4039A/B
Honours Project
A Radio Relay System for Remote Sensors in the Antarctic

Supervisors: Dr. Chris Coleman, Dr Said Al-Sarawi

Interim Progress Report

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Date Submitted: June 3, 2010
Signature of Supervisor:

Abstract

This report describes the current progress of the radio relay system project. Over the past semester much design work has been accomplished, and construction and testing of the first prototype has begun.

Contents

1 High Level Design

The high level design for the project has been slightly changed from the design shown in the Stage 1 Design Document (Appendix A). As no information about the existing sensor equipment has been received, the decision was made to make the data tap section of the project more generic. Focus will be placed on providing a set of libraries for the micro-controller, to enable recording of data from a range of inputs.

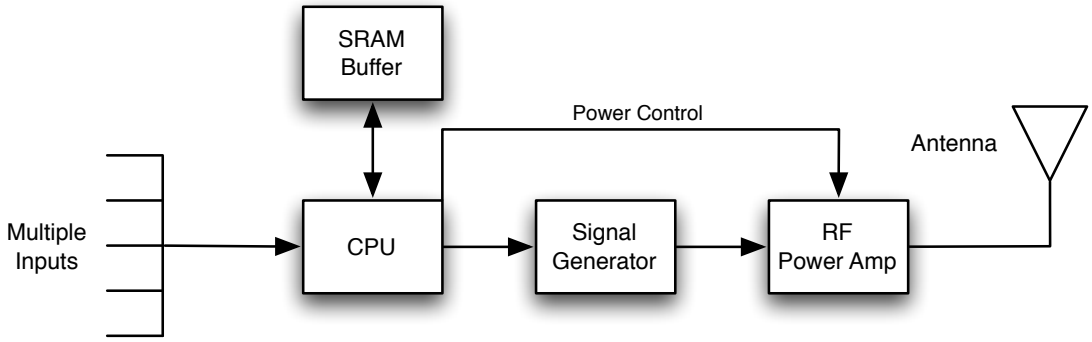

Figure 1: Updated Block Diagram

2 Processor Choice

After looking at a range of processors from the Texas Instruments and Atmel families, the Atmel AT-XMEGA128A1 processor was chosen to be the heart of the project. The AT-XMEGA is a 8-bit RISC processor with a clock speed of up to 32MHz. It has 128Kb of program Flash memory, and 8Kb of SRAM. 9×8-bit general purpose input/output (GPIO) lines are available for use.

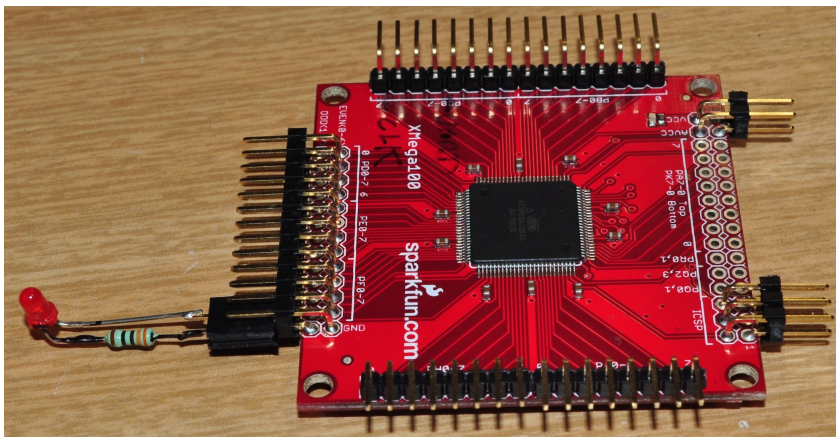

Figure 2: AT-XMEGA128A1 Breakout Board

A key feature is the ability to attach SRAM or SDRAM to either 2 or 3 of the GPIO ports (depending on RAM size), and have the RAM appear at the end of the micro-controllers memory space. This will

allow easy creation of a large buffer space for storing collected data. Of course, attaching extra RAM will reduce the number of GPIO pins available for data collection, but the number of pins remaining ($5 \times$ 8-bit ports, allowing for 3-port RAM and 1-port for transmitter control) is still considerable. Functionality available from the remaining ports includes 5 UARTs, 16 multiplexed ADC inputs, and 2 DAC outputs.

Power usage of the chip averages around 18.5mA in active mode when operating at 32MHz, down to 0.7mA operating at 1MHz. In power-save mode, where only the internal 32KHz RTC (Real-Time Clock) oscillator is active, the chip draws only 0.55μA. As the transmitter will be operating on a small duty cycle (approx. 1 hour per day), the chip will be in this mode most of the time.

An AT-XMEGA128A1 breakout board has been purchased at a cost of $30.80 from Sparkfun Electronics. This board breaks the 100-pin TQFP out to 0.1' pitch pin-headers, for easy prototyping. The final prototype will have everything on one board, but this breakout will help immensely for getting things working in the meantime.

2.1 Cold Testing

To test the suitability of the AT-XMega128A1 for use in cold climates, the breakout board was cooled using dry ice. Operating off an internal 32MHz RC oscillator, the chip reached -54°C, and was still completely operational. The only point of note was that the internal oscillator's frequency drifted up by 1MHz. Further tests will be conducted using crystal oscillators, and the internal RC oscillator.

The secondary purpose of these tests was to determine if cold temperatures would cause warping of PCBs. Two multi-layer PCBs provided by Mr Pavel Simcik were left uninsulated in dry ice while testing of the XMega was underway. Retrieved from the dry ice a day later, the boards showed no sign of deformation.

More information on the testing process is provided in Appendix B.

3 Signal Generator Design

The RF signal is generated by an Analog Devices AD9834 Direct Digital Synthesis (DDS) IC. When supplied with a 50MHz master clock the DDS IC can generate sine waves between DC and 25MHz, and is programmable via a SPI (Serial Peripheral Interface).

Two frequency registers are available, and the IC can switch between them using input from an IO pin, facilitating easy FSK (Frequency Shift Keying) modulation. Additionally, two phase registers and a corresponding IO pin allow easy BPSK (Binary Phase Shift Keying) modulation.

As the chip is produced in a SMD form factor (TSSOP-20), a small breakout board was purchased to break out the SMD chip to pin headers. A PCB was then designed using all through-hole components for easy construction. It is expected that this board will be working by the end of Week 13, Semester 1.

The PCB schematic and artwork appears in Appendix C.

4 Power Amplifier Design

The output from the signal generator is very low, around -40dBm, and hence needs to be amplified to be usable. A class C MOSFET based power amplifier will be the final stage of the amplifier, but the signal from the DDS still needs to be amplified before this stage. To do this, a dual op-amp based circuit based on the Analog Devices AD8008 will be used. The gain of this amplifier will be adjustable using a digital potentiometer, which is itself controlled from the central micro-controller. If all goes well, the output from the PA should be adjustable from approximately 500mW up to 5W.

5 Antenna

For placement in the field, a simple dipole antenna, or some form of broadband antenna will still be used. Unfortunately due to space restrictions such an antenna cannot be erected at the University. Instead a commercial HF antenna will be purchased, most likely a Comet CHA-250B[1], a wide-band HF vertical. This antenna is effectively a giant loading coil, and will not perform as well as a dipole, but with a good ground it will be adequate. The antenna will be mounted on top of the Engineering North building, and will be usable for many other projects for years to come.

Since the antenna is rather expensive (∼USD$450), any budget remaining after component purchases will be put towards it, with the remaining funds sourced elsewhere.

6 Software Design

As stated in Section 1, the software side of the project has become more generalised due to lack of information about the existing hardware. To this end, much of the software work will be devoted to providing a set of libraries to record and transmit data.

The software can be thought of as a series of layers on top of the underlying hardware, with each layer acting to abstract functionality away into simple function calls.

6.1 Software Modules

6.1.1 Transmitter Control

This section can be thought of as the lowest level of the software. It will provide functions to enable and disable the signal generator, program frequencies, and switch between frequency registers (hence

[1] http://www.cometantenna.com/products.php?CatID=1&famID=5&childID=6

modulating the output). If a viable power control system is implemented, then this section will also set output power levels.

6.1.2 Modulation

The next layer up from the transmitter control. This layer will implement various modulation schemes, which can be used in different environments. Simple FSK can be used for transmitting large segments of data (∼263kB/hr), while other modes like MFSK can be used for transmitting smaller amounts of data, but with much greater reliability.

If time permits, it may be worthwhile to implement JT65[2], a very low data-rate mode that can be demodulated with a signal-to-noise ratio of −27dB. This would be a good way to signify that the transmitter is still functional, even in extremely bad radio conditions.

6.1.3 Transmitted Data Structure

To be able to compile data from multiple sources into one transmission, some form of data structure must be devised. This will incorporate some form of packet header with information about the payload data. Checksums should be included to verify received data, and other forms of error correction may be included.

6.1.4 Data Sampling

The free GPIO pins allow collection of data from many different sources, such as ADCs and UARTs. Other data sources, such as from a parallel data bus can be sampled using interrupts. A few different serial standards, such as SPI or I2C can be implemented, using pre-existing libraries.

Various functions will need to be coded to provide easy ways to collect data, package it into some form of standard payload, and then insert it into the transmission packet.

6.2 Timing

Accurate timing is required for two sections of this project: keeping an accurate clock for modulating data, and making sure transmissions occur at regular intervals.

The XMega contains a high accuracy 32.768kHz Real-time clock crystal for timekeeping, but it is possible that this will drift with temperature causing a system clock to become inaccurate over the course of a few months. The degree of inaccuracy can only be determined by testing.

In the Antarctic research application, a GPS receiver will be connected to the system. Since the GPS provides accurate timing data, this provides a means to re-synchronise a system clock at regular intervals.

[2]Joe Taylor, K1JT (September-October 2005). "The JT65 Communications Protocol" `http://physics.princeton.edu/pulsar/K1JT/JT65.pdf`

Since the transmitter will send data at least once a day, it may be possible to compensate for clock drift on the receiving end, reducing complexity in the transmitter. Slight deviations in transmission bit-rate can also be compensated for at the receiving end.

7 Testing

As mentioned in Section 2.1, testing of some components at cold temperatures has already been conducted, but much more testing is still needed. All of the RF stage will need to be tested at low temperatures to determine how the gain changes, or if any of the amplifiers become unstable. More XMega clock options need to be tested, to find the clock source with highest accuracy over a wide range of temperatures.

To test the transmitter within Australia, it will need to be operated on the amateur radio bands (80m or 40m wavelength), since transmission on the 6MHz ISM band is not permitted. To transmit on these bands using non-commercial equipment, an advanced amateur license will be required. The projects supervisor (Dr. Chris Coleman) has the necessary license, but to avoid him needing to be present for each test I (Mark Jessop) will attempt to gain an amateur license over the semester break.

8 Schedule Status

Table 1 shows the project schedule, and which tasks have been completed. The project is currently on schedule, and is on track to be completed in time for the final seminar during the Semester 2 Mid-Semester break.

9 Budget Status

As of Week 12 Semester 1, $75.80 of the $250 budget has been spent, leaving $174.20 remaining. It is anticipated that very little of the remaining budget will need to be spent, as the majority the required components have already been bought.

A cost breakdown appears below:

- AT-XMega128A1 Breakout Board - $30.80
- AD9834 DDS IC $\times$ 2 - $26.30
- TSSOP-20 to Pin Header Breakout Board - $13.70
- Dry Ice for cold testing - $\sim$$5

Table 1: Project Timeline

Task	**Completion Date**
	Semester 1
Background Research	COMPLETE
High-level Design	COMPLETE
Project Sizing & Simulation	COMPLETE
Component Testing	Partially Complete
Hardware Design	
CPU & Buffer	COMPLETE
RF Signal Generator	COMPLETE
RF Power Amplifier	In Progress
Data Tap	On Hold
	Semester 2
Antenna Design	Week 1
Software	In Progress
Prototype Completion	Week 3
Testing & Optimisation	Week 7

Appendices

A Original High-Level Overview

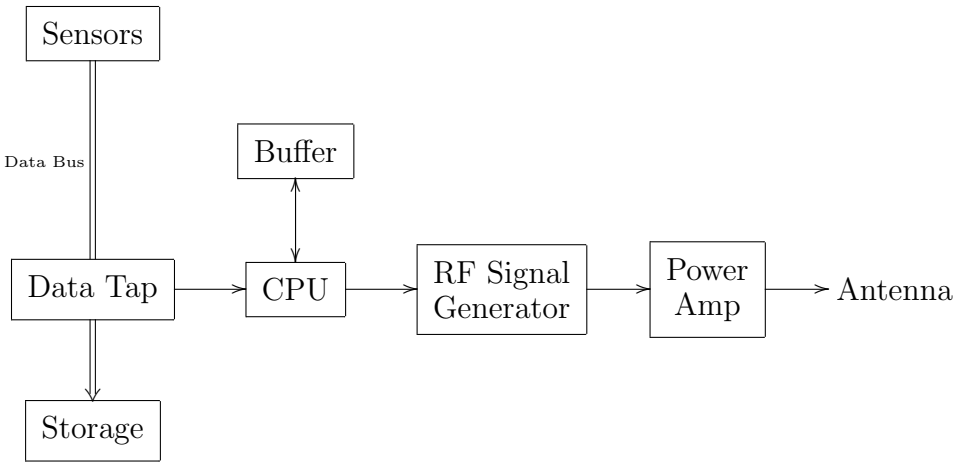

Figure 3: Original High-Level Block Diagram

B Dry Ice Testing

To test the AT-XMEGA128A1 breakout board the chip was programmed to output the internal clock signal on a GPIO pin, and one of the UARTs was programmed to continually send out "Hello World" at 9600 baud. A LED was also attached to the board, and the chip programmed to flash it as 1Hz. The breakout board assembly was wrapped in bubble wrap (for insulation) with a ribbon cable exiting the insulation to carry the data lines. The insulated board was then placed in a small foam Eski containing approximately 3KG of dry ice. Over the course of an hour, the chip cooled down to -49°C, where it stayed for approximately 20 minutes. After shuffling the dry ice slightly, the chip cooled down a further 5°C, to -54°C at which point the test was aborted. Throughout the test the clock frequency and chip temperature were measured, to produce the plot in Figure 4.

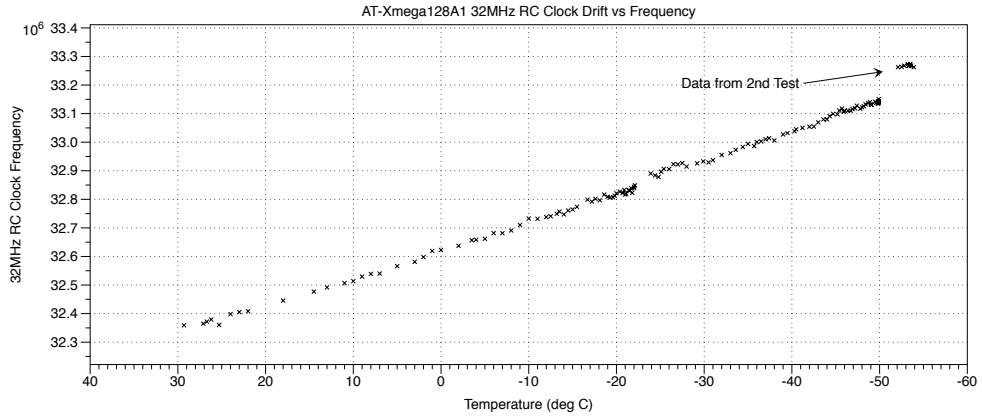

Figure 4: AT-XMEGA128A1 RC Clock Drift

Figure 5: AT-XMEGA128A1 Breakout Board Wrapped in Insulation

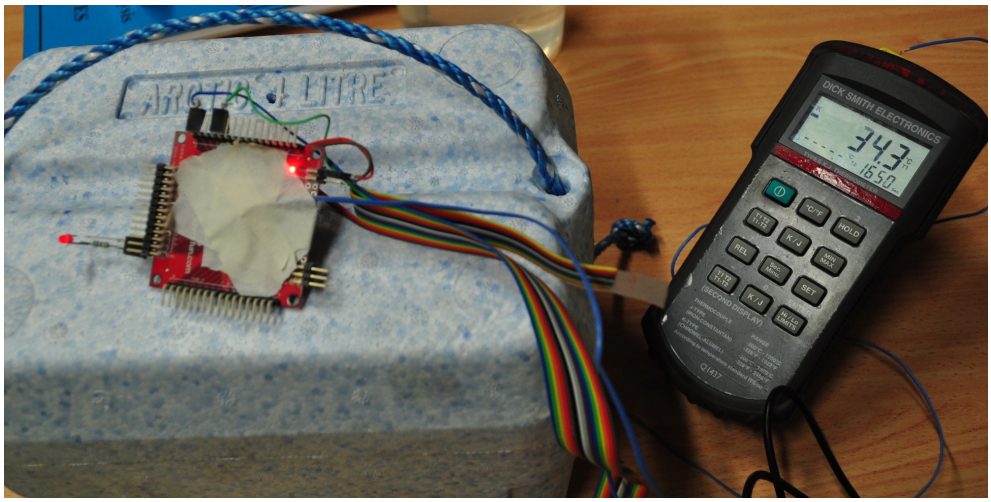

Figure 6: AT-XMEGA128A1 Breakout Board Warming up after testing.

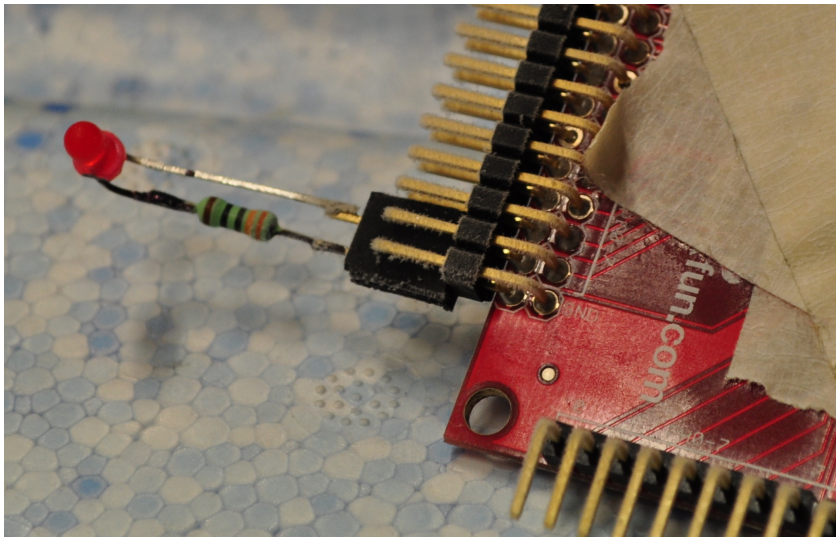

Figure 7: Ice forming on the XMEGA's pin headers after testing.

C AD9834 Breakout Board

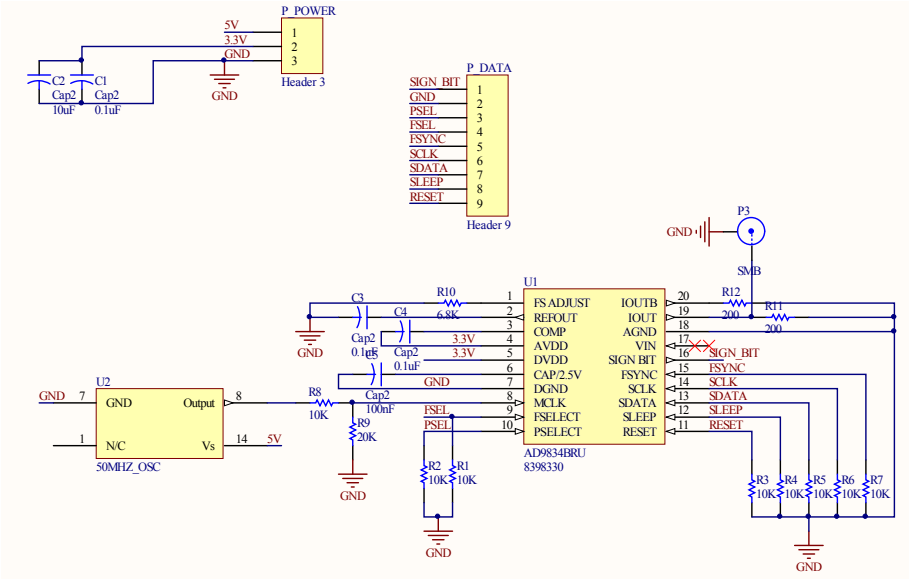

Figure 8: AD9834 Breakout Board Schematic

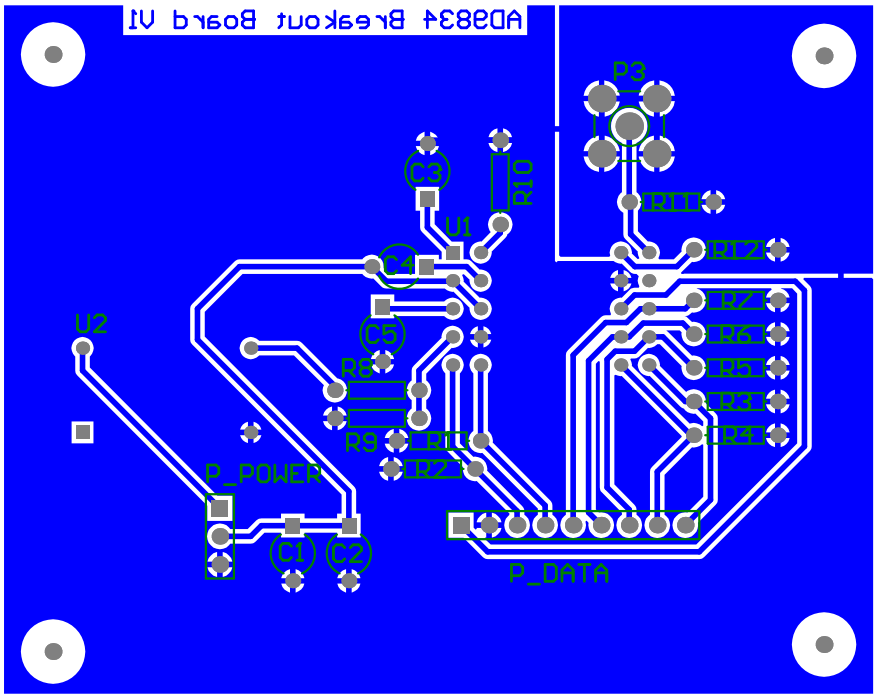

Figure 9: AD9834 Breakout Board PCB Artwork