Monochrome Bitmap Display Controller (MBDC)

Overview

The Aves monochrome bitmap display controller generates an 800 x 512 monochrome display on an SVGA compatible monitor.

Initial Prototype Features

- Standard: VESA SVGA
- Resolution: 800 x 512
- Pixel clock 40MHz
  - 1 x 74AC163 Sync Counter
  - 2.5MHz 'Character Clock'
  - 10MHz Phi2
- MC6845 CRTC
- Display Buffer: 2 x 32KB SRAM
  - 2 X 74HC245 octal bus transceiver
- 15 Bit video address (VA0-VA14)
  - VA0-VA6 ⇒ CRTC MA0-MA6
  - VA7 ⇒ CRTC RA0
  - VA8-VA14 ⇒ CRTC MA7-MA13
  - 2 x 74HC541 octal tristate buffer
- Horizontal scrolling register
  - 1 x 74HC273 8 bit latch
  - 2 x 74HC283 4 bit adder
- Display Timing and Control
  - 1 x ATF22V10-10
  - 1 x 74AC74
  - 1 x 74AC02
  - 2 x 74HC166
  - 1 x 74AC157

RGB Outputs

```
--[430]--+--[75]--
         |
       [150]
         |
```

CPLD Implementation

Primary CPLD (ATF1508)

Core Functionality (20MHz)

- Address generation (17-bit)
- Memory interface (256KB/128KW)
- Horizontal/Vertical scroll
- Bank switching
- Hardwired timing generation (replacing MC6845)

Memory Organization

- 256KB frame buffer
- Accessible as 128K words
- Supports both display modes
- Real-time mode switching
- Multiple screen buffers

Secondary CPLD

Core Functionality

- Mode switching control
- Palette RAM interface
- Shift register implementation
- RGB output generation

Display Modes

Monochrome Mode (800x512)

- 1 bit per pixel

- Maximum resolution
- Direct pixel output
- Full screen requires 51.2KB

Color Mode (400x256)

- 2 bits per pixel
- 4 colors per pixel
- 16 palette registers
  - 8-bit RGB values per register
- Full screen requires 25.6KB

Features

- Real-time mode switching
- Independent palette updates
- Scanline boundary switching
- Special effects capability
- 20MHz input clock

Common Features

- Identical memory interface
- Compatible timing generation
- Shared scroll logic
- Bank switching support
- Flexible display options