```
clock in : 0000000011111111
slot 5   : 1111100000000111
slot 6   : 1111110000000011
slot 7   : 1111111000000001
ready    : 1111100011111111
BA,VACC  | 1111110011111111
```

```
// Timing Diagram (Textual Representation - Improved)

// Time Slots:     0   1   2   3   4   5   6   7   0   1   2   3   4   5   6   7
// Phi2 (Clock):      _   _   _   _   _   _   _   _   _   _   _   _   _   _   _
//                 |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |


// VIC (Clock):    |_____________________________|                             |

// Slot 5:         _________________.   .   .   .   .   .   .   ._________________
//                 .   .   .   .   |_____________________________|

// Slot 6:         ___________________.   .   .   .   .   .   .   ._________
//                 .   .   .   .   .   |_____________________________|

// Slot 7:         _______________________.   .   .   .   .   .   .   ._______
//                 .   .   .   .   .   .   |_____________________________|

// READY:          ________________                              _______________
//                 .   .   .   .   |_____________________________|   .   .  .  .


// BA, VACC                          __________
//                 _________________|          |_______________________________


// Explanation:

// - Each column represents a time slot.  There are 8 time slots per Phi2 cycle.

// - The "_" and "/" characters are used to approximate the high and low states
//   of the signals.  A continuous "_" represents a high state, and a "\" or "/"
//   represents a transition.

// - Phi2 is the main clock.

// - Slots 5, 6, and 7 are the outputs of the shift register.  Notice how they
//   are offset in time.

// - READY is low when *either* Slot 5, 6, or 7 is high *or* VIC Phi2 is high.

// - BA and VACC are high when *either* Slot 6 or 7 is high.
```

```
// - This diagram shows the *general timing relationship*.  The *exact*
//   timing (pulse widths, etc.) will depend on the frequency of the
//   shift register clock and the specific taps you choose.

// - This is still a simplified representation. A true timing diagram
//   would show more precise timing information and would likely be
//   graphical.
```

```
clock in : 0000000011111111
slot 5   : 1111100000000111
slot 6   : 1111110000000011
slot 7   : 1111111000000001
ready    : 1111100011111111
BA,VACC  | 1111110011111111
....

[literal]
....
// Time Slots:     0   1   2   3   4   5   6   7   0   1   2   3   4   5   6   7
// Phi2 (Clock):      _   _   _   _   _   _   _   _   _   _   _   _   _   _   _
//                 |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |_| |


// VIC (Clock):    |_____________________________|                             |

// Slot 5:         _________________.   .   .   .   .   .   .   ._________________
//                 .   .   .   .   |_____________________________|

// Slot 6:         ___________________.   .   .   .   .   .   .   ._________
//                 .   .   .   .   .   |_____________________________|

// Slot 6:         _________________________.   .   .   .   .   .   .   ._______
//                 .   .   .   .   .   .   |_____________________________|

// READY:          ________________                              _______________
//                 .   .   .   .   |_____________________________|   .   .  .  .


// BA, VACC                          __________
//                 _________________|          |_________________________________
```

NOTE

Explanation:

- Each column represents a time slot. There are 8 time slots per Phi2 cycle.
- The "*" and "/" characters are used to approximate the high and low states of the signals. A continuous "*" represents a high state, and a "\" or "/" represents a transition.

- Phi2 is the main clock.
- Slots 5, 6, and 7 are the outputs of the shift register. Notice how they are offset in time.
- READY is low when **either** Slot 5, 6, or 7 is high **or** VIC Phi2 is high.
- BA and VACC are high when **either** Slot 6 or 7 is high.
- This diagram shows the **general timing relationship**. The **exact** timing (pulse widths, etc.) will depend on the frequency of the shift register clock and the specific taps you choose.
- This is still a simplified representation. A true timing diagram would show more precise timing information and would likely be graphical.

VIC Memory Access Timing Design

Overview

The design provides precisely timed memory access slots for the VIC chip while maintaining synchronization with both the VIC clock and color clock domains.

Clock Relationships

- VIC Clock: 7.88MHz (≈127ns period)
- Color Clock: 17.73MHz (≈56.39ns period)
- Ratio: 2.25:1
- Phase offset: 7ns per cycle

Design Elements

Shift Register

- Clocked by 17.73MHz color clock
- Generates three sequential slots (5, 6, and 7)
- Each tap provides initial wide pulses
- Progressive timing reduction through stages:
  - Slot 5: 35ns reduction
  - Slot 6: 28ns reduction
  - Slot 7: Subsequent reduction

Clock Synchronization

- Shift register outputs OR’d with VIC clock
- Ensures rising edge synchronization with VIC
- Guarantees trailing edge timing
- Prevents pulses from becoming too narrow

Timing Margins

- RAM requirement: 55ns
- Slot 6 example:
  - Base pulse: 169ns
  - Reduction: 28ns
  - Final width: 141ns
  - Margin: 86ns above requirement

Key Benefits

- Reliable RAM access timing
- Maintained synchronization with VIC
- Generous timing margins
- Robust against clock domain interactions

Implementation

The design uses standard TTL components: * 17.73MHz crystal oscillator * Shift register for slot generation * OR gates for clock combination

This elegant solution provides precise memory access timing while bridging two clock domains, maintaining both reliability and synchronization.

/*** * Video Memory Access Controller (VMAC) * * Purpose: * Controls memory access arbitration between the CPU and video controller * supporting VIC (6561), VIC-II (6569), and TED (7360/8364) timing * requirements. * * Timing Generation: * - External shift register delays the AEN signal * - Delayed AEN is OR’ed with original AEN to create timing slots * - This creates a pulse at the end of each clock cycle * - tsa/tsb are derived from this delayed timing chain * * VIC-II (6569) Operation: * - AEN indicates when VIC-II has control of the bus * - Can occur in both clock phases * - Shift register must use chroma clock for consistent timing * * VIC (6561) Operation: * - Video access occurs only during PHI1 (clock phase 1) * - PHI2 clock is used as input for AEN * - Phase-locked timing simplifies bus arbitration * * TED (7360/8364) Operation: * - Single 17.73MHz chroma clock source (PAL) * - System clock derived as 1.76MHz (÷10) or 0.88MHz (÷20) * - Video access during PHI1 like VIC * - Always 0.88MHz during video display * - Shift register must use chroma clock for consistent timing

* - Clock division handled by TED internally */

Video Memory Access Controller Discussion

Overview

Analysis of the VMAC design using aves-video-2.pld for VIC, VIC-II and TED support.

Key Points

- Single GAL design works for all three video chips
- Uses 10-bit shift register for timing generation
- Operates from 17.73MHz chroma clock

Timing Details

- Full cycle is 20 chroma clocks
  - Each phase (PHI1/PHI2) is 10 cycles
  - 17.73MHz ÷ 20 = 0.88MHz for TED
- Only using 8 bits of shift register
  - Last 2 fastest bits not needed
  - Slot 6 controls READY
  - Slot 7 provides ~113ns margin

Video Chip Support

VIC (6561)

- PHI2 connected to AEN input
- Timing from slots 6/7

VIC-II (6569)

- Direct AEN connection
- Timing from slots 6/7

TED (7360)

- Clock-derived AEN
- Same slot 6/7 timing

- ~113ns margin from slot 7
- READY control from slot 6

GAL Equations

```
ready = (tsa # aen) & iordy & exrdyin;
vacc  = !(tsb # aen);
exrdy = exrdyin & ready;
exba  = (tsb # aen);
```

Key Benefits

- No GAL changes needed between chips
- External shift register handles timing differences
- Clean bus arbitration for all video chips