

An experimental analysis of loop pipelining techniques on SIMD-like architectures^{*}

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Abstract

1. Introduction

General intro

Background on CP and modulo scheduling...

2. Related Work

3. Approach

3.1 Scheduling one iteration

3.2 Scheduling several iterations simultaneously

3.2.1 Overlapping (Chenxin's way)

3.2.2 Modulo scheduling

3.2.3 Unrolling and modulo scheduling

4. Experiments and evaluation

comparisons... (of which measures?)

4.1 Average throughput

4.2 Code size

4.3 Burstiness

4.4 Reconfiguration

4.5 Scheduling time

5. Experimental analysis

6. Conclusions and future work

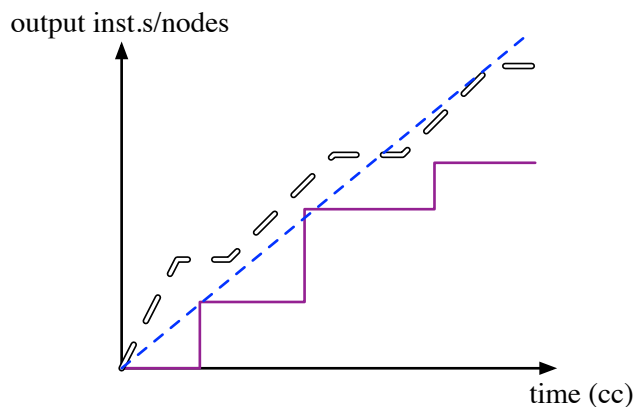


Figure 1: Burstiness

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