|  |  |
| --- | --- |
| Name: Muhammad Ali Ahmad | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-029 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

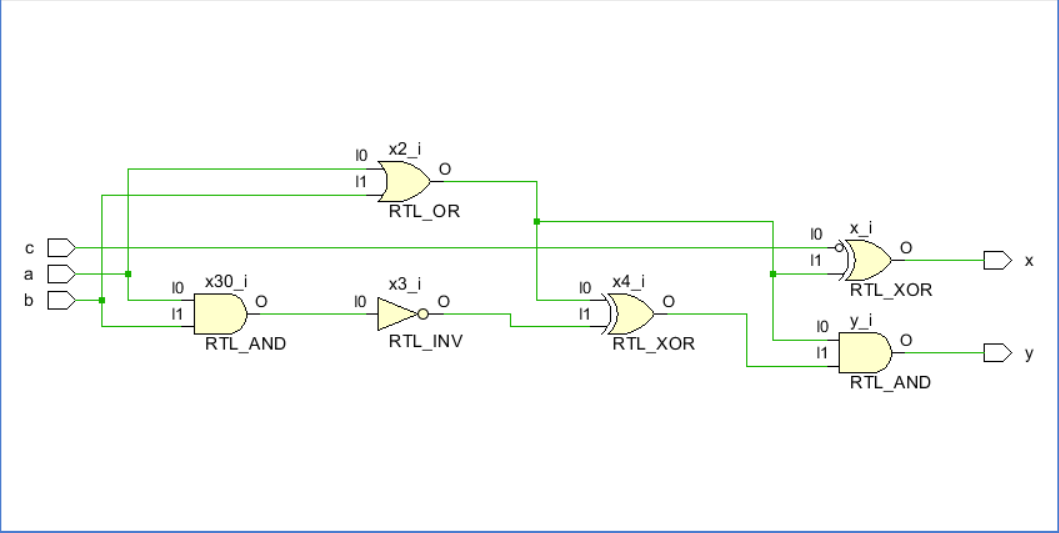
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| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

**LAB 2**

**Task 1:**

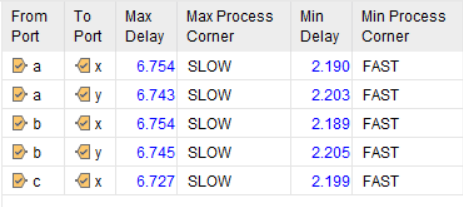
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| a | b | c | x | y |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Task 2:**

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The above circuit is the schematic from Vivado. For not gate Vivado didn’t used the gate diagram of the not gate however vivado represented that with the bubble which means not of the input.

**Task 3:**



The longest combinational delay was from path a to path x and path b to path x which is 6.754ns

**Task 4:**

A close-up of a list

Description automatically generated

**Task 4:**

module mycircuit (

    input logic a,

    input logic b,

    input logic c,

    output logic x,

    output logic y

);

// Local vars

logic x1,x2,x3,x4;

// Circuit Description

assign x1 = ~c;

assign x2 = a|b;

assign x3 = ~(a&b);

assign x4 = x2^x3;

// output vars

assign x = x1^x2;

assign y = x2&x4;

endmodule