|  |  |
| --- | --- |
| Name: Muhammad Ali Ahmad | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-029 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual # 3**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

**Task 1:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| a | b | c | x | y |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The Questa simulation satisfies the above truth table.

Task 2:

Corrected Code :

module full\_adder(

input logic a,

input logic b,

input logic c,

output logic sum,

output logic carry

);

assign sum = (a ^ b) ^ c;

assign carry = (a & b) | (c&(a ^ b));

endmodule

Test Bench

module full\_adder\_tb();

 logic a1;

 logic b1;

 logic c1;

 logic sum1;

 logic carry1;

 full\_adder foo(

 .a(a1),

 .b(b1),

 .c(c1),

 .sum(sum1),

 .carry(carry1)

 );

initial

begin

a1 = 0; b1 = 0; c1 = 0;

#10;

a1 = 0; b1 = 0; c1 = 1;

#10;

a1 = 0; b1 = 1; c1 = 0;

#10;

a1 = 0; b1 = 1; c1 = 1;

#10;

a1 = 1; b1 = 0; c1 = 0;

#10;

a1 = 1; b1 = 0; c1 = 1;

#10;

a1 = 1; b1 = 1; c1 = 0;

#10

a1 = 1; b1 = 1; c1 = 1;

#10;

$stop;

end

initial

begin

$monitor("sum=%b,carry=%b, a=%b, b=%b, c=%b", sum1,carry1,a1,b1,c1);

end

endmodule