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| Name:Muhammad Ali Ahmad | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-029 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

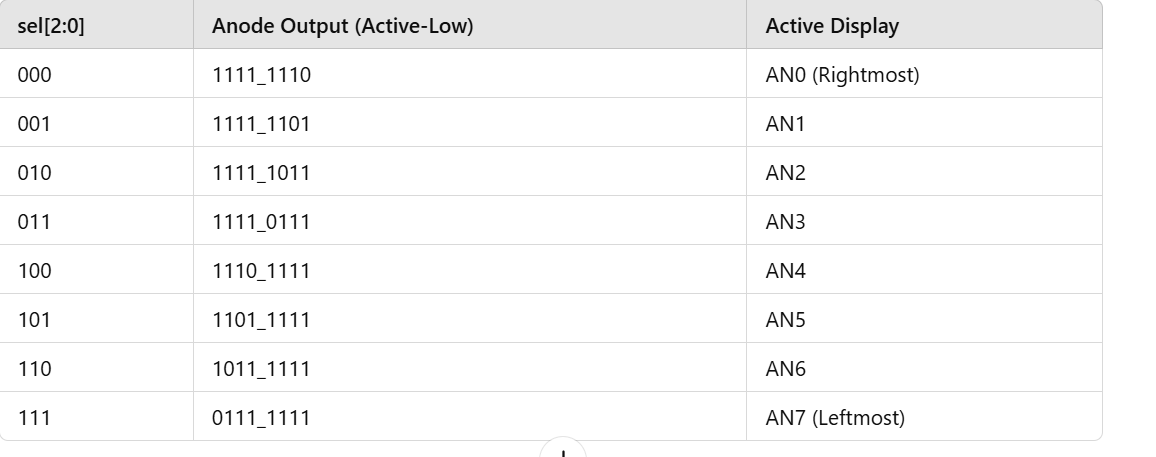
**Lab Manual 5**

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| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

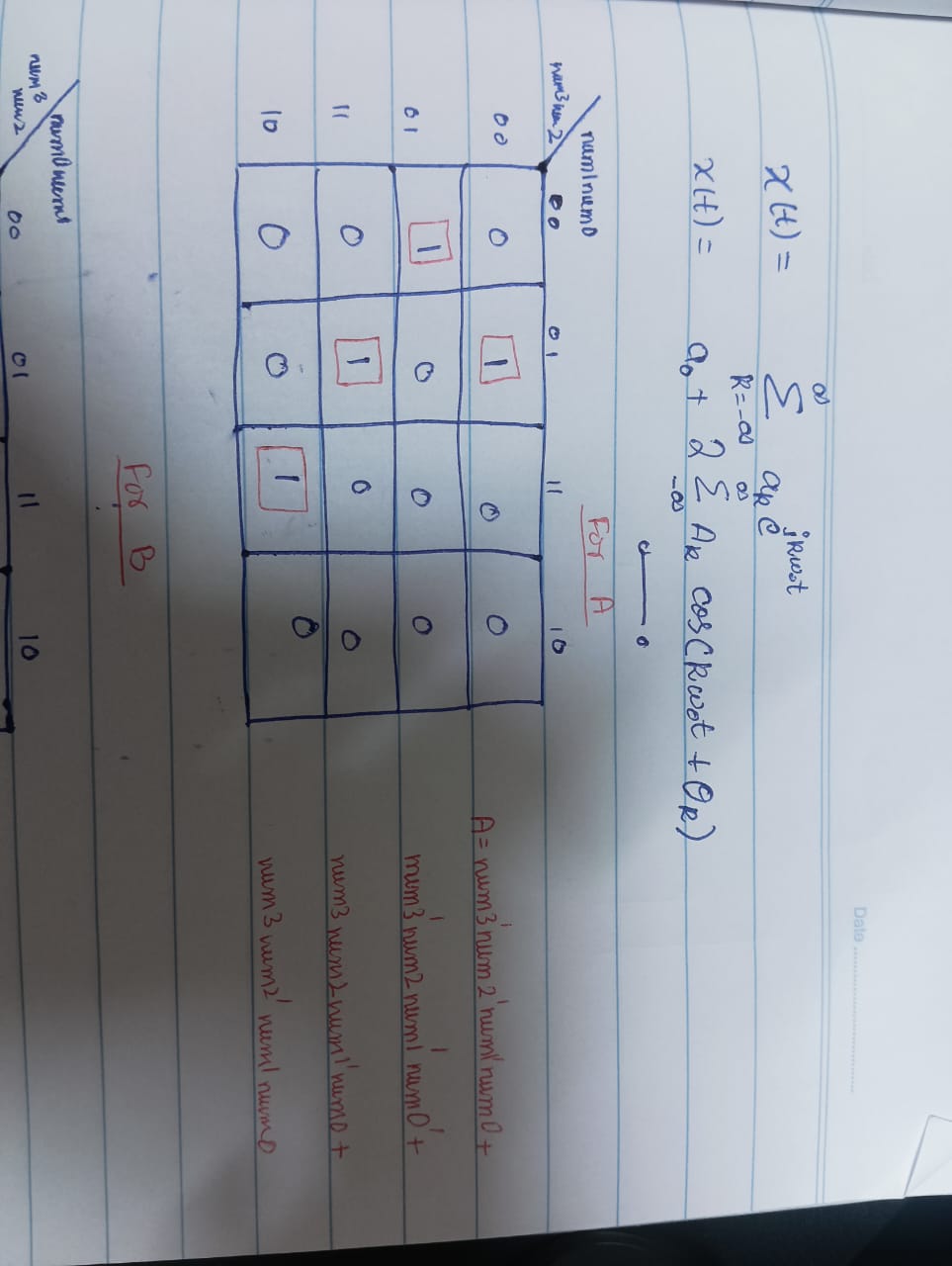
**Part 1)Truth table for cathode**

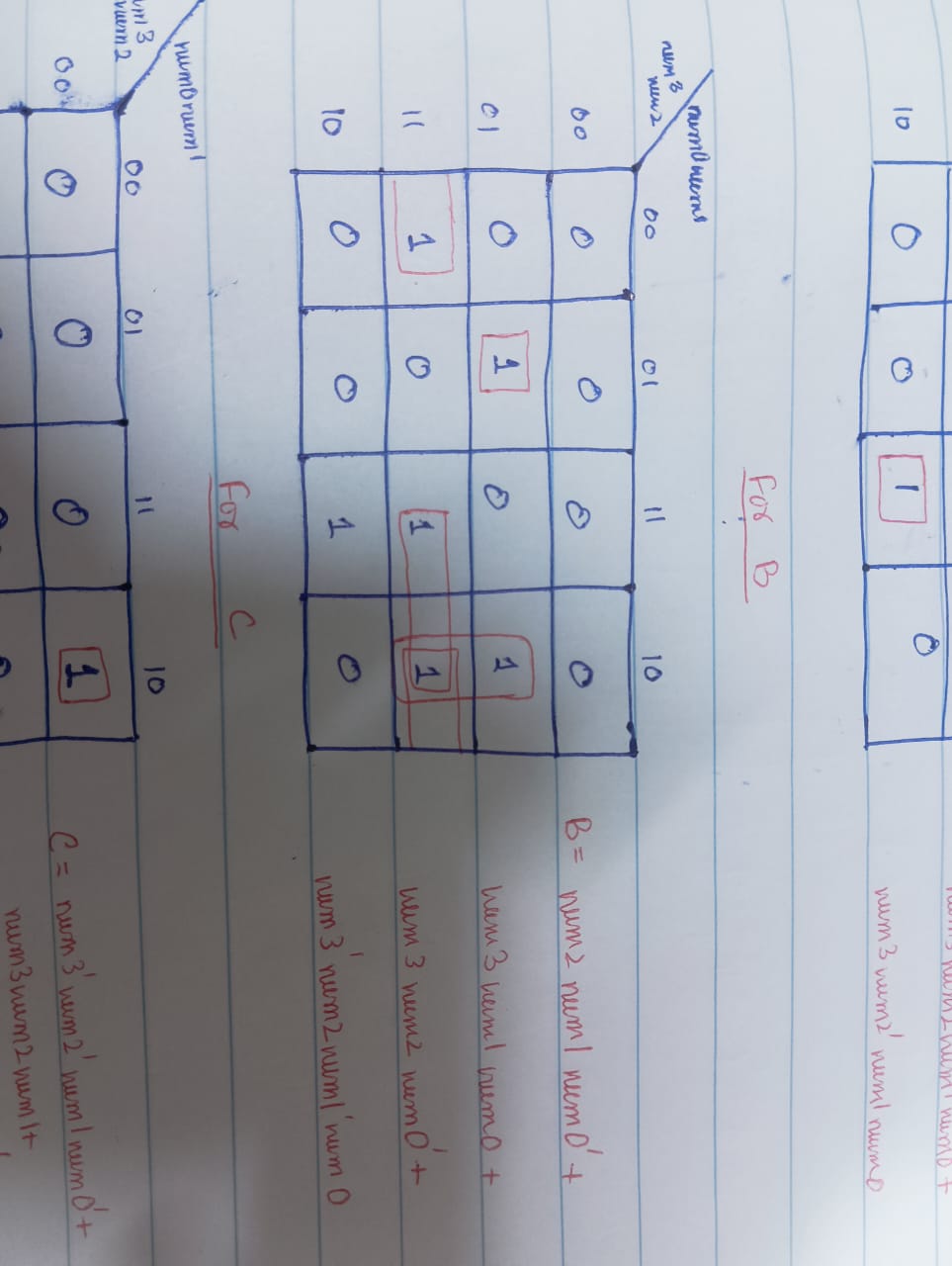
| **Hex** | **Binary (num[3:0])** | **A** | **B** | **C** | **D** | **E** | **F** | **G** | **Display** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **0** |
| 1 | 0001 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | **1** |
| 2 | 0010 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | **2** |
| 3 | 0011 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | **3** |
| 4 | 0100 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | **4** |
| 5 | 0101 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | **5** |
| 6 | 0110 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **6** |
| 7 | 0111 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | **7** |
| 8 | 1000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **8** |
| 9 | 1001 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | **9** |
| A | 1010 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | **A** |
| B | 1011 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **B** |
| C | 1100 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | **C** |
| D | 1101 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | **D** |
| E | 1110 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | **E** |
| F | 1111 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | **F** |

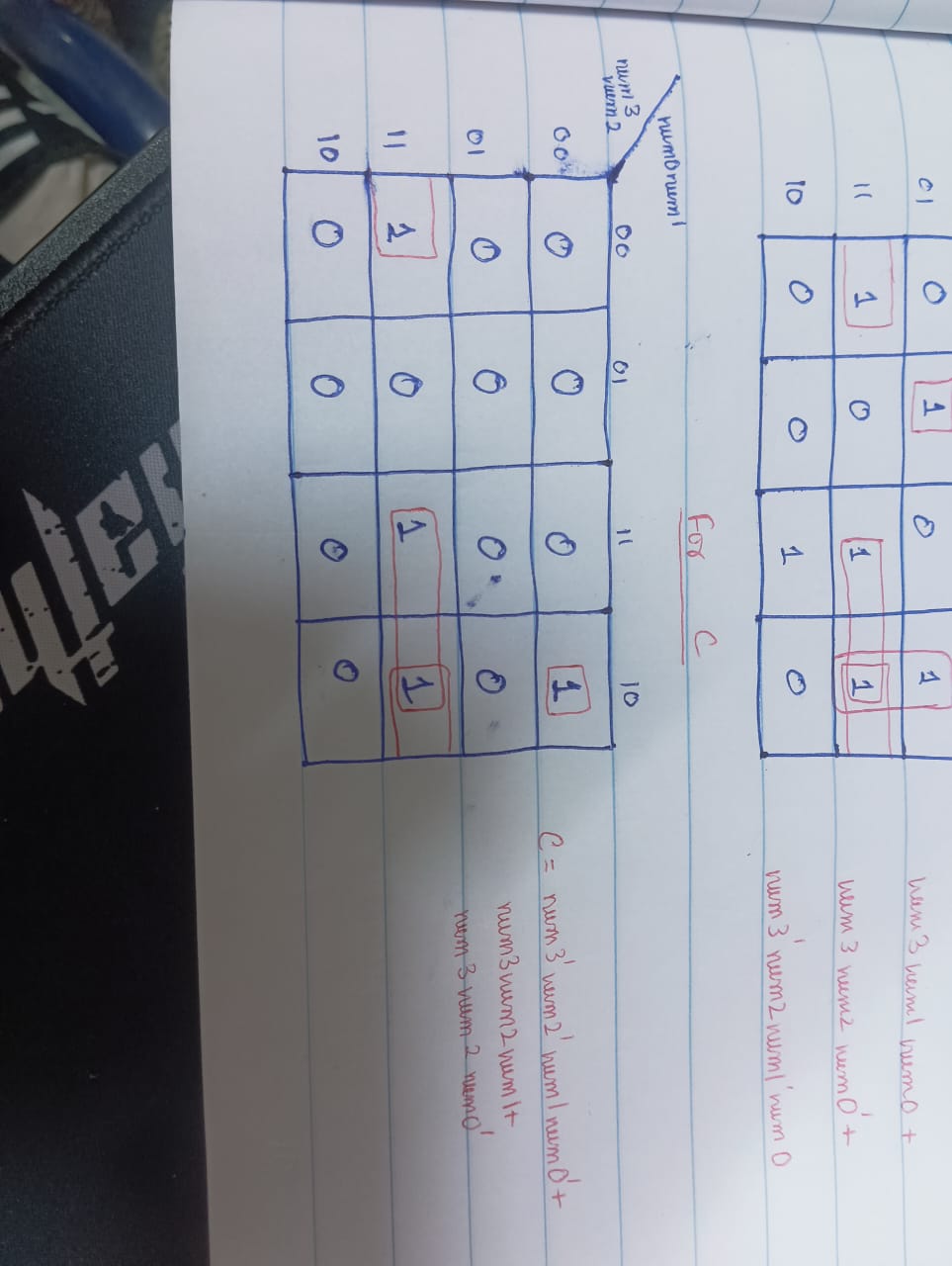
**Truth table for anode**

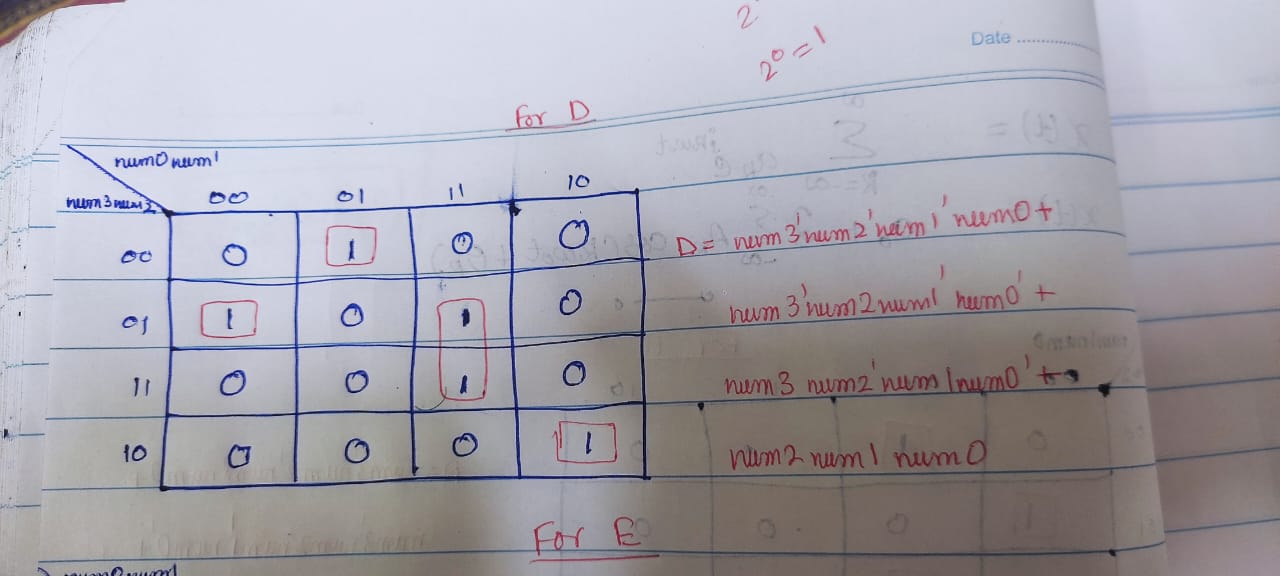
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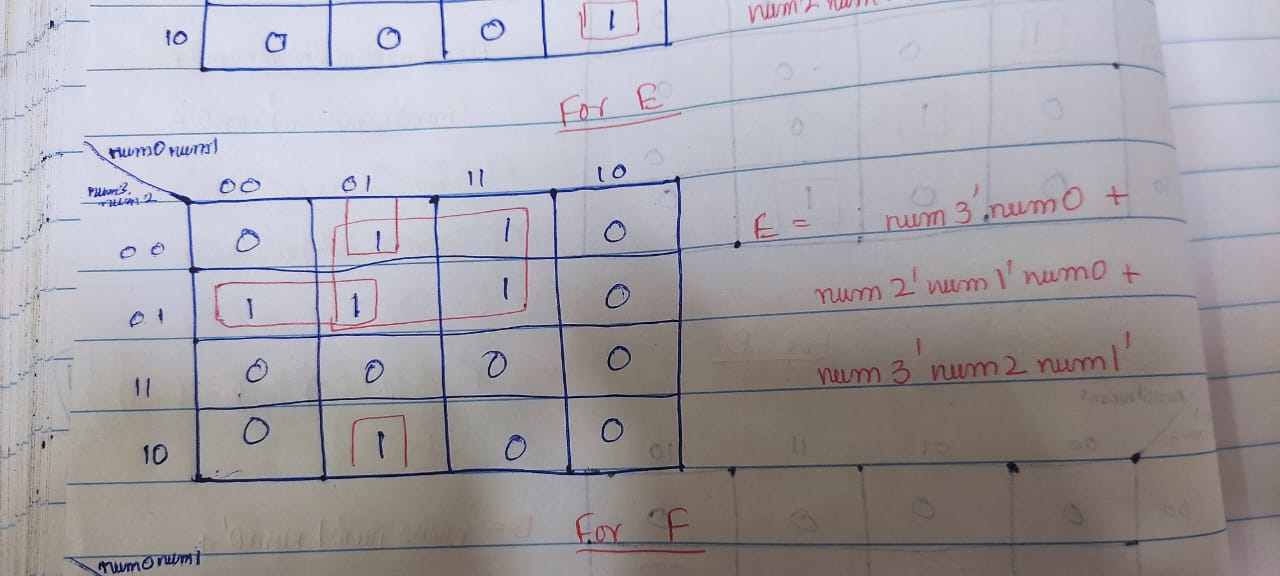
**Part 2) k maps**

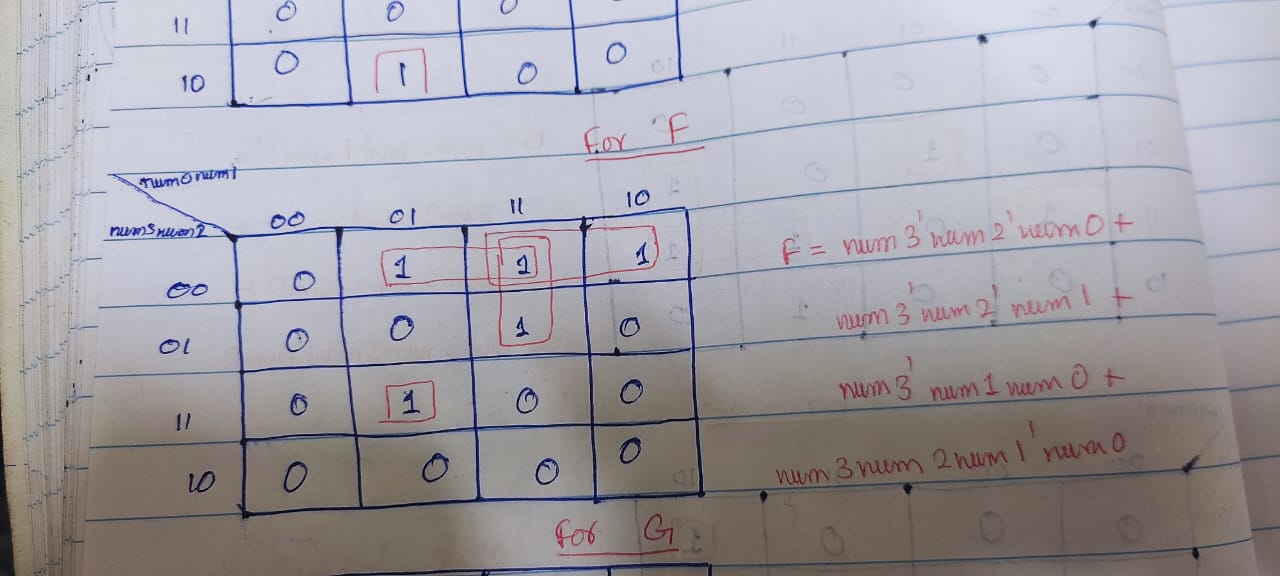
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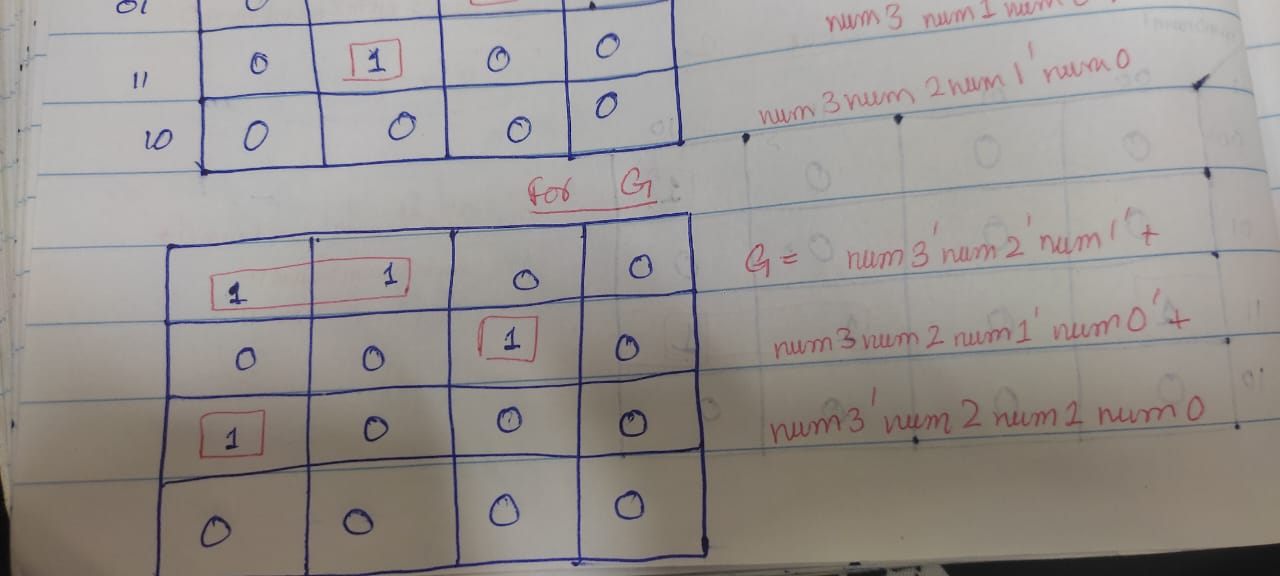
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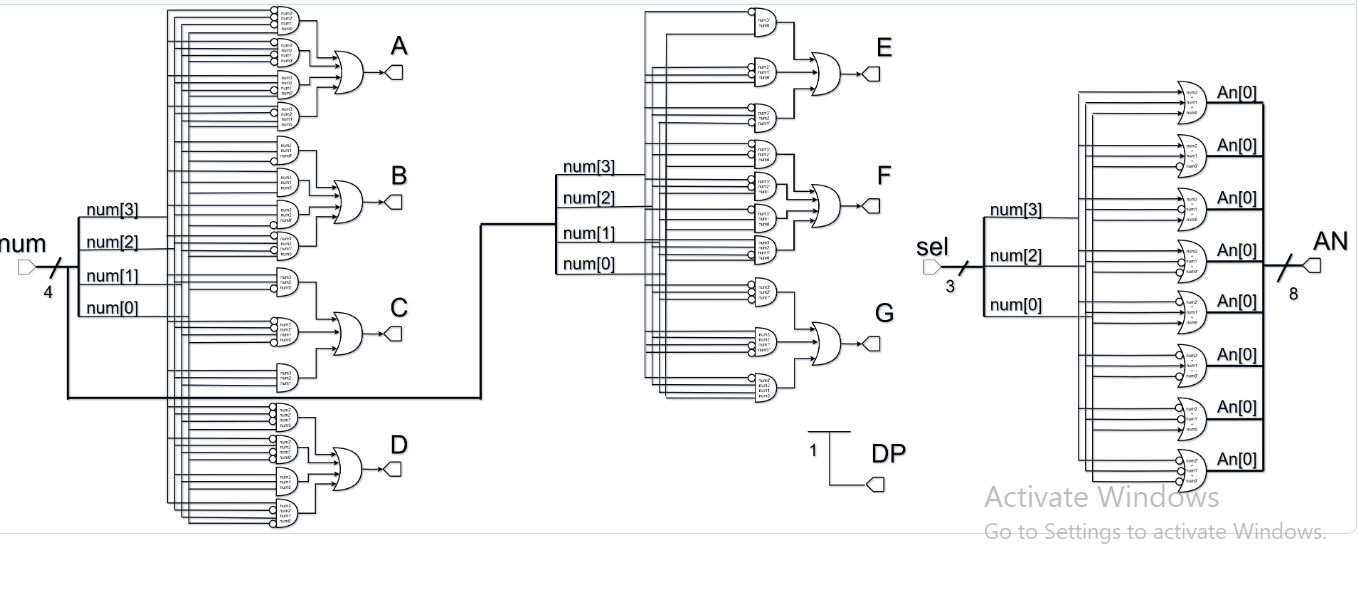
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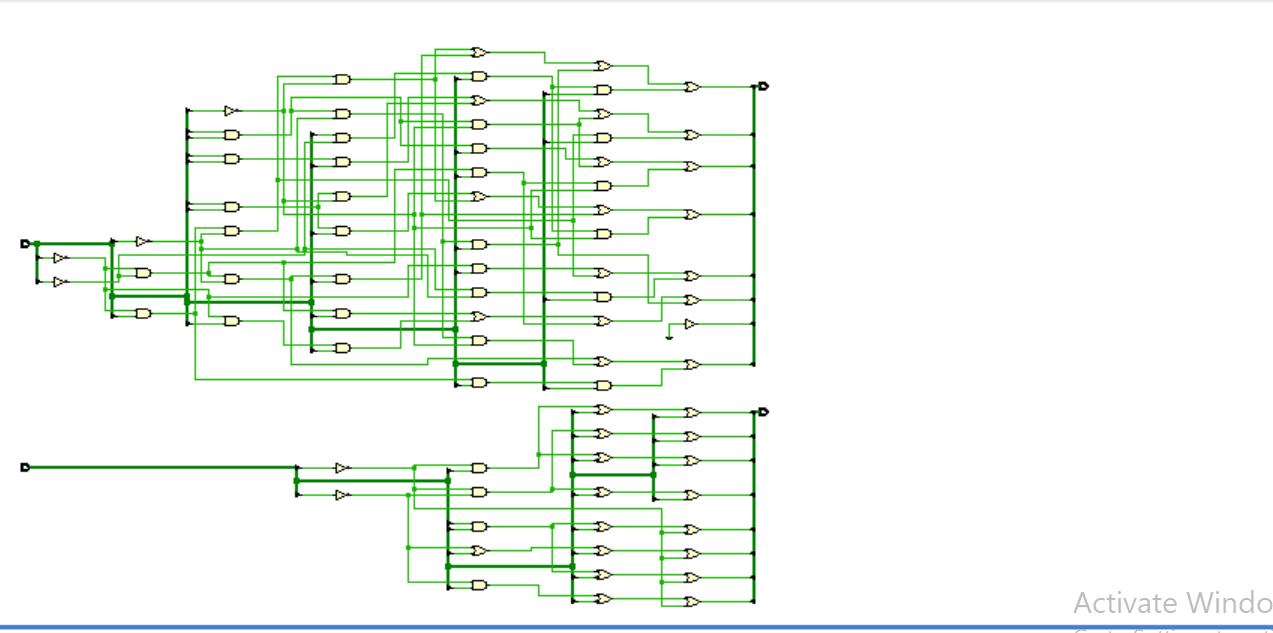
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***Circuit diagram inferred by k maps***

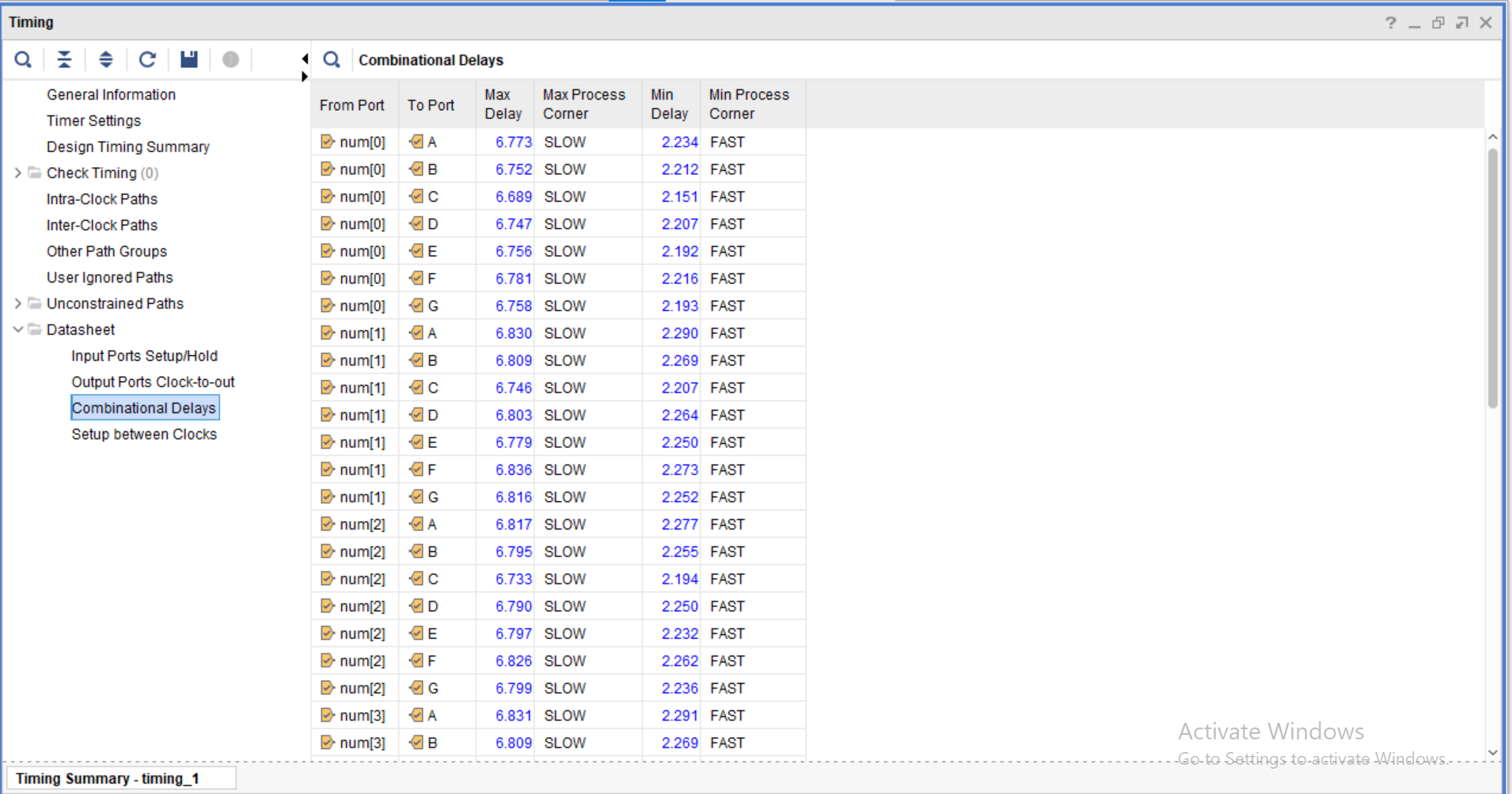
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***Circuit diagram from vivado***

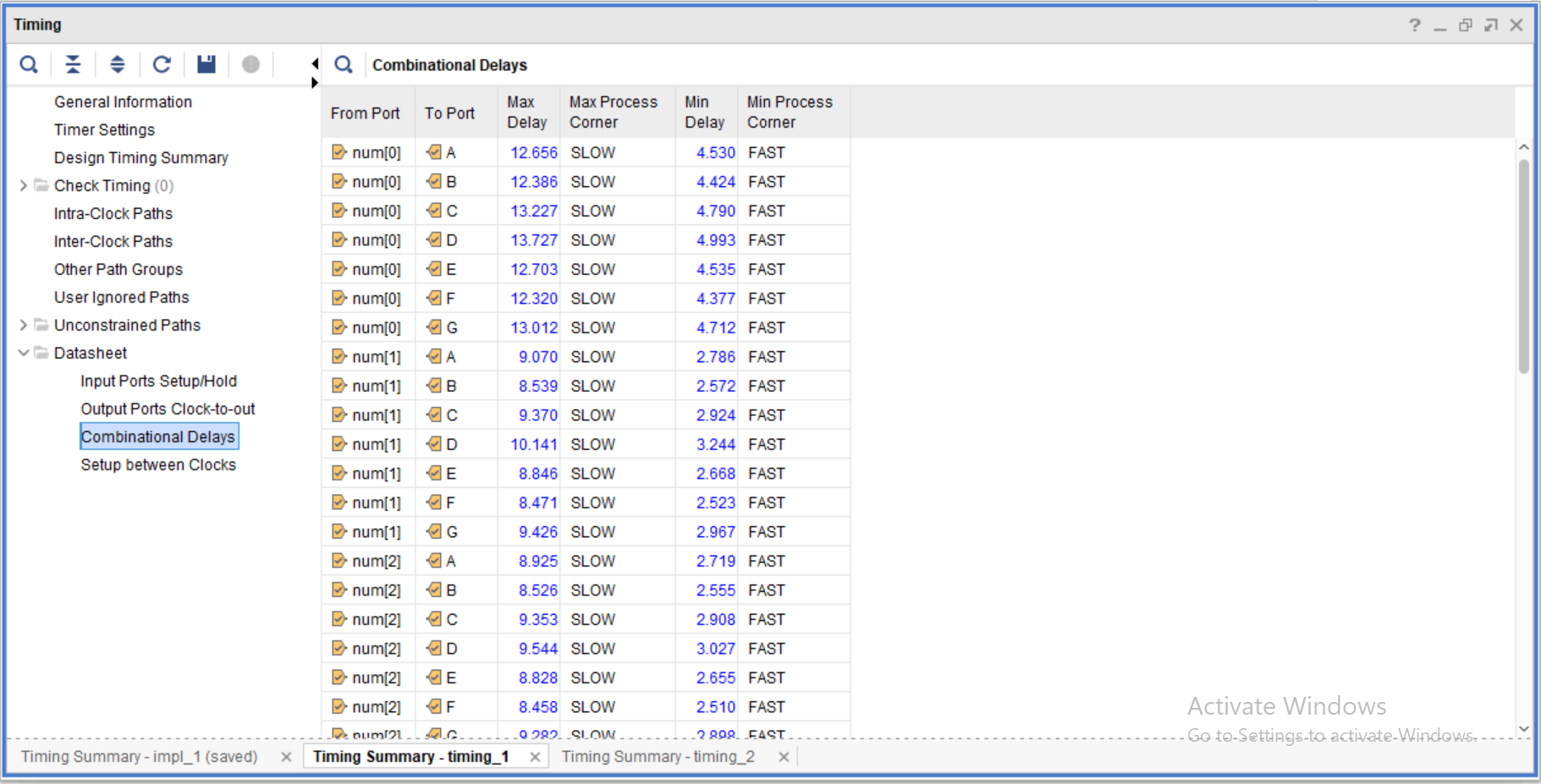
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***Combinational delays***

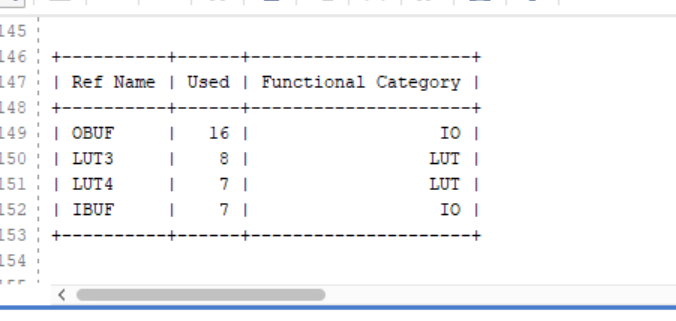
From num[3] to port a is the largest synthesis delay

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From num[0] to port D

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***Primitives***

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