Computer Architecture

Some questions & answers

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Q44

- In the following MIPS code.

```
lw  $t0,    32($s3)
add    $t0,    $s2,    $t0
sw $t0,    48($s3)
```

a. How many times is instruction memory accessed?

b. How many times is data memory accessed?

c. How many times is register file accessed?

d. Which ones are read from the register file, which ones are write to the register file?

A44

a. 3

b. 2

c. 7

d.

lw $t0, 32($s3) ☐ s0 is read from,
t0 is written into

add $t0, $s2, $t0 ☐ s2 and t0 are read from,
t0 is written into

sw $t0, 48($s3) ☐ s3 and t0 are read from

Q45

- Suppose a system has a virtual memory size of 64K and the system uses word addressing.

- If the page size is 1024 Word,

  a. How many bits this virtual memory address requires?

  b. Determine the number of virtual pages.

A45

- Virtual address space:
  - $64K = 2^6 \times 2^{10} = 2^{16}$ Word
- Page size:
  - $1024 \text{ Word} = 2^{10}$ Word

a. Because the virtual memory size is 2^{16} Word, the virtual memory address requires:
  - **16 bits**

b. Number of virtual pages:
  - $2^{16} / 2^{10} = 2^{16-10} = 2^6 =$ **64**

Q46

- Assume that you have a computer with a maximum main memory size of 2 GByte
  - (motherboard does not allow to upgrade the main memory).
- The program you want to run on this computer may require a larger main memory, resulting in a virtual memory that uses part of the hard drive.
  - However, you realized that the magnetic hard drive in this computer is too slow for your application.
- What can you do to increase the performance of this computer?
  - Explain how and why your solution will increase the performance.

A46

- I would replace magnetic hard drive with a Solid State Drive (SSD).

- SSDs have the following advantages over HDDs:
  - High-performance input/output operations per second (IOPS),
  - Less susceptible to physical shock and vibration
  - Longer lifespan
  - Lower power consumption
  - Lower access times and latency rates
  - Silent operation

Q47

- Consider a processor which uses branch delay technique for optimization of pipelining.

```
100   LOAD   R1, (500)
101   JUMP   105
102   ADD    R1, 1
103   AND    R1, (501)
```

- Each intruction has 2 or 3 stages depending on the instruction type
  - I: Instruction fetch, E: Execute
    D: Memory operation

a. Which instruction will be executed first after the processor encounters the instruction in line 101.

Q47

b. Complete the following pipelinening diagram for the given program.

- I: Instruction fetch, E: Execute
- D: Memory operation

```
100  LOAD   R1, (500)
101  JUMP   105
102  ADD    R1, 1
103  AND    R1, (501)
```

	1	2	3	4	5	6
100 LOAD R1, (500)	I	E	D			
101 JUMP 105		I	E			
102 ADD R1, 1			I	E		
103 AND R1, (501)				I	E	D

A47

a. First, instruction in line 100, which adds contents of memory location 500 to R1 will be executed.

- In line 101 there is a jump (unconditional branch) instruction.
- Because the processor uses a branch delay technique, instruction in line 102 will be executed before processor jumps to line 105.

b.

	1	2	3	4	5	6
100 LOAD R1, (500)	I	E	D			
101 JUMP 105		I	E			
102 ADDR1, 1			I	E		
103 ANDR1, (501)				I	E	D