Computer Architecture

Some questions & answers

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Q34

- What is an instruction and instruction set? Explain.

A34

- Instruction:
  - Language of the machine

- Instruction set:
  - Vocabulary of the language (collection of instructions that are understood by a CPU)

Q35

- Consider a stack-based processor with instructions

  PUSH, POP, ADD, SUB , MUL, and DIV.

- Write a program to compute

  $X = (A + B^2)/(D^2 – E)$

A35

- $X = (A + B^2)/(D^2 - E)$

```
PUSH A
PUSH B
PUSH B
MUL
ADD
PUSH D
PUSH D
MUL
PUSH E
SUB
DIV
POP X
```

Q36

A one-address type processor has an 8 bit accumulator (A), and a bytewise memory addressing. Data in memory locations 50 and 60 are 7A and 55 respectively, and they are in twos complement format. The following code is a part of an assembler program. If the code is executed;

```
I0      LDA (50)
I1      ADD (60)
I2      BRN I7
I3      LDA (51)
………………
………………
I7      STA (70)
I8      JMP I3
```

a. What will be the value of overflow flag after the execution of instruction I1? Explain

b. What will be the value of carry flag after the execution of instruction I1? Explain

c. Which line will be executed after the execution of instruction I2? Explain

d. What will be the content of program counter (PC)after the execution of I8.

LDA (X) : Load contents of memory location X to accumulator,
ADD (X) : Add contents of memory location X to accumulator,
BRN X : Branch to line X if negative,
STA : Store contents of accumulator to memory location X,
JMP X : Unconditional jump to line X

A36

a. Overflow flag is 1.

- Both 7A and 55 are positive. But the result is negative:

$$\begin{array}{l} \text{7A}\ (01111010) \\ \quad \underline{+55\ (01010101)} \\ \text{CF}\ (11001111) \end{array}$$

b. Carry flag will be 0, as there is no carry.

c. Because the sign flag is 1 (the result is negative), instruction I7 will be executed after the execution of the instruction I2

d. The program counter content will be I3

Q37

The contents of memory and CPU registers of a computer system is given as following (the values are in **hexadecimal**).

	Memory		CPU registers	
100	1240		101	PC
101	5241		0003	AC
102	2241		5241	IR
	.			
240	0003			
241	0343			
	.			
342	0003			
343	0302			

What will be the actual operand of the instruction for the;

- immediate addressing
- direct addressing
- indirect addressing
- PC relative addressing

A37

a. 0241

b. 0343

c. 0302

d. 0003

Q38

- Assume a stack-based processor that includes the stack operations PUSH and POP. Arithmetic operations automatically involve the top one or two stack elements. Begin with an empty stack. What stack elements remain after the following instructions are executed?

```
PUSH 4
PUSH 7
PUSH 8
ADD
PUSH 10
SUB
MUL
```

A38

Instruction	Stack (top on the left)
PUSH 4	4
PUSH 7	7, 4
PUSH 8	8, 7, 4
ADD	(8+7=15), 4
PUSH 10	10, 15, 4
SUB	(15-10=5), 4
MUL	(5×4=20)

Q39

- Compare zero-, one-, two-, and three-address machines by writing programs to compute

$$X = (A + B \times C)/(D - E \times F)$$

for each of the four machines (0 Address, 1 Address, 2 Address, 3 Address machines).

The instructions available for use are as follows:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOV (X □ Y)	MOV (X □ Y)
POP M	STORE M	ADD (X □ X + Y)	ADD (X □ Y + Z)
ADD	ADD M	SUB (X □ X - Y)	SUB (X □ Y - Z)
SUB	SUB M	MUL (X □ X × Y)	MUL (X □ Y × Z)
MUL	MUL M	DIV (X □ X / Y)	DIV (X □ Y / Z)
DIV	DIV M		

A39

$$X = (A + B \times C)/(D - E \times F)$$

0 Address

(Stack Machines)

```
PUSH A
PUSH B
PUSH C
MUL
ADD
PUSH D
PUSH E
PUSH F
MUL
SUB
DIV
POP X
```

1 Address

(Accumulator
Machine)

```
LOAD E
MUL F
STORE T
LOAD D
SUB T
STORE T
LOAD B
MUL C
ADD A
DIV T
STORE X
```

2 Address

(Memory-Memory, or
Register-register,
or Memory-register
Machine)

```
MOV R0, E
MUL R0, F
MOV R1, D
SUB R1, R0
MOV R0, B
MUL R0, C
ADD R0, A
DIV R0, R1
MOV X, R0
```

3 Address

Load-Store

```
MUL R0, E, F
SUB R0, D, R0
MUL R1, B, C
ADD R1, A, R1
DIV X, R0, R1
```

Q40

- Assume a pipeline with 4 stages:
  - fetch instruction (FI),
  - decode instruction and calculate addresses (DA),
  - fetch operand (FO), and
  - execute (EX).

- Draw the pipelinening diagram for a sequence of 7 instructions, in which the third instruction is a branch to instruction 15 that is taken and in which there are no dependencies.

A40...

	1	2	3	4	5	6	7	8	9	10
I1										
I2										
I3										
I4										
I5										
I6										
I15										

...A40

	1	2	3	4	5	6	7	8	9	10
I1	FI	DA	FO	EX						
I2		FI	DA	FO	EX					
I3			FI	DA	FO	EX				
I4				FI	DA	FO				
I5					FI	DA				
I6						FI				
I15							FI	DA	FO	EX

Q41

- A pipelined processor has a clock rate of 2.5 GHz and executes a program with 1.5 million instructions.
  - The pipeline has five stages, and instructions are issued at a rate of one per clock cycle.
  - Ignore penalties due to branch instructions and out-of-sequence executions.

What is the speedup of this processor for this program compared to a nonpipelined processor?

A41

We can ignore the initial filling up of the pipeline and the final emptying of the pipeline, because this involves only a few instructions out of 1.5 million instructions.

Therefore the speedup is a factor of five.

Q42

- Provide a typical list of the inputs and outputs of a control unit.

A42

- **Inputs** :
  - **Clock:**
    - This is how the control unit “keeps time.” The control unit causes one micro-operation (or a set of simultaneous micro-operations) to be performed for each clock pulse. This is sometimes referred to as the processor cycle time, or the clock cycle time.
  - **Instruction register:**
    - The opcode of the current instruction is used to determine which micro-operations to perform during the execute cycle.
  - **Flags:**
    - These are needed by the control unit to determine the status of the processor and the outcome of previous ALU operations.
  - **Control signals from control bus:**
    - The control bus portion of the system bus provides signals to the control unit, such as interrupt signals and acknowledgments. The
- **Outputs** :
  - **Control signals within the processor:**
    - These are two types: those that cause data to be moved from one register to another, and those that activate specific ALU functions.
  - **Control signals to control bus:**
    - These are also of two types: control signals to memory, and control signals to the I/O modules.

Q43

- Your ALU can add its two input registers, and it can logically complement the bits of either input register, but it cannot subtract.
- Numbers are to be stored in two’s complement representation.

- List the micro-operations your control unit must perform to cause a subtraction.

A43

- Consider the instruction SUB R1, X, which subtracts the contents of location X from the contents of register R1, and places the result in R1.

- t1: MAR □ (IR(address))
- t2: MBR □ Memory
- t3: MBR □ Complement(MBR)
- t4: MBR □ Increment(MBR)
- t5: R1 □ (R1) + (MBR)