Midterm (13.11.2018) (08:30-09:45)

COMP303 – Computer Architecture

Q1(17)	Q2(17)	Q3(17)	Q4(17)	Q5(17)	Q6(17)	Q7(17)	Q8(17)	Q9(17)	Q10(17)	Total

YOU MUST ANSWER 6 QUESTIONS ONLY

Q1. MIPS processor was born in the early 1980s from the work done by John Hennessy and his students at Stanford University and is mainly used in small devices. So,

a. What architecture the MIPS processor adapted? (07)
b. What are the advantages of this architecture? (10)

A1.

a. MIPS adapted the RISC architecture to explore the architectural concept of RISC
b. Advantages of RISC Architecture:
   - The performance of RISC processors is often two to four times than that of CISC processors because of simplified instruction set.
   - This architecture uses less chip space due to reduced instruction set.
   - The per-chip cost is reduced by this architecture that uses smaller chips consisting of more components on a single silicon wafer.
   - RISC processors can be designed more quickly than CISC processors due to its simple architecture.
   - The execution of instructions in RISC processors is high due to the use of many registers for holding and passing the instructions as compared to CISC processors.

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Q2. List the characteristics of the Von Neumann computer model. (17)

A2. The Von Neumann computer model has the following characteristics:

-Three hardware systems:

A central processing unit (CPU)

A main memory system

An I/O system

-The capacity to carry out sequential instruction processing.

-A single data path between the CPU and main memory.

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Q3. Write a simple VVM assembly program that if the entered number is 0, it keeps asking to enter a non-zero number, otherwise the number is stored in the location 10 and it stops. (17)

A3. The solution is as follows:

```
00      in              // input number
```

```
01      brz 00          // if 0 keep asking to reenter the number (go to 00)
02      sto 10          // else store in 10
06      hlt             // stop.  "cob" can also be used
```

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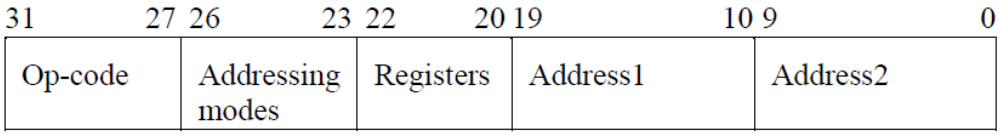
Q4. If a computer system, in which addressing is by 1 byte unit, has the following instruction format:



a. How many registers this computer system might have? (04)
b. How many bits are needed for the program counter? (04)
c. How many memory locations this instruction will occupy? (04)
d. Total how many bits can be stored in the memory of this computer? (05)

A4.

a. 2^3 = 8 registers,
b. 10 bits are needed
c. 32 / 8 = 4 memory locations
d. 2^{10} = 1024 Byte = 1024×8 = 8192 bit,

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Q5. Data from a damaged file containing variables in 32 bit IEEE floating point number format needs to be recovered. One of the recovered data appears to be $(432AA000)_{fp(hex)}$.

$(X_{10}=(-1)^S \times 1.M \times 2^{BE-127})$

a. What is the recovered data in decimal? (12)

b. Find corresponding BCD code of the recovered data. (05)

A5.

a. $(432AA000)_{fp(hex} = (01000011001010101010000000000000)_{fp(bin)}$

S = 0

BE = $(134)_{10} = (10000110)_2$ ➔ E = $(134-127)_{10} = (10000110 - 01111111)_2 = (00000111)_2$

M = 01010101010000000000000

$X_{10}=(-1)^S \times 1.M \times 2^{BE-127}) = (-1)^0 \times 1.\ 0101010101 \times 2^7 = 10101010.101 = (170.625)_{10}$

b. $(170.625)_{10}$ = (0001 0111 0000.0110 0010 0101)$_{BCD}$

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Q6. Consider the following assembly program written for a computer with a two-addres instruction processor. If a portion of the memory is given as beside (V, W, X, Y, and Z are variables);

```
100   MOVE   R1, (200)
101   SUB    R1, (201)
102   MOVE   R2, (202)
103   ADD    R2, (204)
104   MPY    R1, R2
105   MOVE   (204), R1
```

Mem. Adress	Data
200	V = A4
201	W = A0
202	X = 72
203	Y = 22
204	Z = 41

a. What function (in terms of the given variables) this program implements? (R1 and R2 are registers; MOVE: data movement instruction; SUB: subtraction instruction; MPY: multiplication instruction; ADD: addition instruction; DIV: division instruction) (08)

b. Assuming that V, W, X, Y, and Z are 2s complement signed numbers, what will be the values of *carry flag*, *sign flag*, *zero flag*, and *overflow flag* after the execution of instruction in memory location 103? Explain (09)

A6.

a. Z = (V - W) (X + Y)

b.

```
                1
72      ➔       0 1 1 1 0 0 1 0
41      ➔       0 1 0 0 0 0 0 1
B3      ➔       0 1 0 1 1 0 0 1 1
```

carry flag = 0 , sign flag = 1, zero flag = 0, overflow flag = 1

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Q7. In the following MIPS code

```
lw    $t0,   32($s3)
add   $t0,   $s2,   $t0
sw    $t0,   48($s3)
```

a. How many times is instruction memory accessed? (04)
b. How many times is data memory accessed? (04)
c. How many times is register file accessed? (04)
d. Which ones are read from the register file, which ones are write to the register file? (05)

A7.

a. 3
b. 2
c. 7
d.

```
lw    $t0, 32($s3)      ➔   s0 is read from, t0 is written into
add   $t0, $s2, $t0     ➔   s2 and  t0 are read from, t0 is written into
sw    $t0, 48($s3)      ➔   s3 and t0 are read from
```

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Q8. Given ***x* = 100** and ***y* = 110** in unsigned integer notation, compute the product ***p* = *x* × *y*** by using multiplication algorithm. (complete the following table) (17)

A8.

	C	A	Q	M	Process
	0	0 0 0	1 0 0	1 1 0	Initial
Step 1	0	0 0 0	0 1 0	1 1 0	Logic Shift Right
Step 2	0	0 0 0	0 0 1	1 1 0	Logic Shift Right
Step 3	0	1 1 0	0 0 1	1 1 0	A ← A + M
	0	0 1 1	0 0 0	1 1 0	Logic Shift Right

The following solution is also correct:

	C	A	Q	M	Process
	0	0 0 0	1 1 0	1 0 0	Initial
Step 1	0	0 0 0	0 1 1	1 0 0	Logic Shift Right
Step 2	0	1 0 0	0 1 1	1 0 0	A ← A + M
	0	0 1 0	0 0 1	1 0 0	Logic Shift Right
Step 3	0	1 1 0	0 0 1	1 0 0	A ← A + M
	0	0 1 1	0 0 0	1 0 0	Logic Shift Right

$p = x \times y = 100 \times 110 = (011000)_2 = (24)_{10}$

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Q9. The contents of memory and CPU registers of a computer system are given as following (the values are in hexadecimal). What will be the content of the actual operand for the instruction being executed when the addressing mode is;

a. immediate addressing (04)
b. direct addressing (04)
c. indirect addressing (04)
d. PC relative addressing (05)

Memory address	Memory content		Register Content	Register
1 0	5 6 1		10	PC
1 1	1 6 0			AC
1 2	3 6 1		5 6 1	IR
	.			
6 0	0 0 3			
6 1	0 7 0			
	.			
7 0	0 0 5			
7 1	0 0 2			

A9. a. 061 (operand is adress)

b. 070 (operand is the value in the address 61)

c. 005 (operand is the value in the address 70 pointed by the address 61)

d. 002 (operand is the value in the address calculated as 61+10 (content of PC))

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Q10. In an 8 bit microprocessor data transfer rate is given as 2 MByte per second. Find the clock frequency of the processor if a bus cycle takes 2 clock cycles. (17)

A10. If 2 MByte is transferred in 1 second, 1 Byte is transferred in $\mathbf{1/(2\times10^6) = 0.5\times10^{-6}}$ **second** .

If 1 byte requires 2 clock cycle to transfer, clock cycle is $\mathbf{(0.5\times10^{-6})/2 = 0.25\times10^{-6}}$ second.

So, the clock frequency is $\mathbf{1/(0.25\times10^6}$ **second) = 4 MHz**.