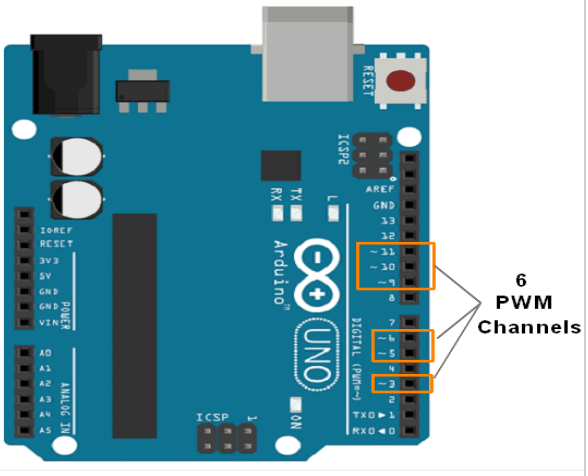
Timer Registers Summary for ATMEGA32P

Register	Description	Bits							
		7	6	5	4	3	2	1	0
TCCRnA	Timer/Counter Control Register A	COMnA1	COMnA0	COMnB1	COMnB0	-	-	WGM01	WGM00
TCCRnB	Timer/Counter Control Register B	FOCnA	FOCnB	-	-	WGM02	CS02	CS01	CS00
TCNTn	Timer/Counter Register	**TCNTn [7:0]**							
OCRnA	Output Compare Register A	OCRnA**[7:0]**							
OCRnB	Output Compare Register B	OCRnB[**7:0]**							

Timers in ATMEGA32p

Timer output	Arduino output	Pin name
OC0A	6	PD6
OC0B	5	PD5
OC1A	9	PB1
OC1B	10	PB2
OC2A	11	PB3
OC2B	3	PD3



The ATmega328P has three timers known as Timer 0, Timer 1, and Timer 2. Each timer has two output compare registers that control the PWM width for the timer's two outputs: when the timer reaches the compare register value, the corresponding output is toggled. The two outputs for each timer will normally have the same frequency, but can have different duty cycles (depending on the respective output compare register).

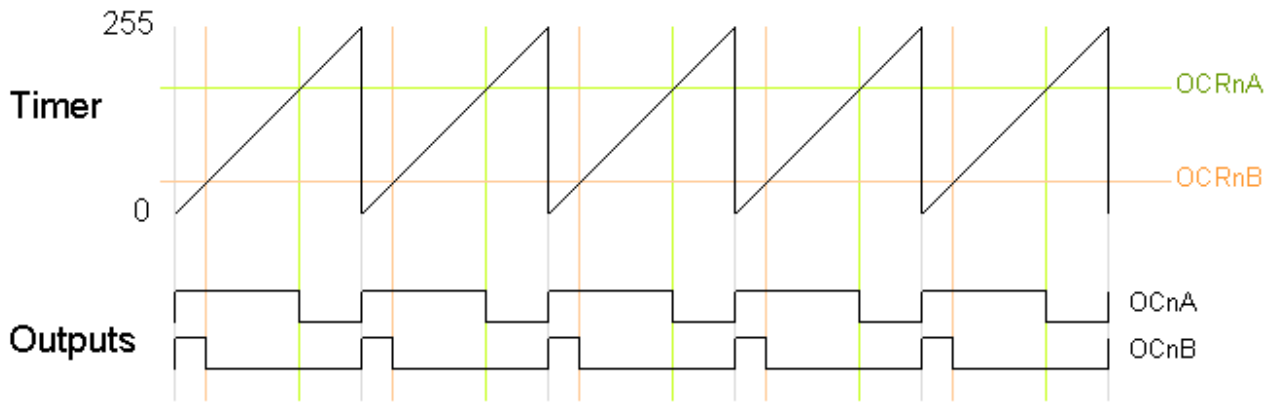
Each of the timers has a prescaler that generates the timer clock by dividing the system clock by a prescale factor such as 1, 8, 64, 256, or 1024. The Arduino has a system clock of 16MHz and the

timer clock frequency will be the system clock frequency divided by the prescale factor. Note that Timer 2 has a different set of prescale values from the other timers.

The timers are complicated by several different modes. The main PWM modes are "Fast PWM" and "Phase-correct PWM", which will be described below. The timer can either run from 0 to 255, or from 0 to a fixed value. (The 16-bit Timer 1 has additional modes to supports timer values up to 16 bits.) Each output can also be inverted.

Fast PWM (Timer Mode)

In the simplest PWM mode, the timer repeatedly counts from 0 to 255. The output turns on when the timer is at 0, and turns off when the timer matches the output compare register. The higher the value in the output compare register, the higher the duty cycle. This mode is known as Fast PWM Mode. The following diagram shows the outputs for two particular values of OCRnA and OCRnB. Note that both outputs have the same frequency, matching the frequency of a complete timer cycle.



Timer Registers

Several registers are used to control each timer. The Timer/Counter Control Registers TCCRnA and TCCRnB hold the main control bits for the timer. (Note that TCCRnA and TCCRnB do not correspond to the outputs A and B.) These registers hold several groups of bits:

- Waveform Generation Mode bits (WGM): these control the overall mode of the timer. (These bits are split between TCCRnA and TCCRnB.)
- Clock Select bits (CS): these control the clock prescaler
- Compare Match Output A Mode bits (COMnA): these enable/disable/invert output A
- Compare Match Output B Mode bits (COMnB): these enable/disable/invert output B

The Output Compare Registers OCRnA and OCRnB set the levels at which outputs A and B will be affected. When the timer value matches the register value, the corresponding output will be modified as specified by the mode.

The bits are slightly different for each timer, so consult the datasheet for details. Timer 1 is a 16-bit timer and has additional modes. Timer 2 has different prescaler values.

Register Configurations for Fast PWM (Timer Mode)

1. Waveform Generation Mode bits (WGM)

these control the overall mode of the timer.

- The WGM02 bit is located in the TCCRnB register
- The WGM01 and WGM00 bits are located in the TCCRnA register

Mode	WGM02	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCRx at
0	0	0	0	Normal	0xFF	Immediate
1	0	0	1	PWM, phase correct	0xFF	TOP
2	0	1	0	CTC	OCRA	Immediate
3	0	1	1	Fast PWM	0xFF	BOTTOM
4	1	0	0	Reserved	–	–
5	1	0	1	PWM, phase correct	OCRA	TOP
6	1	1	0	Reserved	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM

Notes: 1. MAX = 0xFF
2. BOTTOM = 0x00

The difference between the mode 3 Fast PWM and mode 7 Fast PWM is the TOP value. For mode 3 the TOP value is is 0xFF whereas the the TOP value for mode 7 is OCRA. If mode 7 is used then we have to load count value into the OCR0A register. If mode 3 is used then we don't have to load the counter since the TOP value in this case is 0xFF. Thus in Fast PWM mode, we have to select either mode 3 or 7. Once selected the counter is started and the timer/counter starts counting from zero to TOP value and when TOP value is reached the counting is repeated from the bottom.

2. Clock Select bits (CS):

these control the clock prescaler

The Fast PWM frequency can be calculated by the following equation:

$$F_{PWM} = \frac{F_{osc}}{256\ N}$$

where, F_{PWM} is the frequency of the generated PWM wave, F_{osc} is the CPU frequency, N is the pre-scalar which can have value of 1, 8, 64, 256 and 1024.

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/(no prescaling)
0	1	0	$clk_{I/O}$/8 (from prescaler)
0	1	1	$clk_{I/O}$/64 (from prescaler)
1	0	0	$clk_{I/O}$/256 (from prescaler)
1	0	1	$clk_{I/O}$/1024 (from prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

3. The Output Compare Registers OCRnA and OCRnB

These registers are set the levels at which outputs A and B will be affected. When the timer value matches the register value, the corresponding output will be modified as specified by the mode.

They are used to implement the required duty cycle. The duty cycle of the Fast PWM signal is calculated using the following formula.

$$OCRnA = \frac{256\ D}{100} - 1$$

where, D is the Duty cycle that range from 0% to 100%.

4. Compare Match Output A Mode bits (COMnA)

these enable/disable/invert output A

COM0A1	COM0A0	Description
0	0	Normal port operation, OC0A disconnected.
0	1	WGM02 = 0: Normal port operation, OC0A disconnected. WGM02 = 1: Toggle OC0A on compare match.
1	0	Clear OC0A on compare match, set OC0A at BOTTOM, (non-inverting mode).
1	1	Set OC0A on compare match, clear OC0A at BOTTOM, (inverting mode).

5. Compare Match Output B Mode bits (COMnB)

these enable/disable/invert output B, can be configured in the same manner as timer nA

COM0B1	COM0B0	Description
0	0	Normal port operation, OC0B disconnected.
0	1	Reserved
1	0	Clear OC0B on compare match, set OC0B at BOTTOM, (non-inverting mode)
1	1	Set OC0B on compare match, clear OC0B at BOTTOM, (inverting mode).