A

SAVITRIBAI PHULE PUNE UNIVERSITY

Seat No S1910208522
Stk. No 5411488
Sub. LDCO
Centre 4102

214442-LDCO

Sem:3 7021929

...ination	Entrance Oct / Nov 2024
...Date	30/11/24 Friday
...ct	LDCO
...No.	63521-60 Sec -
...dium ...nswer	English
...t No. : In figure & In words	1 0 2 0 8 5 2 2
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Instruction to Candidate

1. Candidate has to confirm seat number, subject and centre number printed on Bar code and write it on attendance sheet.
   विद्यार्थ्याने प्रथम बार कोडवरील आसन क्रमांक, विषय व केंद्र क्रमांक तपासून घेण्य असल्याची खात्री करावी आणि उपस्थिती पत्रकावर नोंदवावी.
2. Paste Bar Code in prescribed space.
   उत्तरपत्रिकेवरील विहित जागेतच बार कोड लावावा.
3. Do not write anything on Bar code sticker, otherwise it will be treated as unfairmeans.
   बार कोड स्टिकरवर काहीही लिहू नये, अन्यथा परीक्षा गैरप्रकार समजला जाईल.

Q. No.	Examiner	Moderator
1	— —	
2	0 7	
3	— —	
4	0 7	
5	— 1	
6	— -	
7	— —	
8	0 2	
9		
10		
11		
12		
Total in Figure	1 7	
Total in Words	Seventeen	
Signature	VE	

Specific remarks regarding malpractice (in Red Ink)

Total	Marks in Figure	Marks in Words	Sign
Examiner	17	Seventeen	VE
Moderator			

१. विद्यार्थ्याने उत्तरपत्रिकेच्या मुखपृष्ठावर तसेच उपस्थिती पत्रकावर विहित जागेत आसन क्रमांक अंकात व अक्षरात बिनचूक लिहून स्वाक्षरी करावी.

Candidate shall fill all information about seat number, paper etc. in prescribed space and sign on the answer book and attendance sheet.

२. उत्तरपत्रिकेवर फक्त निळ्या अथवा काळ्या शाईचा उपयोग करावा, अन्यथा उत्तरपत्रिकेचे मूल्यमापन केले जाणार नाही.

Candidate shall use blue or black ink only. Otherwise answer book will not be evaluated.

३. उत्तरपत्रिकेच्या पृष्ठक्रमांक ३ पासून लिहिण्यास प्रारंभ करावा.

Candidate shall start writing answer from page no. 3 of the answer book.

४. संबंधित प्रश्नाचे अथवा उपप्रश्नाचे उत्तर जेथून सुरू होते तेथेच समासात प्रश्न क्रमांक, उपप्रश्न क्रमांक अचूक व स्पष्ट लिहावा, यासाठी वेगळ्या शाईचा उपयोग करू नये.

Candidate shall mention question number, sub question number correctly at the beginning of the same and shall not use ink other than blue or black.

५. प्रत्येक पानाच्या दोन्ही बाजूस लिहावे, उत्तरपत्रिका किंवा पुरवणी उत्तरपत्रिकेचे कोणतेही पान फाडू नये, फाडल्यास परीक्षा गैरप्रकार समजून पुढील कार्यवाही करण्यात येईल.

Candidate shall write on both sides of pages and shall not tear off any page, it will be treated as unfairmeans.

६. पेपर संपण्यापूर्वी १० मिनिटे अगोदर इशारा घंटा होईल, त्यानंतर विद्यार्थ्याने उत्तरपत्रिका व पुरवणी उत्तरपत्रिकेवर होलोक्राफ्ट स्टिकर विहित जागेवरच लावावा.

Warning bell will be given before 10 minutes of the concluding time. Candidate shall paste Holocraft Sticker at appropriate space on the answer book.

७. कॉपी करणे किंवा दुसऱ्याच्या नावावर परीक्षेस बसणे यांसारख्या कृती 'महाराष्ट्र-प्रीव्हेन्शन ऑफ मालप्रॅक्टिस ॲक्ट युनिव्हर्सिटी, बोर्ड ॲण्ड अदर स्पेसिफाईड एक्झामिनेशन्स ॲक्ट, १९८२' (सा.फु.पु.वि. चा अध्यादेश क्रमांक ९) त्यानुसार संमत केलेला कायदा या अन्वये दंडही असेल.

An Act of Copying or Impersonations at an Examination is Punishable under 'The Maharashtra Prevention of Malpractices at University, Board and Other Specified Examinations Act, 1982' (Ordinance 9 of SPPU). The Act passed to the effect.

Examiner and Moderator has to write marks on all given appropriate place only. Examiner should give assessment tick(✓) or (×) in the margin.

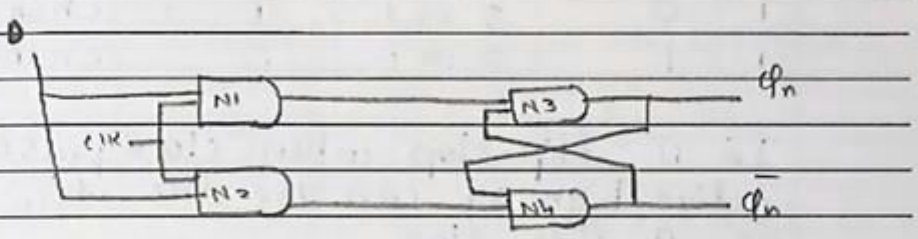
Q. No.	Examiner	Moderator	Verification	Revaluation
1	—			
2	7			
3	—			
4	7			
5	1			
6	—			
7	—			
8	2			
9				
10				
11				
12				
Total	17			

प्र./Q.No.

Q.2

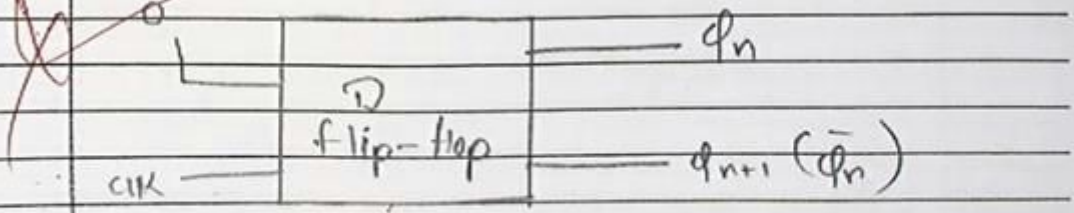
D flip-flop is a flip-flop which take one input and given two output

Logic Diagram of D flip-flop



In D-flip-flop there are four nand gate as N1, N2, N3 and N4
Input N1 and N2 is same that is D and clock pulse (CLK)
Input N3 and N4 are having the input as output of N1 and N2 and second input as the next state output of N3 and N4.
D is the input giving to the N1 and N2 is the same and in the simultaneous format.

Symbol / Block Diagram.



Y. E. /Q.No.

Truth table

Input		Output		
CLK	D	Q_n	$Q_{n+1}(\bar{Q}_n)$	State
0	0	Qn	Q_{n+1}	
1	0	0 or 1	1	change
1	1	0 or 1	0	change

In D - flip-flop when clock pulse is active high we can use the flip-flop as D-flip-flop
When D is active low the present (Q_n) state becomes 0 (low) or 1 (high)

When D is active high the next (Q_{n+1}) state becomes 0 (low)

When D is active low the next state (Q_{n+1}) becomes 1 (high)

When D is active high the present state (Q_n) becomes 0 (low)

प्र./Q.No.

Q.2

B
- Asynchronous counter is counter which is used as a temporary memory.
- Asynchronous counter is a type of counter in which the clock pulse is give each flip-flop is individually different.
- In this counter flip-flops are connected in such manner that the ouput of the first flip-flop is feeded to the clock pulse of the next flip-flop.
- The flip-flop's clock-pulses are not same for each-flip-flop.
- To design a n-bit asynchronous we need n (number of flip-flops)
- Types of Asynchronous counter
  - ↳ (1) Up counter
  - ↳ (2) Down Counter

- To design a 3-bit Asynchronous up counter we need 3 flip-flop.
- As given by using J-K-flip flop
- We will need 3 J-K flip-flop to design a 3-bit Asynchronous up counter.
- If 3 flip-flops are used then the possible input combinations are 2^n

$\therefore n = 3$

n = number of flip-flops

$\therefore 2^n = 2^3 = 8$

$\therefore$ 8 possible inputs are needed to design 3-bit asynchronous counter

Truth-table of J-K flipflop

Inputs		Outputs		State
J	K	Q_n	Q_{n+1}	Y
0	0	Q_n	Q_{n+1}	No change
0	1	0	0 1	0 (set)
1	0	1	0	1 (reset)
1	1	Q_{n+1}	Q_n	Toggle

When J = K = same (then the state is no change or the output gets toggle)

When J = 1 and K = 0
then the output is said to be in reset state.

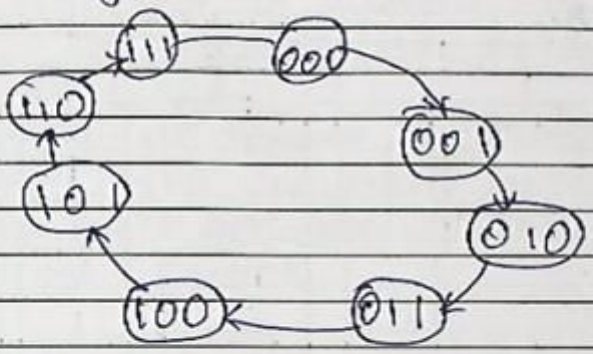
When J = 0 and K = 1
then the output is said to be in set state.

Excitation table for J-K- flop.

Q_n	Q_{n+1}	J	K
0	0	1	X
0	1	0	X
1	0	X	1
1	1	X	0

000
001
010
011
100
101
110
111

Flow diagram



As it is up-counter it start from 0 to 7 (000 to 111)

Output Table for 3-bit Asychronous up counter

Present state			Next State			output					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	1	X	1	X	1	X
0	0	1	1	1	1	0	X	0	X	X	1
0	1	0	1	1	0	0	X	X	1	1	X
0	1	1	1	0	1	0	X	X	0	X	1
1	0	0	1	0	0	X	1	1	X	1	X
1	0	1	0	1	1	X	0	0	X	X	1
1	1	0	0	1	0	X	0	X	1	X	X
1	1	1	0	0	1	X	0	X	0	X	1

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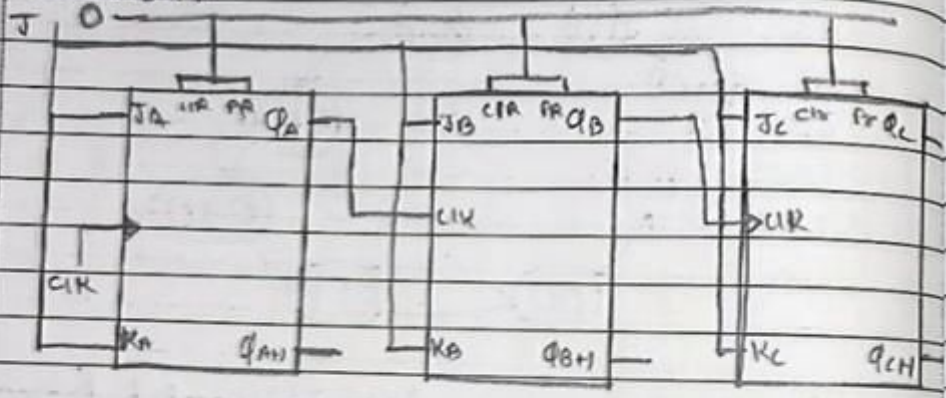
P. E. /Q.No.

Implementation of 3-bit Asychrounous counter.



Q.No.

Q.2

c) The registers is a device which is capable of storing the data instructions and addresses
Register is capable of transforming binary (data sequence) instructions either to the right side or left side are called as level shifter.

Thus, the flip-flop are arrange is cascated format are output of one flip-flop is connected to the input of another flip-flop
All the flip-flop gets the same clock pulse due to which flip-flop instruction are transformation
The flip-flops and registers are cascated the input in involveds or delivered

Types of shift registers

1) SISO
SISO means (shift in shift Out)

2) PISO

3) CISO

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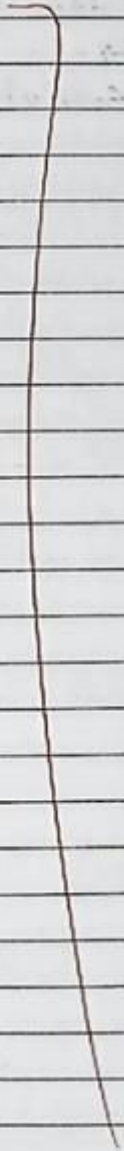

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Q. K./Q.No.

Applicat

1) used as flag register
2) used to store data
3) used to convert serial to parallel converter

Q. No. / Q.No.

Q.4

a) Register is an electronic devices which acts as a temporary memory to store data, instructions or any other binary sequence.
In computer there are many types of registers.
A computer itself is made up of using registers and transisters.
A computer's main compenents are.
1) ALU (Arithmatic logic unit)
↳ control circuit
↳ Accumulator.
2) Memory → It consists of data and instructions.

3) Input / Output devices → Peripherals.

Q. No./Q.No.

In computer organization various types of register are used to maintain the architect of the computer.

1) PC (Program Counter)
   - ↳ It is a register
   - ↳ It holds the starting addressing of next instructions.

2) MAR/AR (Memory Address Register)
   - ↳ It is a register
   - ↳ It holds the address of the data and instruction.
   - ↳ MAR is connected to the memory using address bus.

3) MBR/MDR/DR (Memory Buffer/Data register)
   - ↳ It is a register.
   - ↳ Holds the data and also instructions.
   - ↳ MBR is connected to the memory using data bus.

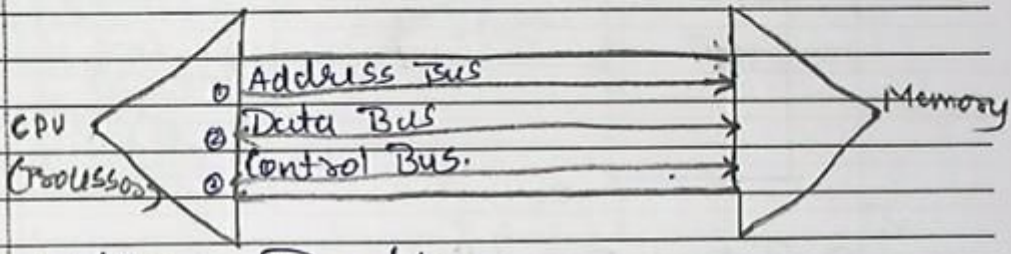
4) IR (Instruction register)
   - ↳ This is type of register in which instruction are predefined
   - ↳ It decodes the instruction and sends to MAR.

5) CI CKT (Control Circuit)
   - ↳ It is a register.
   - ↳ It controls the flow of the prog...

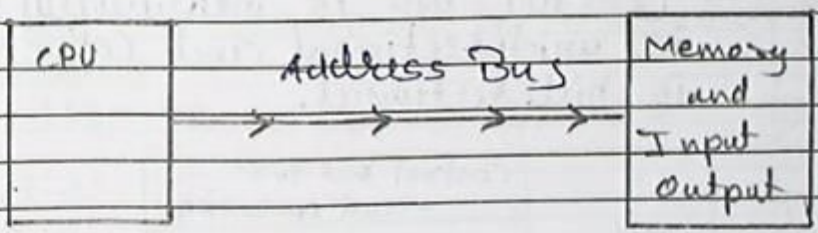
प्र. क्र./Q.No.

Q4 b) Multiple Bus organization is nothing but it is the system bus in which the data, instructions and addresses are flowed.

There are mainly three types of bus
1) Address Bus / line
2) Data Bus / line
3) Control Bus / line. — read, write



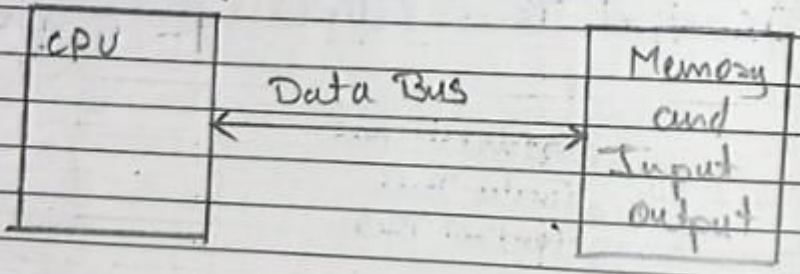
① Address Bus / line.
- This line is used to send the address from the CPU or processor to the memory.
- Address Bus is unidirectional.



② Data Bus / line.

↳ This line is used to send data from CPU to memory or from memory to CPU.

↳ Data Bus is Bidirectional.



③ Control Bus / line.

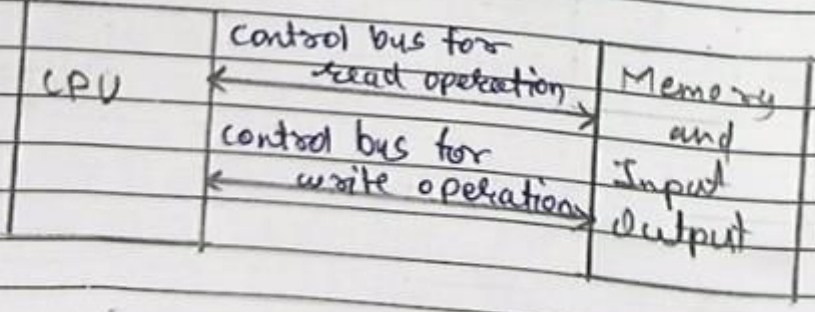
↳ This control the flow of program.

↳ This bus has two operations

① Memory (Read) / Read
LOAD

② Memory (write) / write.
Store

↳ Control bus is individually ~~unidirectional~~ is unidirectional and collectively is bidirectional.



Q.4

c)

Sections Of Comparison	Hardwired Control Unit	Micro Programmed Control Unit
1) Speed	fast	Slow
2) flexibility	non-flexible	flexible
3) design	complex	easier
4) Approach of towards complex instruction	Difficult	Easier.
5) Application	RISC	CISC
6) Control unit space	large	small.
7) No of instructions	Small	large
8) No of addressing modes.	large	Small

4

	Q.No.						TOTAL
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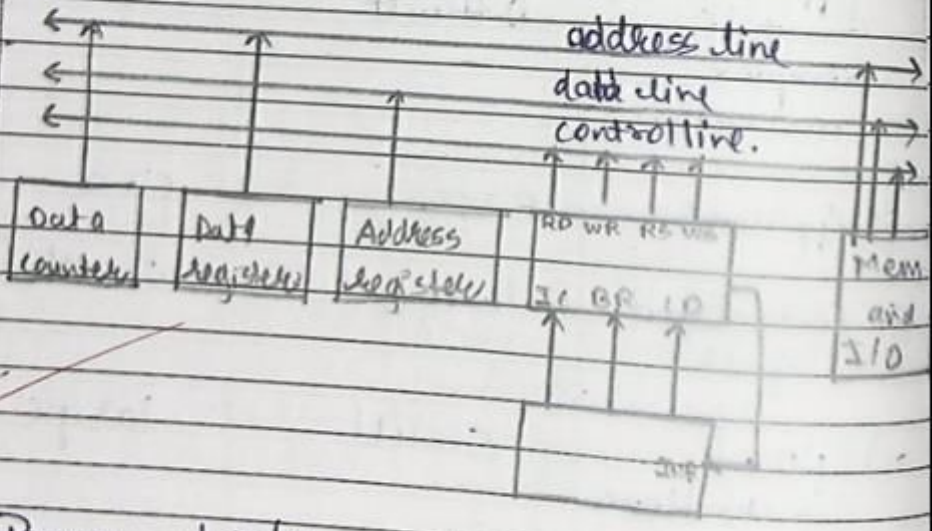
Q. No.

Q.8

a) DMA

It means Direct Memory Addressing. Direct memory addressing is a hardware in which data tranfer in huge amount is done using the DMA.

It consists of data registers, address registers and processors which are connected to the system bus lines



Programmed I/O	Interrupt Driven I/o
By the programmers	By the processor.

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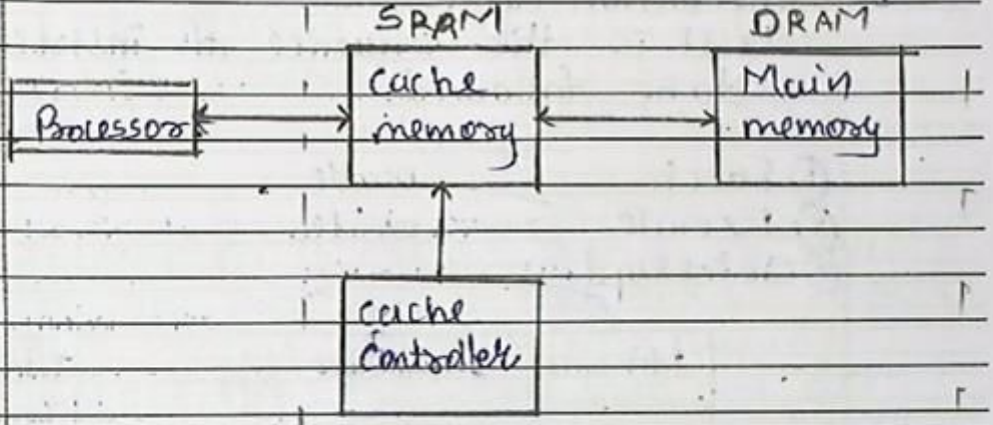
Q. 8

b)



cache memory is a memory which is used to improve the programs speed. The data is transfered from main memory and also to the processor. the SRAM part is called as cache memory.

Cache Coherency.

↳ When the data is copied to the main memory and cache memory, but the data of the both memory is different or the data is been changed is called as cache coherence.

↳ The differ data from cache memory with respect to the main memory is called as, cache coherency.

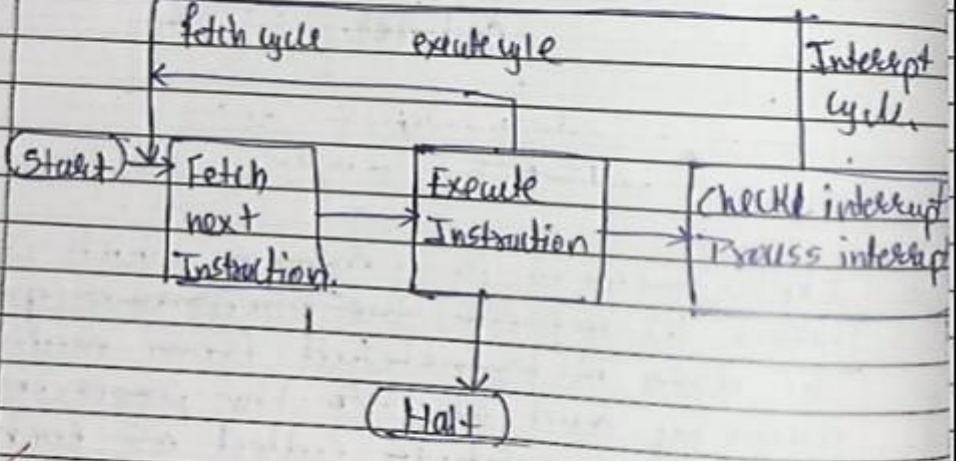
Q. P. /Q.No.

Q.5 Interrupt

b) Instruction Cycle

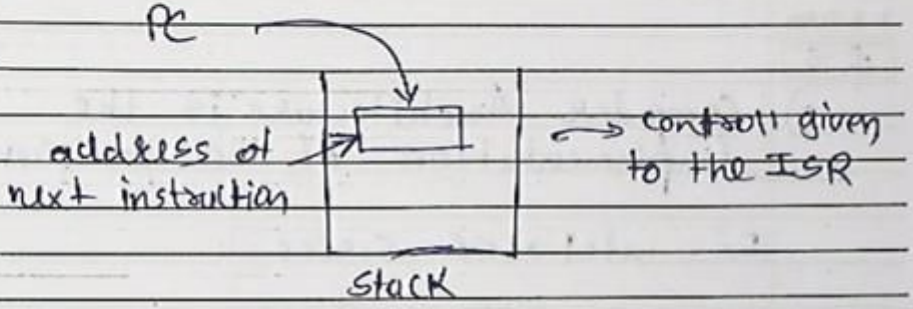
↳ It is the sequence of instructions to be followed.

1. Fetch — Decode
2. Execute — execute.
3. Interrupt



When the fetch and execute cycle is completed it checks for the interruption and then processes the interruption. then fetch the next instruction.

When ~~interrupt~~ interrupt is accured. the PC is been Push to the stack. (address of next instruction) and then the control is given to ISR (Interrupt Sub routine)



Interruption is error which is pop when the one program is run and we have send another program for running forcefully then the first program get interrupted and stop working and start the processing for second program

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S. E. /Q.No.

Q. 8

c) Computer Architecture is the implementation of the program

Ex intel x86 series

intel 3086
intel 3086
intel 4086
intel. 5086

thus, their organization is same but their architeture is different.

i) Multi-core advantages

- uses the data
- It has low frequency

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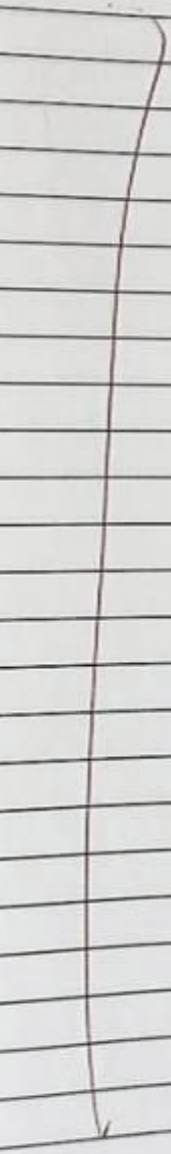

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