Step

COMPUTER SYSTEM ARCHITECTURE

LAB REPORT #01

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Introduction to Vivado &Venus

1. Introduction to Vivado

Vivado Design Suite is a software developed by **Xilinx (now AMD)** for **FPGA (Field Programmable Gate Array)** and **SoC (System-on-Chip)** design. It provides a complete environment for:

- Hardware description (using VHDL, Verilog, or SystemVerilog)
- IP (Intellectual Property) integration
- Synthesis and implementation
- Simulation and debugging
- Bitstream generation for FPGA programming

Key Features of Vivado

- Supports both **RTL design** and **High-Level Synthesis (HLS)**.
- Provides **Block Design** for graphical hardware development.
- Includes **Vivado Simulator** for testing HDL designs.
- Integration with **Xilinx SDK / Vitis** for software development on FPGA SoCs.
- Compatible with Zynq, Artix, Kintex, Virtex, and Spartan FPGAs.
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Lab Objectives:

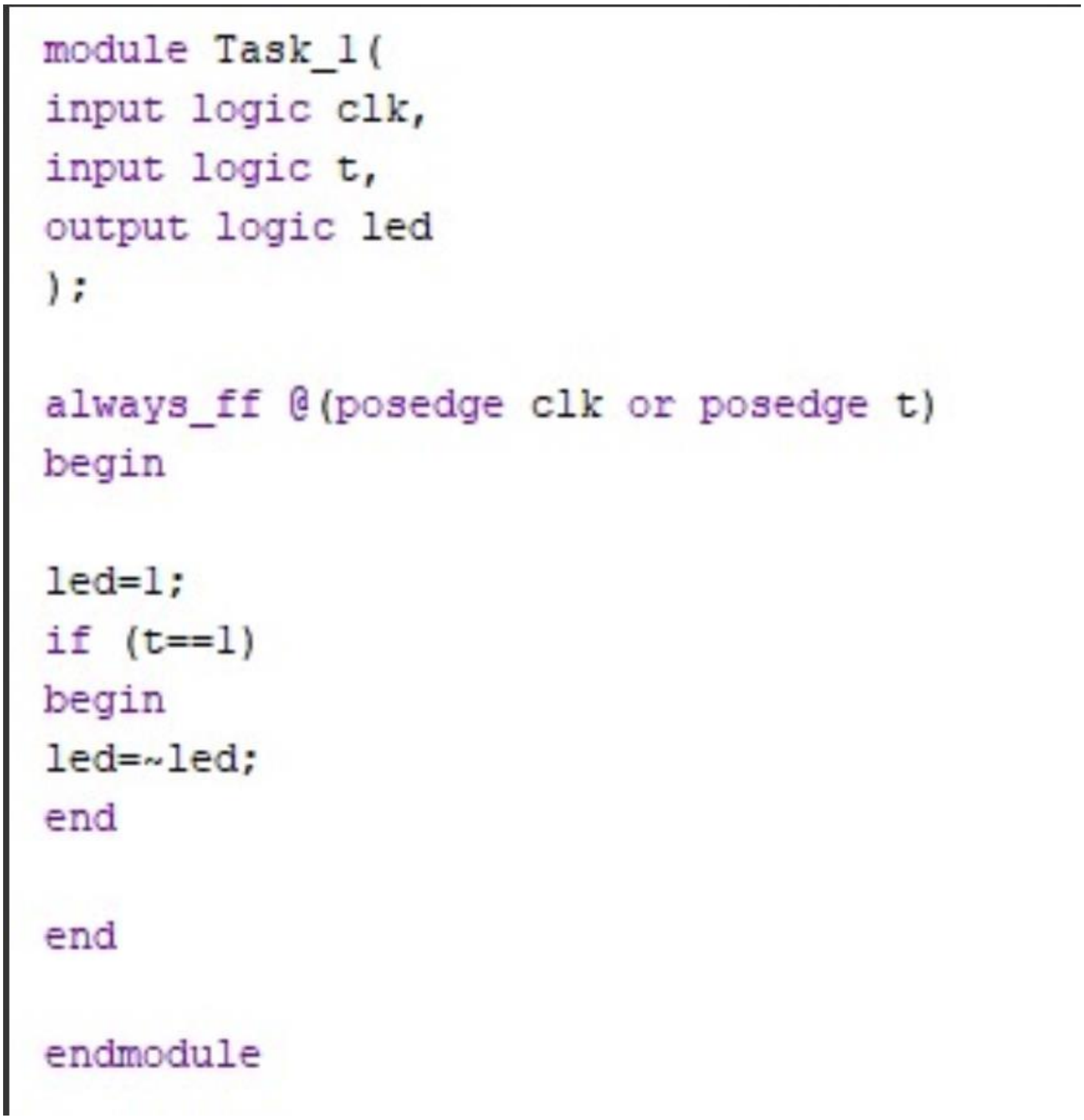
- The main objective of this lab is to understand basics of system Verilog and how do they work.

Sofwares: The lab was carried out using Xilinx Vivado for SystemVerilog coding, simulation, and waveform analysis, which provided an environment to design and verify digital circuits. Venus RISC-V simulator was used to write and execute assembly code step by step, allowing detailed observation of instruction flow and machine code generation. Together, these tools offered both hardware-level and software-level insights.

Task:

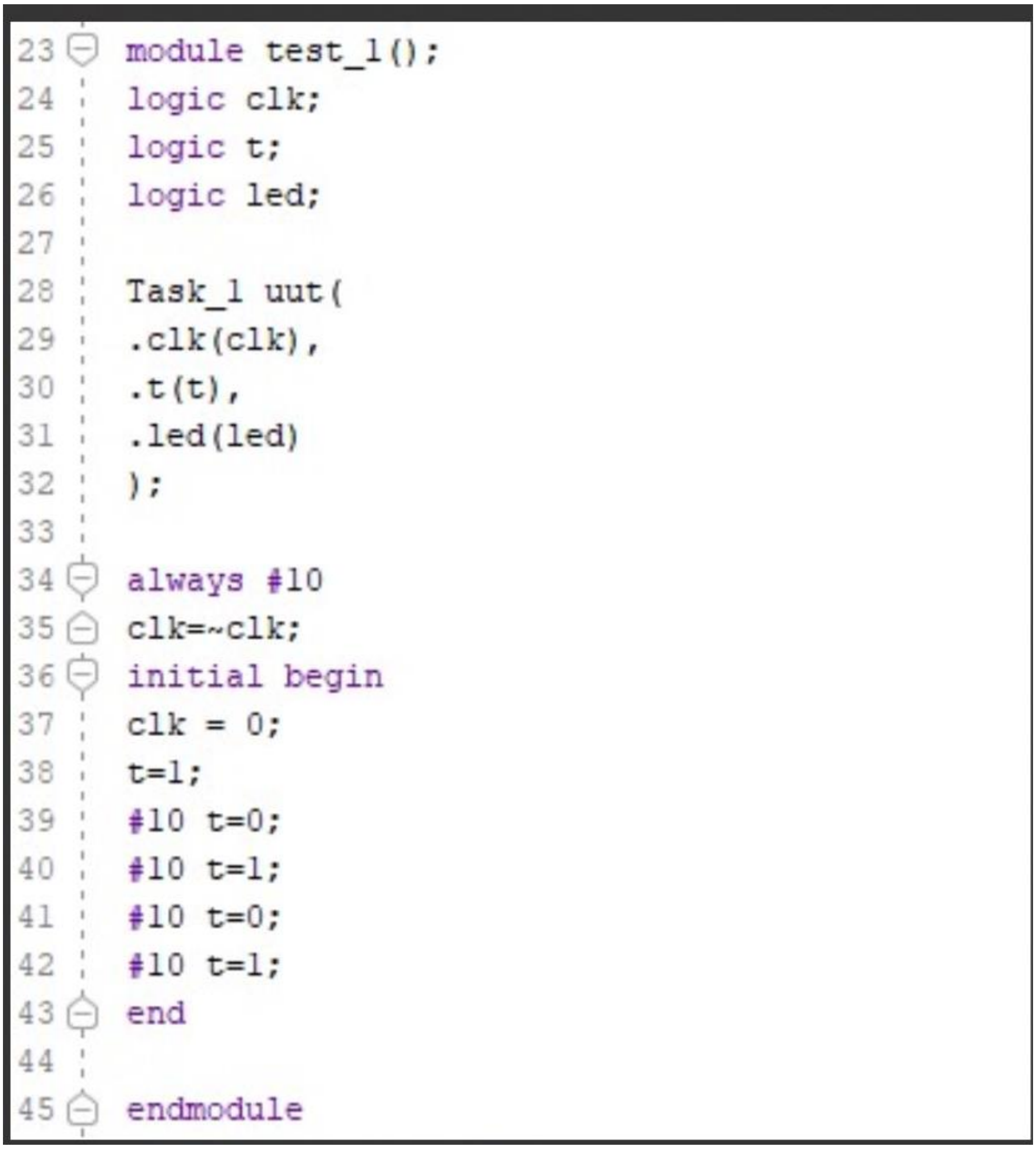
Implement the simulation of toggling of LED in System Verilog and show the waveform.

System Verilog code:



```
module Task_1(
input logic clk,
input logic t,
output logic led
);

always_ff @(posedge clk or posedge t)
begin

led=1;
if (t==1)
begin
led=~led;
end

end

endmodule
```

Testbench Code:



```
module test_1();
logic clk;
logic t;
logic led;

Task_1 uut(
.clk(clk),
.t(t),
.led(led)
);

always #10
clk=~clk;
initial begin
clk = 0;
t=1;
#10 t=0;
#10 t=1;
#10 t=0;
#10 t=1;
end

endmodule
```

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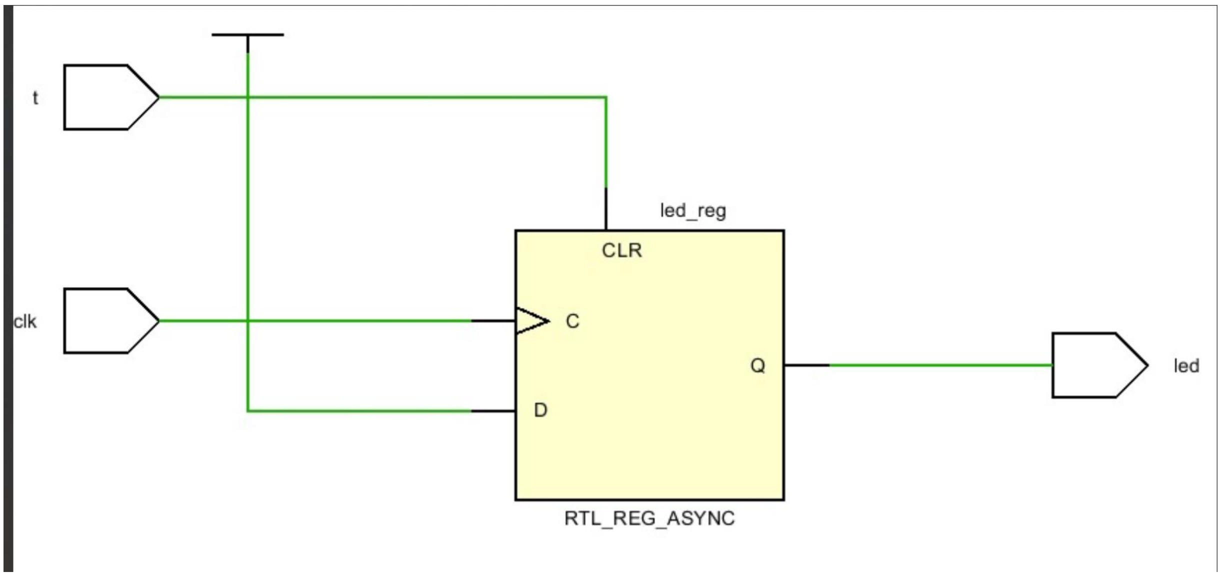
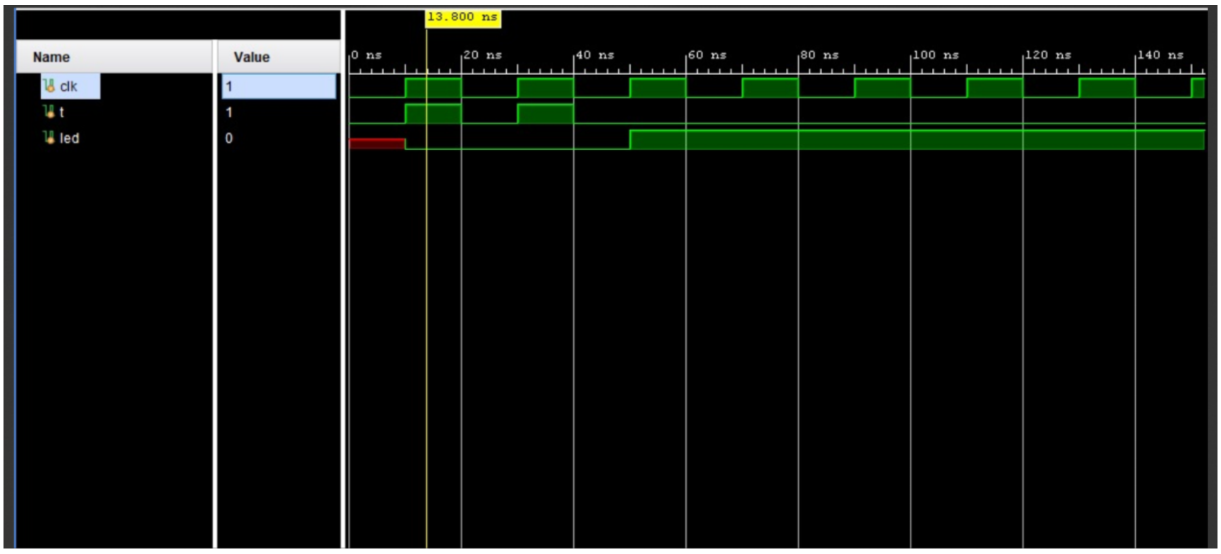
Schematic Diagram



Simulation Diagram



Introduction to Venus Software

Venus is an **educational tool** often used for **MIPS Assembly Language** simulation and learning. It provides a simple environment for writing, assembling, and executing **MIPS assembly programs**.

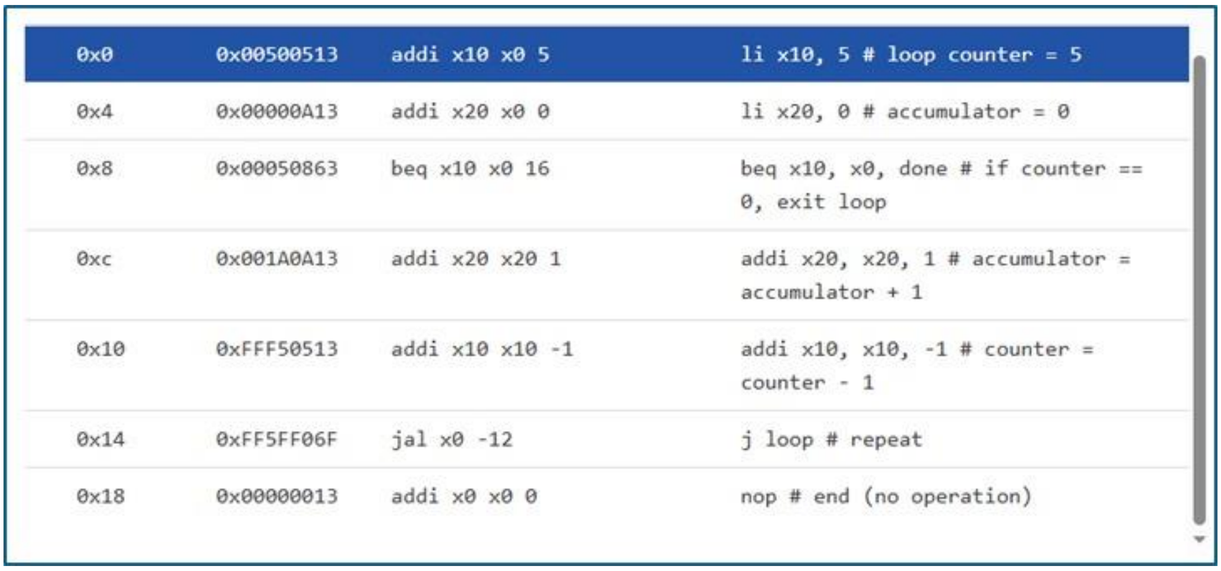
Key Features of Venus

- Web-based and lightweight (can also run locally).
- Supports standard **MIPS assembly instructions**.
- Provides an **editor, assembler, and simulator** in one environment.
- Helps students understand **instruction execution, registers, and memory operations**.
- Easy visualization of registers, stack, and memory.

Why Use Venus?

- Beginner-friendly for learning **Computer Organization & Assembly Language**.
- No complex installation required (runs in browser or via JAR file).
- Useful for students and teachers in **computer architecture courses**.

Explore more about venus and write above code and execute step by step and write all the instructions and their machine code



0x0	0x00500513	addi x10 x0 5	li x10, 5 # loop counter = 5
0x4	0x00000A13	addi x20 x0 0	li x20, 0 # accumulator = 0
0x8	0x00050863	beq x10 x0 16	beq x10, x0, done # if counter == 0, exit loop
0xc	0x001A0A13	addi x20 x20 1	addi x20, x20, 1 # accumulator = accumulator + 1
0x10	0xFFF50513	addi x10 x10 -1	addi x10, x10, -1 # counter = counter - 1
0x14	0xFF5FF06F	jal x0 -12	j loop # repeat
0x18	0x00000013	addi x0 x0 0	nop # end (no operation)

Conclusion:

In this lab, the simulation of LED toggling in SystemVerilog was successfully implemented and verified through waveform analysis, and the step-by-step execution of assembly code in Venus was explored along with its corresponding machine code. These tasks provided practical understanding of hardware simulation, waveform interpretation, and the mapping between assembly instructions and machine-level representation, building a strong foundation for future

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