

IRF1010E

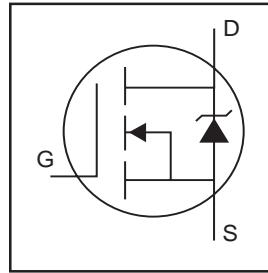
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

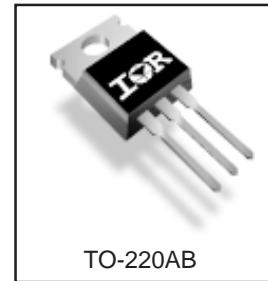
Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



$V_{DSS} = 60V$
$R_{DS(on)} = 12m\Omega$
$I_D = 84A\text{ }\textcircled{\text{7}}$



TO-220AB

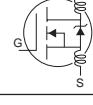
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	84\text{ }\textcircled{\text{7}}	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	59	
I_{DM}	Pulsed Drain Current \textcircled{\text{1}}	330	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.4	W/\text{°C}
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current\textcircled{\text{1}}	50	A
E_{AR}	Repetitive Avalanche Energy\textcircled{\text{1}}	17	mJ
dv/dt	Peak Diode Recovery dv/dt \textcircled{\text{3}}	4.0	V/ns
T_J	Operating Junction and	-55 to + 175	\text{°C}
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	300 (1.6mm from case)	
		10 lbf\text{-in} (1.1N\text{-m})	

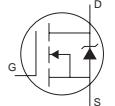
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	\text{°C/W}
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.064	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	12	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 50\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
g_f	Forward Transconductance	69	—	—	S	$V_{DS} = 25\text{V}, I_D = 50\text{A}$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
Q_g	Total Gate Charge	—	—	130	nC	$I_D = 50\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	28		$V_{DS} = 48\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	44		$V_{GS} = 10\text{V}, \text{See Fig. 6 and 13}$
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 30\text{V}$
t_r	Rise Time	—	78	—		$I_D = 50\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	48	—		$R_G = 3.6\Omega$
t_f	Fall Time	—	53	—		$V_{GS} = 10\text{V}, \text{See Fig. 10}$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3210	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	690	—		$V_{DS} = 25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	140	—		$f = 1.0\text{MHz}, \text{See Fig. 5}$
E_{AS}	Single Pulse Avalanche Energy ②	—	1180 ⑤ 320 ⑥	mJ	$I_{AS} = 50\text{A}, L = 260\mu\text{H}$	

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	84 ⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	330		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50\text{A}, V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	73	110	ns	$T_J = 25^\circ\text{C}, I_F = 50\text{A}$
Q_{rr}	Reverse Recovery Charge	—	220	330	nC	$di/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
 ② Starting $T_J = 25^\circ\text{C}$, $L = 260\mu\text{H}$
 $R_G = 25\Omega$, $I_{AS} = 50\text{A}$, $V_{GS} = 10\text{V}$ (See Figure 12)
 ③ $V_{SD} \leq 50\text{V}$, $di/dt \leq 230\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
 ⑤ This is a typical value at device destruction and represents operation outside rated limits.
 ⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.
 ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

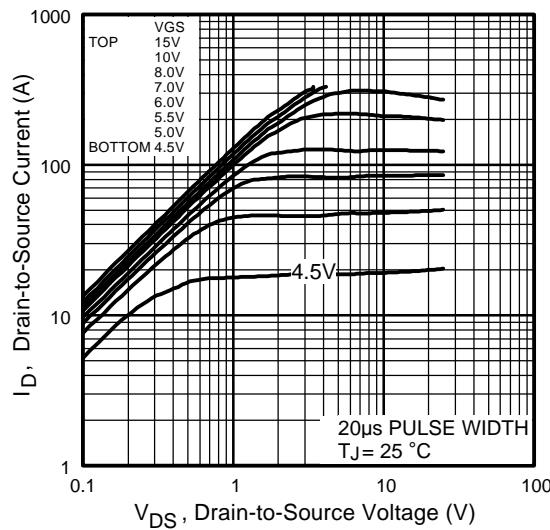


Fig 1. Typical Output Characteristics

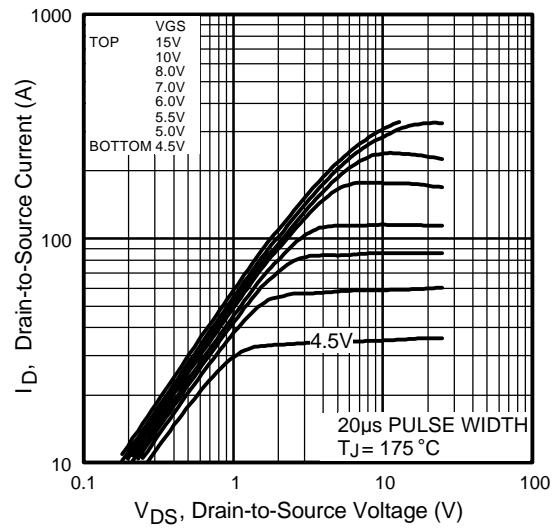


Fig 2. Typical Output Characteristics

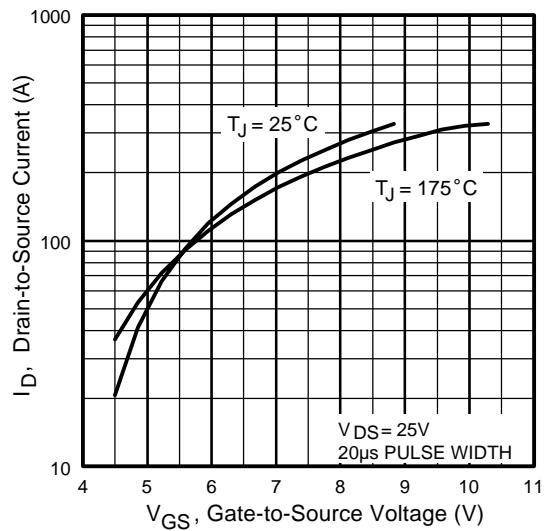


Fig 3. Typical Transfer Characteristics

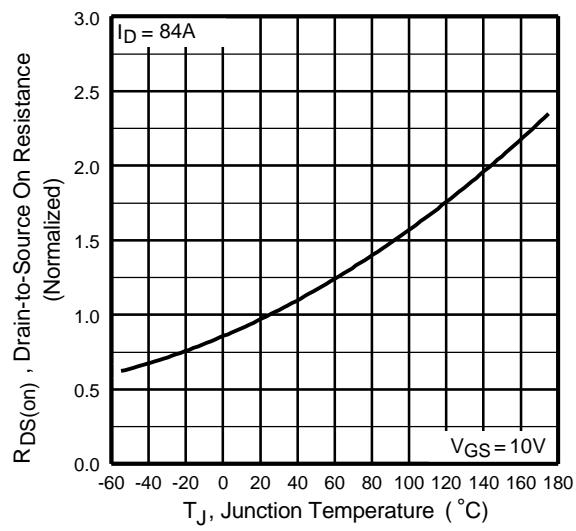


Fig 4. Normalized On-Resistance
Vs. Temperature

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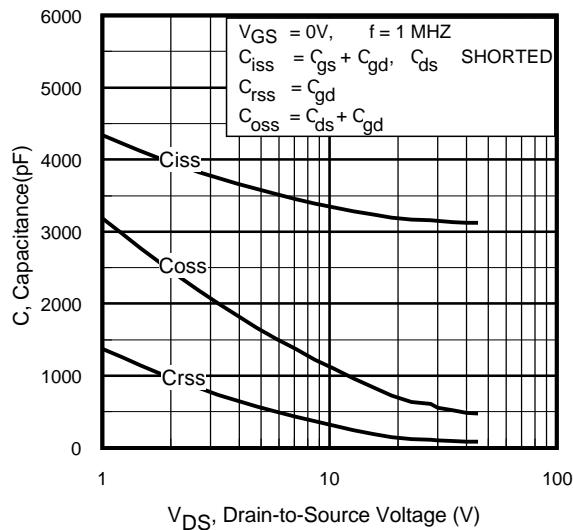


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

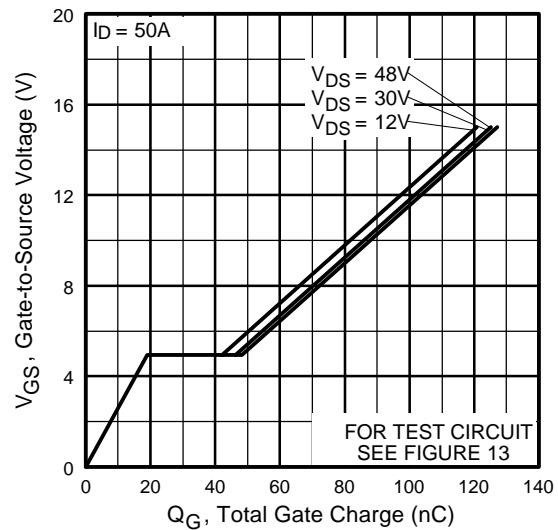


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

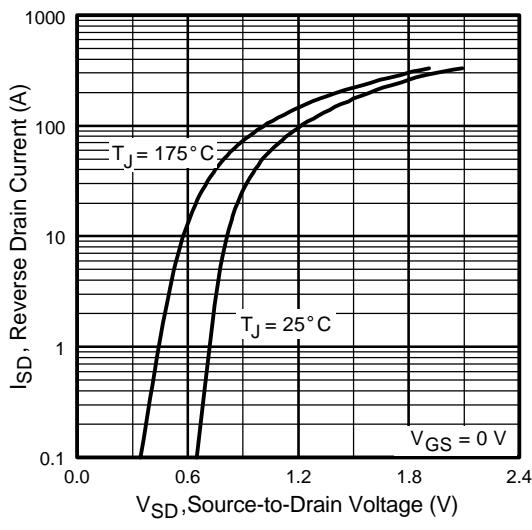


Fig 7. Typical Source-Drain Diode
Forward Voltage

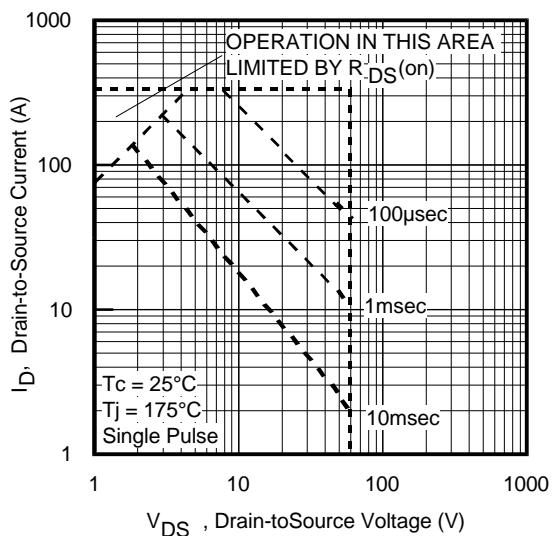


Fig 8. Maximum Safe Operating Area

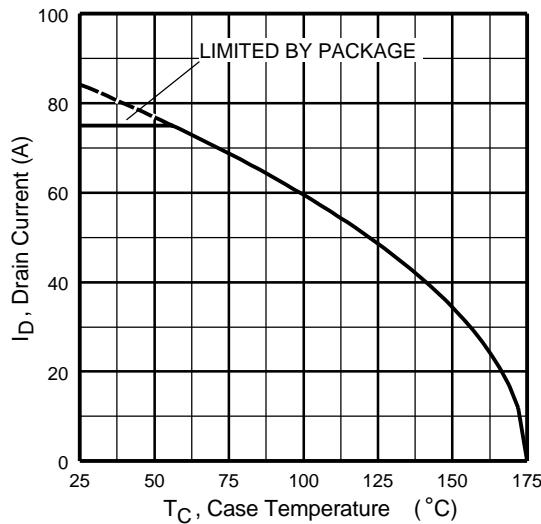


Fig 9. Maximum Drain Current Vs.
Case Temperature

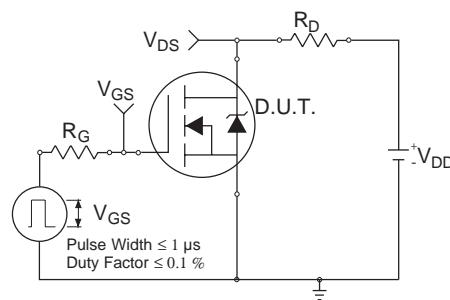


Fig 10a. Switching Time Test Circuit

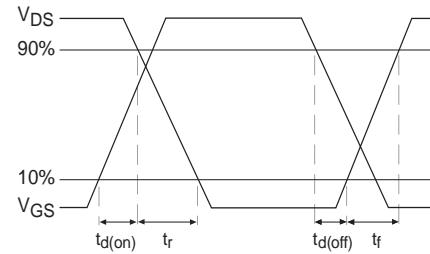


Fig 10b. Switching Time Waveforms

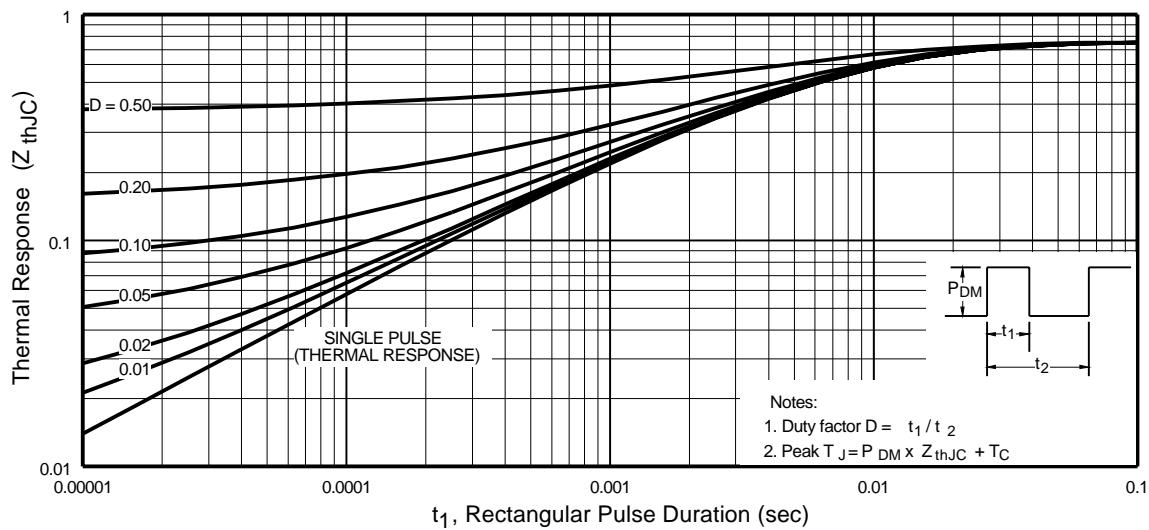


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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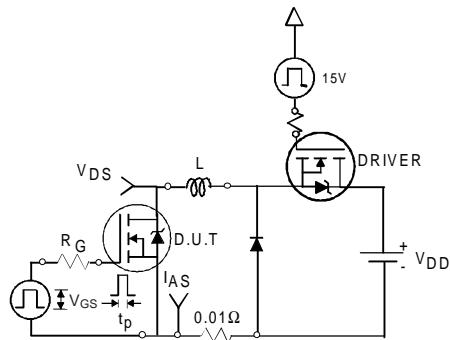


Fig 12a. Unclamped Inductive Test Circuit

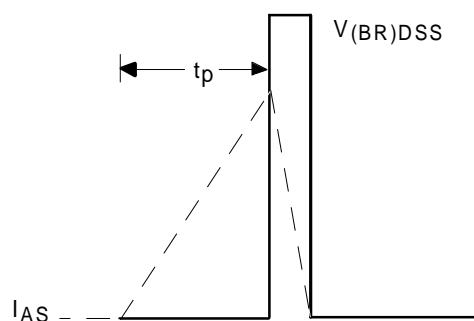


Fig 12b. Unclamped Inductive Waveforms

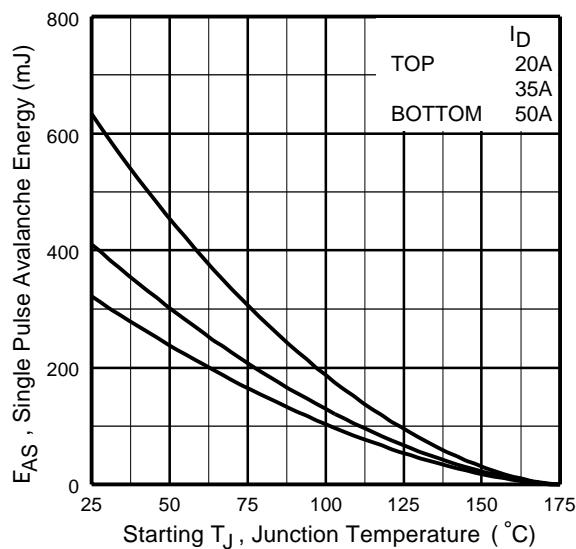


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

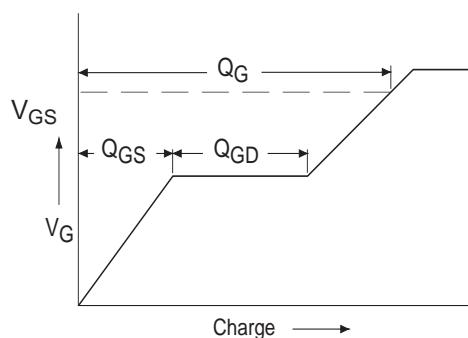


Fig 13a. Basic Gate Charge Waveform

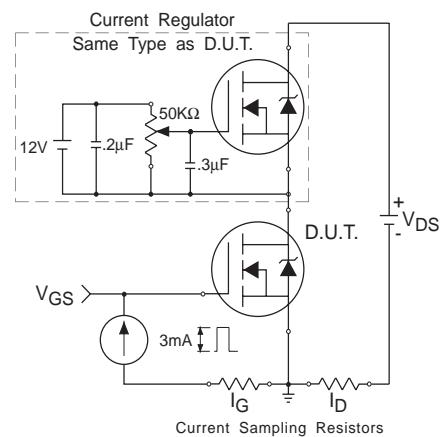
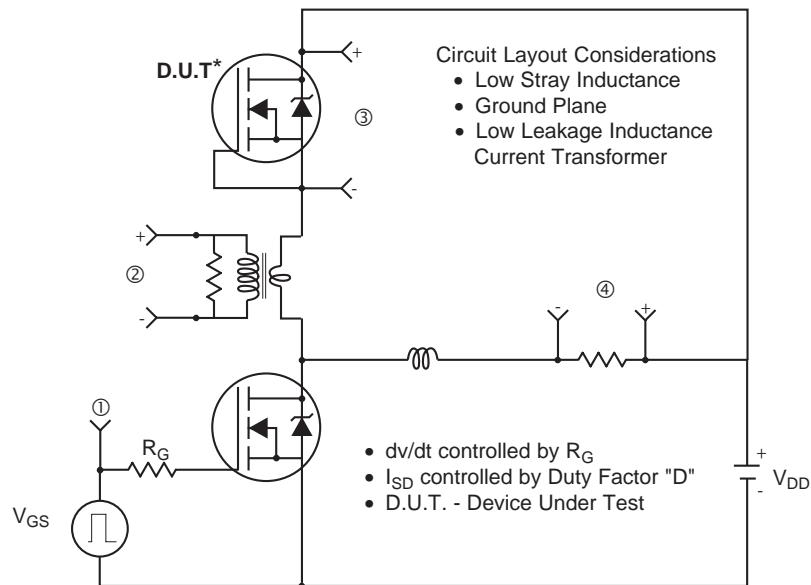
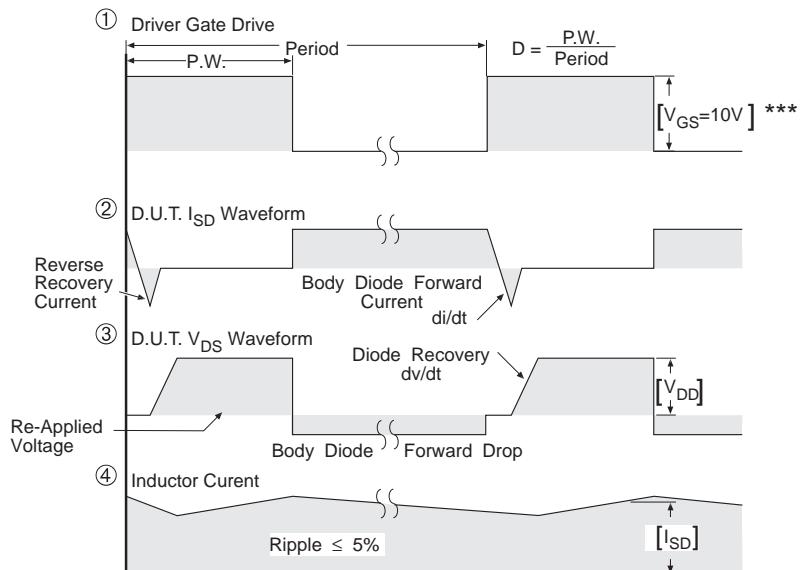


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

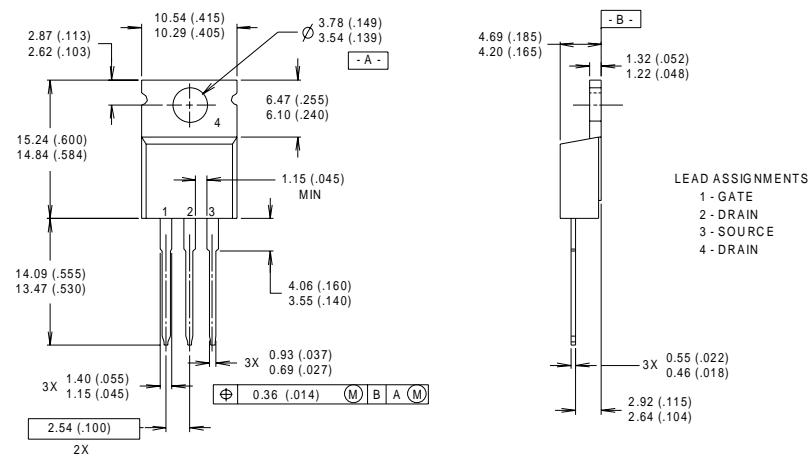
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Package Outline

TO-220AB

Dimensions are shown in millimeters (inches)



NOTES:

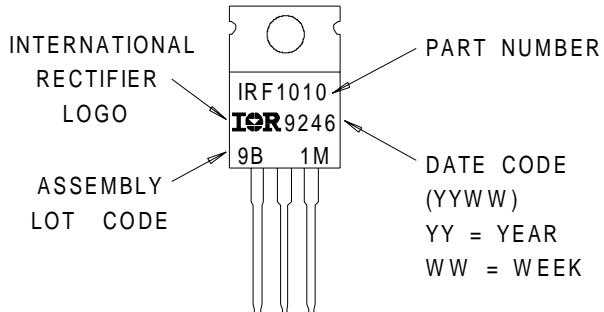
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Data and specifications subject to change without notice.
This product has been designed and qualified for the automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>