Group-4Week-1 Day-5 Task-1

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4x1 MUX VHDL Code and Timing analysis

Design code:

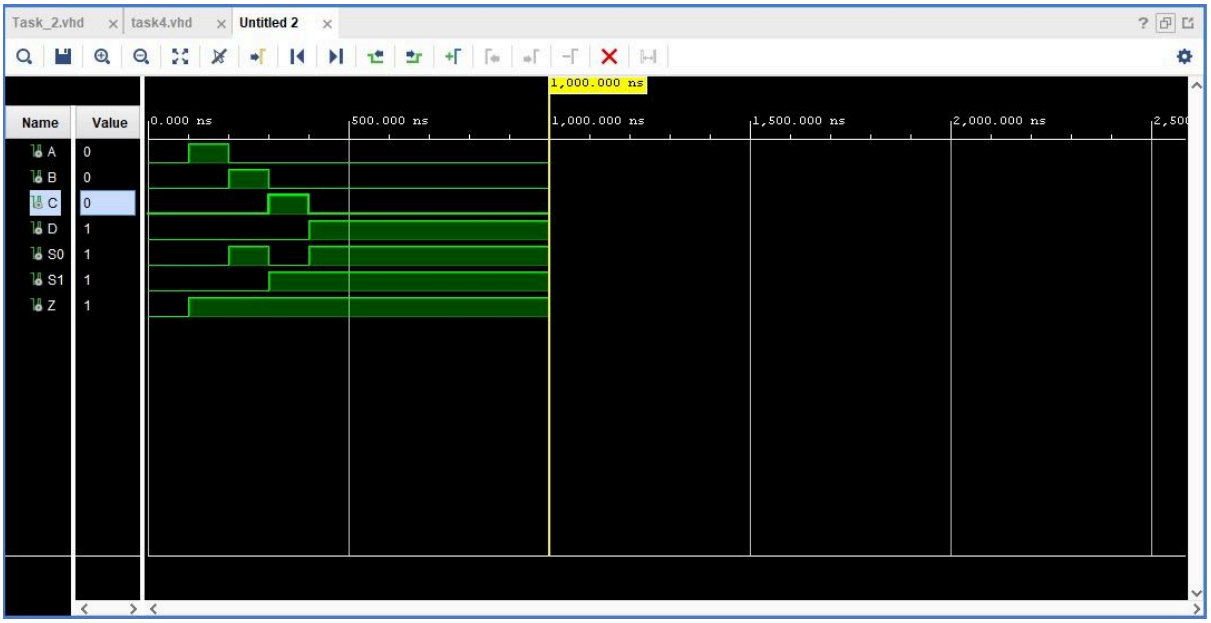
```
library IEEE;
use IEEE.std_logic_1164.all;

entity MUX41 is
port(
in0 : in std_logic ;
in1 : in std_logic ;
in2 : in std_logic ;
in3 : in std_logic ;
sg0 : in std_logic ;
sg1 : in std_logic ;
y : out std_logic
);
end MUX41 ;

architecture MUX of MUX41 is
signal x1,x2,x3,x4 : std_logic ;
begin
x1 <= (not sg0)and(not sg1)and(in0);
x2 <= (not sg0)and sg1 and in1;
x3 <= sg0 and(not sg1) and in2;
x4 <= sg0 and sg1 and in3;
y <= x1 and x2 and x3 and x4;
end MUX ;
```

TestBench code:

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MUX41_tb is
end MUX41_tb;

architecture tb_arch of MUX41_tb is

  -- Component declaration for MUX41
  component MUX41
    port(
      in0 : in std_logic;
      in1 : in std_logic;
      in2 : in std_logic;
      in3 : in std_logic;
      sg0 : in std_logic;
      sg1 : in std_logic;
      y   : out std_logic
    );
  end component;

  -- Signals for testbench
  signal in0_tb, in1_tb, in2_tb, in3_tb, sg0_tb, sg1_tb : std_logic;
  signal y_tb : std_logic;

begin

  -- Instantiate the MUX41 component
  UUT : MUX41
    port map(
      in0 => in0_tb,
      in1 => in1_tb,
      in2 => in2_tb,
      in3 => in3_tb,
      sg0 => sg0_tb,
      sg1 => sg1_tb,
      y   => y_tb
    );

  -- Stimulus process
  stimulus : process
  begin
    -- Test case 1: sg0 = '0', sg1 = '0'
    in0_tb <= '0';
```

```
    in1_tb <= '1';
    in2_tb <= '0';
    in3_tb <= '1';
    sg0_tb <= '0';
    sg1_tb <= '0';
    wait for 10 ns;

    -- Test case 2: sg0 = '0', sg1 = '1'
    in0_tb <= '1';
    in1_tb <= '0';
    in2_tb <= '1';
    in3_tb <= '0';
    sg0_tb <= '0';
    sg1_tb <= '1';
    wait for 10 ns;

    -- Test case 3: sg0 = '1', sg1 = '0'
    in0_tb <= '1';
    in1_tb <= '1';
    in2_tb <= '0';
    in3_tb <= '0';
    sg0_tb <= '1';
    sg1_tb <= '0';
    wait for 10 ns;

    -- Test case 4: sg0 = '1', sg1 = '1'
    in0_tb <= '0';
    in1_tb <= '0';
    in2_tb <= '0';
    in3_tb <= '1';
    sg0_tb <= '1';
    sg1_tb <= '1';
    wait for 10 ns;

    -- End of testbench
    wait;
  end process stimulus;

end tb_arch;
```

Timing analysis


Task_2.vhd
task4.vhd
Untitled 2
Name
Value
A
B
C
D
S0
S1
Z
0
0
0
1
1
1
1
0.000 ns
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
1,000.000 ns