

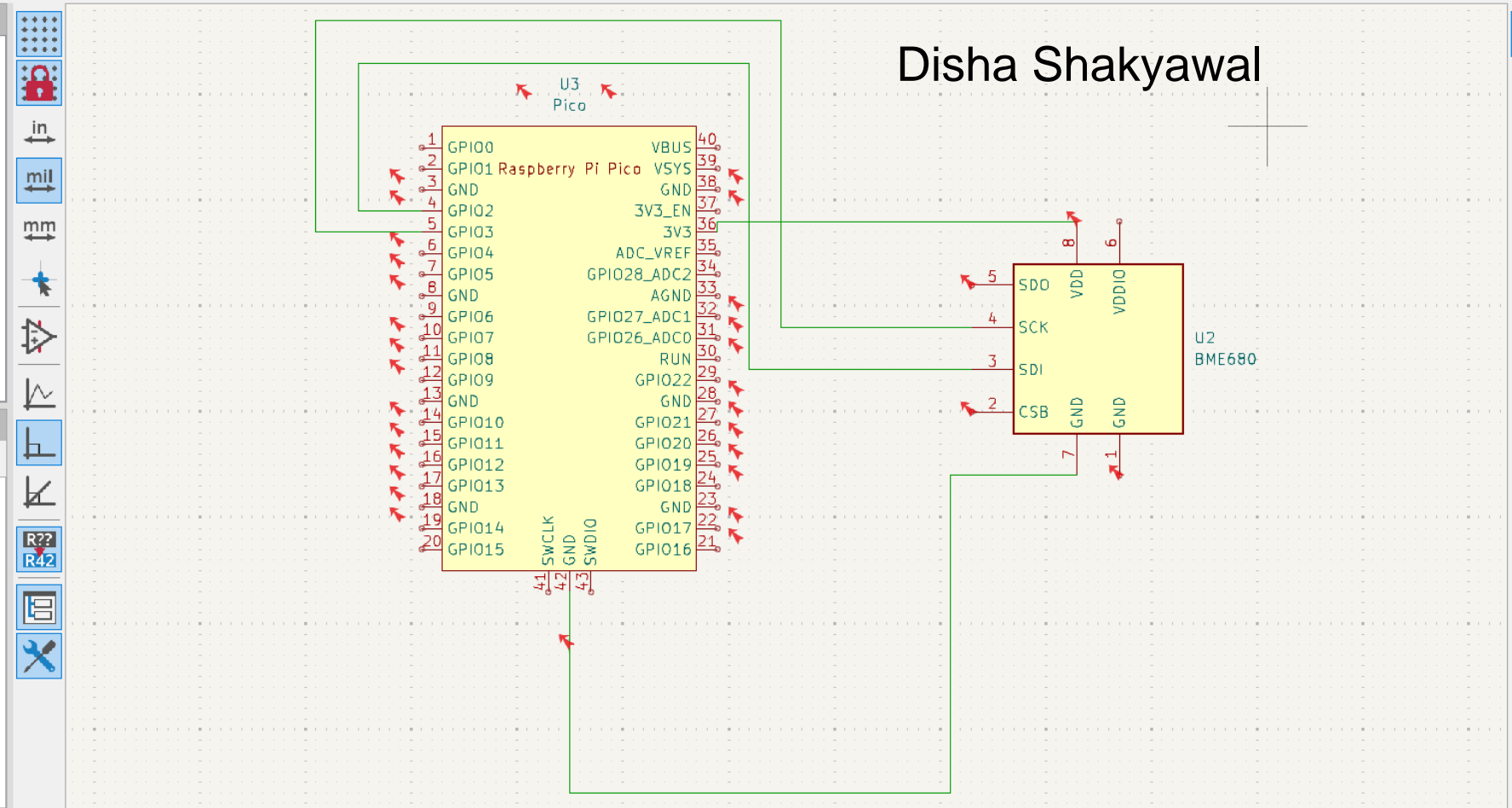


Schematic Hierarchy

Root (page 1)

Properties

No objects selected



Disha Shakyawal



Track: use netclass width Via: use netclass sizes Edge.Cuts 0.5000 mm (19.69 mils) Zoom 2.20



## Design Rules Checker

- ☒ Refill all zones before performing DRC ☐ Test for parity between PCB and schematic  
☐ Report all errors for each track

Violations (2) Unconnected Items (0) Schematic Parity (not run) Ignored Tests (4)

## ▼ Warning: Silkscreen clipped by board edge

Segment on Edge.Cuts

Footprint Text 'ADC\_VREF' of U3

## ▼ Warning: Silkscreen clipped by board edge

Segment on Edge.Cuts

Footprint Text '3V3\_EN' of U3

Show: ☐ All ☒ Errors 0 ☒ Warnings 2 ☐ Exclusions

Save...

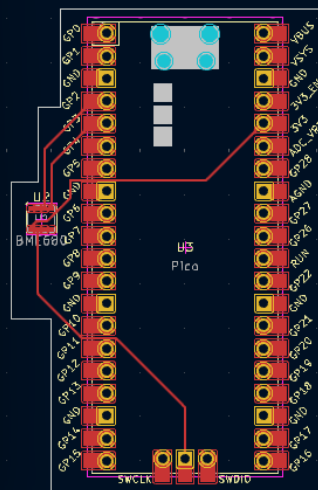
Delete Marker

Delete All Markers

Run DRC

Close

Copper Keepouts shown on Dwgs layer



## Appearance

Layers Objects Nets

- B.Paste
- F.Silkscreen
- B.Silkscreen
- F.Mask
- B.Mask
- User.Drawings
- User.Comments
- User.Eco1
- User.Eco2
- Edge.Cuts
- Margin
- F.Courtyard
- B.Courtyard

Layer Display Options

Presets (Ctrl+Tab):

All Layers

Viewports (Shift+Tab):

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## Selection Filter

- ☒ All items ☐ Locked items
- ☒ Footprints ☒ Text
- ☒ Tracks ☒ Vias
- ☒ Pads ☒ Graphics
- ☒ Zones ☒ Rule Areas
- ☒ Dimensions ☒ Other items

Pads 98 Vias 0 Track Segments 18 Nets 47 Unrouted 0

File 'C:\Users\Admin\Documents\r... Z 2.11 X 132.5000 Y 19.0000 dx 132.5000 dy 19.0000 dist 133.8553 grid 0.5000

mm Select item(s)



Search

ENG  
US15:28  
23-07-2024

