



ck: use Design Rules Checker (69 mils)

Design Rules Checker

☒ Refill all zones before performing DRC

☐ Test for parity between PCB and schematic

☐ Report all errors for each track

Violations (0)

Unconnected Items (0)

Schematic Parity (not run)

Ignored Tests (4)

Show: ☐ All ☒ Errors 0 ☒ Warnings 0 ☐ Exclusions

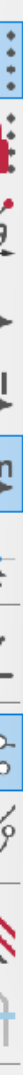
Delete Marker

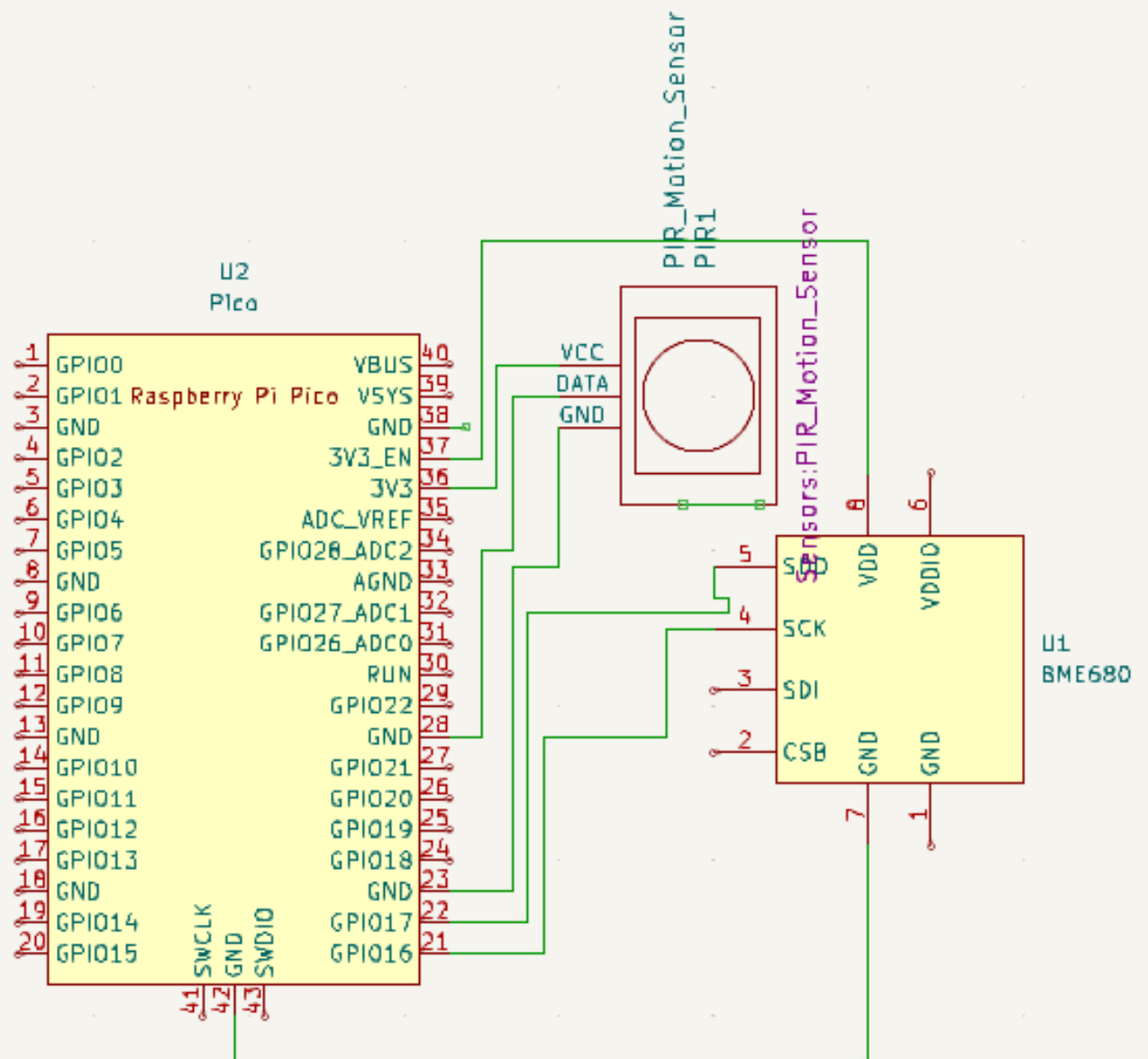
Delete All Markers

Run DRC

Close

Save...





Copper Keepouts shown on Dwgs layer

PIR1

