DC CIPAPA, Data or unified Cache line Clean and Invalidate by PA to PoPA

The DC CIPAPA characteristics are:

Purpose

Clean and Invalidate data cache by physical address to the Point of Physical Aliasing.

Note

This instruction cleans and invalidates all copies of the Location specified in the Xt argument, irrespective of any MECID associated with the Location. Memory accesses resulting from the Clean operation use the MECID associated with the cache entry.

Configuration

This instruction is present only when FEAT_RME is implemented. Otherwise, direct accesses to DC CIPAPA are undefined.

Attributes

DC CIPAPA is a 64-bit System instruction.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

NS NSE RESO PA
PA

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

NS, bit [63]

Together with the NSE field, this field specifies the target physical address space.

NSE	NS	Meaning	
0b0	0b0	Secure.	
0d0	0b1	Non-secure.	

NSE	NS	Meaning
0b1	0b0	Root.
0b1	0b1	Realm.

If FEAT_SEL2 is not implemented, and $\{NSE, NS\} == \{0b0, 0b0\}$, then no cache entries are required to be cleaned or invalidated

NSE, bit [62]

Together with the NS field, this field specifies the target physical address space.

For a description of the values derived by evaluating NS and NSE together, see DC CIPAPA.NS.

Bits [61:52]

Reserved, res0.

PA, bits [51:0]

Physical address to use. No alignment restrictions apply to this PA.

Executing DC CIPAPA

- This instruction is not subject to any translation, permission checks, or granule protection checks.
- This instruction affects all caches in the Outer Shareable shareability domain.
- This instruction has the same ordering, observability, and completion behavior as VA-based cache maintenance instructions issued to the Outer Shareable shareability domain.

Accesses to this instruction use the following encodings in the System instruction encoding space:

DC CIPAPA, <Xt>

op0	op1	CRn	CRm	op2
0b01	0b110	0b0111	0b1110	0b001

```
if PSTATE.EL == EL0 then
     UNDEFINED;
elsif PSTATE.EL == EL1 then
     UNDEFINED;
elsif PSTATE.EL == EL2 then
```

UNDEFINED;
elsif PSTATE.EL == EL3 then
 DC_CIPAPA(X[t, 64]);

AArch32 Registers AArch64 Registers AArch32 Instructions AArch64 Instructions Index by Encoding External Registers

 $28/03/2023\ 16:01;\ 72747e43966d6b97dcbd230a1b3f0421d1ea3d94$

Copyright \hat{A} © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.