<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding

Pseu

TST (immediate)

Test bits (immediate), setting the condition flags and discarding the result

: Rn AND imm.

This is an alias of ANDS (immediate). This means:

- The encodings in this description are named to match the encodings of <u>ANDS</u> (immediate).
- The description of <u>ANDS (immediate)</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31 30 2	9 28	27	26	25	24	23	22	21 20 19 18 17 16	15 14 13 12 11 10	9	8	7	6	5	4	3	2	1	0
sf 1 1	. 1	0	0	1	0	0	N	immr	imms			Rn			1	1	1	1	1
opc	:								-								Rd		

32-bit (sf == 0 && N == 0)

```
TST <Wn>, #<imm>
```

is equivalent to

```
ANDS WZR, <Wn>, #<imm>
```

and is always the preferred disassembly.

64-bit (sf == 1)

```
TST <Xn>, #<imm>
```

is equivalent to

```
ANDS XZR, <Xn>, #<imm>
```

and is always the preferred disassembly.

Assembler Symbols

<wn></wn>	Is the 32-bit name of the general-purpose source register, encoded in the "Rn" field.
<xn></xn>	Is the 64-bit name of the general-purpose source register, encoded in the "Rn" field.

<imm> For the 32-bit variant: is the bitmask immediate, encoded in
"imms:immr".

For the 64-bit variant: is the bitmask immediate, encoded in "N:imms:immr".

Operation

The description of <u>ANDS (immediate)</u> gives the operational pseudocode for this instruction.

BaseSIMD&FPSVESMEIndex byInstructionsInstructionsInstructionsInstructions

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel; Build timestamp: 2023-09-18T17:56

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