STUMIN, STUMINL

Atomic unsigned minimum on word or doubleword in memory, without return, atomically loads a 32-bit word or 64-bit doubleword from memory, compares it against the value held in a register, and stores the smaller value back to memory, treating the values as unsigned numbers.

- STUMIN does not have release semantics.
- STUMINL stores to memory with release semantics, as described in *Load-Acquire*, *Store-Release*.

For information about memory accesses, see *Load/Store addressing modes*.

This is an alias of <u>LDUMIN, LDUMINA, LDUMINAL, LDUMINL</u>. This means:

- The encodings in this description are named to match the encodings of LDUMIN, LDUMINA, LDUMINAL, LDUMINL.
- The description of <u>LDUMIN</u>, <u>LDUMINA</u>, <u>LDUMINAL</u>, <u>LDUMINL</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

Integer (FEAT_LSE)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

1 x 1 1 1 0 0 0 0 R 1 Rs 0 1 1 1 0 0 Rn 1 1 1 1 1

size A opc Rt
```

32-bit LDUMIN alias (size == 10 && R == 0)

```
STUMIN <Ws>, [<Xn | SP>]

is equivalent to

LDUMIN <Ws>, WZR, [<Xn | SP>]
```

and is always the preferred disassembly.

32-bit LDUMINL alias (size == 10 && R == 1)

```
STUMINL <Ws>, [<Xn | SP>]

is equivalent to

LDUMINL <Ws>, WZR, [<Xn | SP>]
```

and is always the preferred disassembly.

64-bit LDUMIN alias (size == 11 && R == 0)

```
STUMIN <Xs>, [<Xn | SP>]

is equivalent to

LDUMIN <Xs>, XZR, [<Xn | SP>]
```

and is always the preferred disassembly.

64-bit LDUMINL alias (size == 11 && R == 1)

```
STUMINL <Xs>, [<Xn|SP>]
is equivalent to
LDUMINL <Xs>, XZR, [<Xn|SP>]
```

and is always the preferred disassembly.

Assembler Symbols

<Ws> Is the 32-bit name of the general-purpose register holding

the data value to be operated on with the contents of the

memory location, encoded in the "Rs" field.

<Xs> Is the 64-bit name of the general-purpose register holding

the data value to be operated on with the contents of the

memory location, encoded in the "Rs" field.

<Xn|SP> Is the 64-bit name of the general-purpose base register or

stack pointer, encoded in the "Rn" field.

Operation

The description of <u>LDUMIN, LDUMINA</u>, <u>LDUMINAL</u>, <u>LDUMINL</u> gives the operational pseudocode for this instruction.

Operational information

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

<u>Base</u> <u>SIMD&FP</u> <u>SVE</u> <u>SME</u> <u>Index by</u> Instructions Instructions Instructions Encoding

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