GICR_STATUSR, Error Reporting Status Register

The GICR STATUSR characteristics are:

Purpose

Provides software with a mechanism to detect:

- Accesses to reserved locations.
- Writes to read-only locations.
- Reads of write-only locations.

Configuration

A copy of this register is provided for each Redistributor.

If the GIC implementation supports two Security states this register is Banked to provide Secure and Non-secure copies.

Attributes

GICR STATUSR is a 32-bit register.

Field descriptions

| 31302928272625242322212019181716151413121110 9 8 7 6 5 | 1 3 | 2 | 1 | 0 |
|--|------|------|-----|-----|
| RES0 | WROD | RWOD | WRD | RRD |

Bits [31:4]

Reserved, res0.

WROD, bit [3]

Write to an RO location.

| WROD | Meaning |
|------|--|
| 0d0 | Normal operation. |
| 0b1 | A write to an RO location has been detected. |

When a violation is detected, software must write 1 to this register to reset it.

RWOD, bit [2]

Read of a WO location.

| RWOD | Meaning |
|------|--|
| 0d0 | Normal operation. |
| 0b1 | A read of a WO location has been detected. |

When a violation is detected, software must write 1 to this register to reset it.

WRD, bit [1]

Write to a reserved location.

| WRD | Meaning |
|-----|---|
| 0b0 | Normal operation. |
| 0b1 | A write to a reserved location has been detected. |

When a violation is detected, software must write 1 to this register to reset it.

RRD, bit [0]

Read of a reserved location.

| RRD | Meaning |
|-----|--|
| 0b0 | Normal operation. |
| 0b1 | A read of a reserved location has been detected. |

When a violation is detected, software must write 1 to this register to reset it.

Accessing GICR_STATUSR

This is an optional register. If the register is not implemented, the location is RAZ/WI.

GICR STATUSR can be accessed through the memory-mapped interfaces:

| Component | Frame | Offset | Instance |
|----------------------|---------|--------|---------------------|
| GIC Redistributor | RD_base | 0x0010 | GICR_STATUSR (S) |

This interface is accessible as follows:

• When an access is Secure, accesses to this register are **RW**.

• When FEAT_RME is implemented and an access is Root, accesses to this register are **RW**.

| Component | Frame | Offset | Instance | |
|---------------|---------|--------|--------------|--|
| GIC | RD_base | 0x0010 | GICR_STATUSR | |
| Redistributor | _ | | (NS) | |

This interface is accessible as follows:

- When an access is Non-secure, accesses to this register are **RW**.
- When FEAT_RME is implemented and an access is Realm, accesses to this register are **RW**.

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