# MPAMF_MBW_IDR, MPAM Memory Bandwidth Partitioning Identification Register

The MPAMF_MBW_IDR characteristics are:

## Purpose

Indicates which MPAM bandwidth partitioning features are present on this MSC.

MPAMF_MBW_IDR_s indicates bandwidth partitioning features accessed from the Secure MPAM feature page. MPAMF_MBW_IDR_ns indicates bandwidth partitioning features accessed from the Non-secure MPAM feature page. MPAMF_MBW_IDR_rt indicates bandwidth partitioning features accessed from the Root MPAM feature page. MPAMF_MBW_IDR_rl indicates bandwidth partitioning features accessed from the Realm MPAM feature page.

When MPAMF_IDR.HAS_RIS is 1, some fields in this register give information for the resource instance selected by MPAMCFG_PART_SEL.RIS. The description of every field that is affected by MPAMCFG_PART_SEL.RIS has that information within the field description.

## Configuration

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_MBW_PART == 1. Otherwise, direct accesses to MPAMF_MBW_IDR are res0.

The power and reset domain of each MSC component is specific to that component.

## Attributes

MPAMF_MBW_IDR is a 32-bit register.

## Field descriptions

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES0 | | | BWPBM_WD | | | | | | | | | | | | | RES0 | WINDWR | HAS_PROP | HAS_PBM | HAS_MAX | HAS_MIN | RES0 | | | | | | | | BWA_W |

**Bits [31:29]**

Reserved, res0.

**BWPBM_WD, bits [28:16]**

Bandwidth portion bitmap width.

The number of bandwidth portion bits in the MPAMCFG_MBW_PBM<n> register array.

If MPAMF_MBW_IDR.HAS_PBM is 1, this field must contain a value from 1 to 4096, inclusive. Values greater than 32 require a group of 32-bit registers to access the BWPBM, up to 128 if BWPBM_WD is the largest value.

If MPAMF_MBW_IDR.HAS_PBM is 0, this field must be ignored by software.

If RIS is implemented, this field indicates the width of the memory bandwidth portion bitmap partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**Bit [15]**

Reserved, res0.

**WINDWR, bit [14]**

Indicates the bandwidth accounting period register is writable.

| WINDWR | Meaning |
|---|---|
| 0b0 | The bandwidth accounting period is readable from MPAMCFG_MBW_WINWD which might be fixed or vary due to clock rate reconfiguration of the memory channel or memory controller. |
| 0b1 | The bandwidth accounting width is readable and writable per partition in MPAMCFG_MBW_WINWD. |

**HAS_PROP, bit [13]**

Indicates that this MSC implements proportional stride bandwidth partitioning and the MPAMCFG_MBW_PROP register can be accessed.

| HAS_PROP | Meaning |
|---|---|

| | |
|---|---|
| 0b0 | There is no memory bandwidth proportional stride control and the MPAMCFG_MBW_PROP register is res0. |
| 0b1 | The proportional stride memory bandwidth partitioning scheme is supported and the MPAMCFG_MBW_PROP register can be accessed. |

If RIS is implemented, this field indicates the presence of the memory bandwidth proportional stride partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**HAS_PBM, bit [12]**

Indicates that bandwidth portion partitioning is implemented and the MPAMCFG_MBW_PBM<n> register array can be accessed.

| HAS_PBM | Meaning |
|---|---|
| 0b0 | There is no memory bandwidth portion control and the MPAMCFG_MBW_PBM<n> is res0. |
| 0b1 | The memory bandwidth portion allocation scheme exists and the MPAMCFG_MBW_PBM<n> register can be accessed. |

If RIS is implemented, this field indicates the presence of the memory bandwidth portion partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**HAS_MAX, bit [11]**

Indicates that this MSC implements maximum bandwidth partitioning and the MPAMCFG_MBW_MAX register can be accessed.

| HAS_MAX | Meaning |
|---|---|
| 0b0 | There is no maximum memory bandwidth control and the MPAMCFG_MBW_MAX register is res0. |

| | |
|---|---|
| 0b1 | The maximum memory bandwidth allocation scheme is supported and the MPAMCFG_MBW_MAX register can be accessed. |

If RIS is implemented, this field indicates the presence of the maximum bandwidth partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**HAS_MIN, bit [10]**

Indicates that this MSC implements minimum bandwidth partitioning and the MPAMCFG_MBW_MIN register can be accessed.

| HAS_MIN | Meaning |
|---|---|
| 0b0 | There is no minimum memory bandwidth control and the MPAMCFG_MBW_MIN register is res0. |
| 0b1 | The minimum memory bandwidth allocation scheme is supported and the MPAMCFG_MBW_MIN register can be accessed. |

If RIS is implemented, this field indicates the presence of the minimum bandwidth partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**Bits [9:6]**

Reserved, res0.

**BWA_WD, bits [5:0]**

Number of implemented bits in the bandwidth allocation fields: MIN, MAX, and STRIDE. See MPAMCFG_MBW_MIN, MPAMCFG_MBW_MAX, and MPAMCFG_MBW_PROP.

In any of these bandwidth allocation fields exist, this field must have a value from 1 to 16, inclusive. Otherwise, it is permitted to be 0.

If RIS is implemented, this field indicates the number of implemented bits in the bandwidth allocation control fields for the resource instance selected by MPAMCFG_PART_SEL.RIS.

## Accessing MPAMF_MBW_IDR

This register is within the MPAM feature page memory frames. In a system that supports Secure, Non-secure, Root, and Realm memory maps, there must be MPAM feature pages in all four address maps.

MPAMF_MBW_IDR is read-only.

MPAMF_MBW_IDR must be readable from the Non-secure, Secure, Root, and Realm MPAM feature pages.

MPAMF_MBW_IDR is permitted to have the same contents when read from the Secure, Non-secure, Root, and Realm MPAM feature pages unless the register contents are different for the different versions:

- MPAMF_MBW_IDR_s is permitted to have either the same or different contents to MPAMF_MBW_IDR_ns, MPAMF_MBW_IDR_rt, or MPAMF_MBW_IDR_rl.
- MPAMF_MBW_IDR_ns is permitted to have either the same or different contents to MPAMF_MBW_IDR_rt or MPAMF_MBW_IDR_rl.
- MPAMF_MBW_IDR_rt is permitted to have either the same or different contents to MPAMF_MBW_IDR_rl.

There must be separate registers in the Secure (MPAMF_MBW_IDR_s), Non-secure (MPAMF_MBW_IDR_ns), Root (MPAMF_MBW_IDR_rt), and Realm (MPAMF_MBW_IDR_rl) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_MBW_IDR shows the configuration of memory bandwidth partitioning for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

**MPAMF_MBW_IDR can be accessed through the memory-mapped interfaces:**

| Component | Frame | Offset | Instance |
|---|---|---|---|
| MPAM | MPAMF_BASE_s | 0x0040 | MPAMF_MBW_IDR_s |

Accesses on this interface are **RO**.

| Component | Frame | Offset | Instance |
|---|---|---|---|
| MPAM | MPAMF_BASE_ns | 0x0040 | MPAMF_MBW_IDR_ns |

Accesses on this interface are **RO**.

| Component | Frame | Offset | Instance |
|---|---|---|---|
| MPAM | MPAMF_BASE_rt | 0x0040 | MPAMF_MBW_IDR_rt |

When FEAT_RME is implemented, accesses on this interface are **RO**.

| Component | Frame | Offset | Instance |
|---|---|---|---|
| MPAM | MPAMF_BASE_rl | 0x0040 | MPAMF_MBW_IDR_rl |

When FEAT_RME is implemented, accesses on this interface are **RO**.

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