

TRCCNTRLDVR<n>, Counter Reload Value Register <n>, n = 0 - 3

The TRCCNTRLDVR<n> characteristics are:

Purpose

This sets or returns the reload count value for Counter <n>.

Configuration

External register TRCCNTRLDVR<n> bits [31:0] are architecturally mapped to AArch64 System register [TRCCNTRLDVR<n>\[31:0\]](#).

This register is present only when FEAT_ETE is implemented, FEAT_TRC_EXT is implemented and $\text{UInt}(\text{TRCIDR5.NUMCNTR}) > n$. Otherwise, direct accesses to TRCCNTRLDVR<n> are res0.

Attributes

TRCCNTRLDVR<n> is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																VALUE															

Bits [31:16]

Reserved, res0.

VALUE, bits [15:0]

Contains the reload value for Counter <n>. When a reload event occurs for Counter <n> then the trace unit copies the VALUE<n> field into Counter <n>.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Accessing TRCCNTRLDVR<n>

Must be programmed if [TRCRSCTLR<a>.GROUP == 0b0010](#) and [TRCRSCTLR<a>.COUNTERS\[n\] == 1](#).

Writes are constrained unpredictable if the trace unit is not in the Idle state.

TRCCNTRLDVR<n> can be accessed through the external debug interface:

Component	Offset	Instance
ETE	0x140 + (4 * n)	TRCCNTRLDVR<n>

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.