<u>Index by</u>	<u>Sh</u>
Encoding	Pseud

SIMD&FP **SME** Base **SVE Instructions Instructions Instructions Instructions**

SDOT (2-way, vectors)

Signed integer dot product

The signed integer dot product instruction computes the dot product of a group of two signed 16-bit integer values held in each 32-bit element of the first source vector multiplied by a group of two signed 16-bit integer values in the corresponding 32-bit element of the second source vector, and then destructively adds the widened dot product to the corresponding 32-bit element of the destination vector.

This instruction is unpredicated.

integer m = UInt(Zm);integer da = UInt(Zda);

SVE₂ (FEAT_SVE2p1)

```
31\ 30\ 29\ 28\ 27\ 26\ 25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0
0 1 0 0 0 1 0 0 0 0 0
                                      Zm
                                                1 1 0 0 1 0
                                                                        Zn
                                                                                      Zda
```

```
SDOT <Zda>.S, <Zn>.H, <Zm>.H
if !<u>HaveSME2() && !HaveSVE2p1()</u> then UNDEFINED;
constant integer esize = 32;
integer n = UInt(Zn);
```

Assembler Symbols

<zda></zda>	Is the name of the third source and destination scalable vector register, encoded in the "Zda" field.
<zn></zn>	Is the name of the first source scalable vector register, encoded in the "Zn" field.
<zm></zm>	Is the name of the second source scalable vector register, encoded in the "Zm" field.

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV esize;
bits(VL) operand1 = \underline{Z}[n, VL];
bits(VL) operand2 = \underline{Z}[m, VL];
bits(VL) operand3 = \mathbb{Z}[da, VL];
bits(VL) result;
for e = 0 to elements-1
     bits(esize) res = Elem[operand3, e, esize];
```

```
for i = 0 to 1
    integer element1 = SInt(Elem[operand1, 2 * e + i, esize DIV 2])
    integer element2 = SInt(Elem[operand2, 2 * e + i, esize DIV 2])
    res = res + element1 * element2;
    Elem[result, e, esize] = res;
Z[da, VL] = result;
```

Operational information

This instruction might be immediately preceded in program order by a MOVPRFX instruction. The MOVPRFX instruction must conform to all of the following requirements, otherwise the behavior of the MOVPRFX and this instruction is unpredictable:

- The MOVPRFX instruction must be unpredicated.
- The MOVPRFX instruction must specify the same destination register as this instruction.
- The destination register must not refer to architectural register state referenced by any other source operand register of this instruction.

BaseSIMD&FPSVESMEIndex byInstructionsInstructionsInstructionsInstructions

 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no_diffs_2023_09_RC2,\ sve\ v2023-06_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.

Sh Pseu