

## TRBPIDR4, Peripheral Identification Register 4

The TRBPIDR4 characteristics are:

### Purpose

Provides discovery information about the component.

For additional information, see the CoreSight Architecture Specification.

### Configuration

This register is present only when FEAT\_TRBE\_EXT is implemented. Otherwise, direct accesses to TRBPIDR4 are res0.

TRBPIDR4 is in the Core power domain.

### Attributes

TRBPIDR4 is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																SIZE				DES 2											

#### Bits [31:8]

Reserved, res0.

#### SIZE, bits [7:4]

Size of the component.

The distance from the start of the address space used by this component to the end of the component identification registers.

A value of 0b0000 means one of the following is true:

- The component uses a single 4KB block.
- The component uses an implementation defined number of 4KB blocks.

Any other value means the component occupies  $2^{\text{TRBPIDR4.SIZE}}$  4KB blocks.

Using this field to indicate the size of the component is deprecated. This field might not correctly indicate the size of the component. Arm recommends that software determine the size of the component from the Unique Component Identifier fields, and other implementation defined registers in the component.

Reads as 0b0000.

Access to this field is **RO**.

## DES\_2, bits [3:0]

Designer, JEP106 continuation code. This is the JEDEC-assigned JEP106 bank identifier for the designer of the component, minus 1. The code identifies the designer of the component, which might not be not the same as the implementer of the device containing the component. To obtain a number, or to see the assignment of these codes, contact JEDEC <http://www.jedec.org>.

### Note

For a component designed by Arm Limited, the JEP106 bank is 5, meaning this field has the value 0x4.

This field has an implementation defined value.

Access to this field is **RO**.

## Accessing TRBPIDR4

**TRBPIDR4 can be accessed through the external debug interface:**

Component	Offset	Instance
TRBE	0xFD0	TRBPIDR4

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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