GICM_SETSPI_SR, Set Secure SPI Pending Register

The GICM_SETSPI_SR characteristics are:

Purpose

Adds the pending state to a valid SPI.

A write to this register changes the state of an inactive SPI to pending, and the state of an active SPI to active and pending.

Configuration

This register is present only when GICM_TYPER.SR == 1. Otherwise, direct accesses to GICM_SETSPI_SR are res0.

When GICD_CTLR.DS==1, this register is WI.

Attributes

GICM_SETSPI_SR is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																			INTID												

Bits [31:13]

Reserved, res0.

INTID, bits [12:0]

This field is an alias of GICD_SETSPI_SR.

Accessing GICM_SETSPI_SR

Writes to this register have no effect if:

- The value is written by a Non-secure access.
- The value written specifies an invalid SPI.
- The SPI is already pending.

16-bit accesses to bits [15:0] of this register must be supported.

GICM_SETSPI_SR can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Distributor	MSI_base	0x0050	GICM_SETSPI_SR

This interface is accessible as follows:

- When GICD_CTLR.DS == 1, accesses to this register are **WI**.
- When GICD_CTLR.DS == 0 and an access is Secure, accesses to this register are **WO**.
- When GICD_CTLR.DS == 0 and an access is Non-secure, accesses to this register are **WI**.
- When GICD_CTLR.DS == 0, FEAT_RME is implemented and an access is Root, accesses to this register are **WO**.
- When GICD_CTLR.DS == 0, FEAT_RME is implemented and an access is Realm, accesses to this register are **WI**.

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