

## FMOV (immediate, unpredicated)

Move 8-bit floating-point immediate to vector elements (unpredicated)

Unconditionally broadcast the floating-point immediate into each element of the destination vector. This instruction is unpredicated.

This is an alias of [FDUP](#). This means:

- The encodings in this description are named to match the encodings of [FDUP](#).
- The description of [FDUP](#) gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1	size	1	1	1	0	0	1	1	1	0	imm8						Zd							

**FMOV** <Zd>.<T>, #<const>

is equivalent to

**FDUP** <Zd>.<T>, #<const>

and is always the preferred disassembly.

### Assembler Symbols

<Zd> Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T> Is the size specifier, encoded in "size":

size	<T>
00	RESERVED
01	H
10	S
11	D

<const> Is a floating-point immediate value expressible as  $\hat{A} \pm n \hat{A} \cdot 16 \hat{A} - 2^r$ , where n and r are integers such that  $16 \hat{A} \hat{\%} n \hat{\%} 31$  and  $-3 \hat{\%} r \hat{\%} 4$ , i.e. a normalized binary floating-point encoding with 1 sign bit, 3-bit exponent, and 4-bit fractional part, encoded in the "imm8" field.

Operation

The description of [FDUP](#) gives the operational pseudocode for this instruction.

[Base  
Instructions](#)

[SIMD&FP  
Instructions](#)

[SVE  
Instructions](#)

[SME  
Instructions](#)

[Index by  
Encoding](#)

[Sh  
Pseu](#)

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56  
Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This  
document is Non-Confidential.