

## TRCIMSPEC0, IMP DEF Register 0

The TRCIMSPEC0 characteristics are:

### Purpose

TRCIMSPEC0 shows the presence of any implementation defined features, and provides an interface to enable the features that are provided.

### Configuration

External register TRCIMSPEC0 bits [31:0] are architecturally mapped to AArch64 System register [TRCIMSPEC0\[31:0\]](#).

This register is present only when FEAT\_ETE is implemented and FEAT\_TRC\_EXT is implemented. Otherwise, direct accesses to TRCIMSPEC0 are res0.

### Attributes

TRCIMSPEC0 is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											RES0											EN		SUPPORT							

#### Bits [31:8]

Reserved, res0.

#### EN, bits [7:4]

When **TRCIMSPEC0.SUPPORT != 0b0000**:

Enable. Controls whether the implementation defined features are enabled.

EN	Meaning
0b0000	The implementation defined features are not enabled. The trace unit must behave as if the implementation defined features are not supported.
0b0001	The trace unit behavior is implementation defined.

0b0010	The trace unit behavior is implementation defined.
0b0011	The trace unit behavior is implementation defined.
0b0100	The trace unit behavior is implementation defined.
0b0101	The trace unit behavior is implementation defined.
0b0110	The trace unit behavior is implementation defined.
0b0111	The trace unit behavior is implementation defined.
0b1000	The trace unit behavior is implementation defined.
0b1001	The trace unit behavior is implementation defined.
0b1010	The trace unit behavior is implementation defined.
0b1011	The trace unit behavior is implementation defined.
0b1100	The trace unit behavior is implementation defined.
0b1101	The trace unit behavior is implementation defined.
0b1110	The trace unit behavior is implementation defined.
0b1111	The trace unit behavior is implementation defined.

---

The reset behavior of this field is:

- On a Trace unit reset, this field resets to 0.

#### Otherwise:

Reserved, res0.

#### **SUPPORT, bits [3:0]**

Indicates whether the implementation supports implementation defined features.

<b>SUPPORT</b>	<b>Meaning</b>
0b0000	No implementation defined features are supported.
0b0001	implementation defined features are supported.
0b0010	implementation defined features are supported.

0b0011	implementation defined features are supported.
0b0100	implementation defined features are supported.
0b0101	implementation defined features are supported.
0b0110	implementation defined features are supported.
0b0111	implementation defined features are supported.
0b1000	implementation defined features are supported.
0b1001	implementation defined features are supported.
0b1010	implementation defined features are supported.
0b1011	implementation defined features are supported.
0b1100	implementation defined features are supported.
0b1101	implementation defined features are supported.
0b1110	implementation defined features are supported.
0b1111	implementation defined features are supported.

---

Use of nonzero values requires written permission from Arm.

Access to this field is **RO**.

## Accessing TRCIMSPEC0

**TRCIMSPEC0 can be accessed through the external debug interface:**

Component	Offset	Instance
ETE	0x1C0	TRCIMSPEC0

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or !IsTraceCorePowered(), accesses to this register generate an error response.
  - Otherwise, accesses to this register are **RW**.
-

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.