# ACTLR_EL3, Auxiliary Control Register (EL3)

The ACTLR_EL3 characteristics are:

## Purpose

Provides implementation defined configuration and control options for EL3.

## Configuration

This register is present only when EL3 is implemented. Otherwise, direct accesses to ACTLR_EL3 are undefined.

## Attributes

ACTLR_EL3 is a 64-bit register.

## Field descriptions

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IMPLEMENTATION DEFINED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| IMPLEMENTATION DEFINED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

#### IMPLEMENTATION DEFINED, bits [63:0]

implementation defined.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

## Accessing ACTLR_EL3

Accesses to this register use the following encodings in the System register encoding space:

```
MRS <Xt>, ACTLR_EL3
```

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b110 | 0b0001 | 0b0000 | 0b001 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ACTLR_EL3;
```

## MSR ACTLR_EL3, <Xt>

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b110 | 0b0001 | 0b0000 | 0b001 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    ACTLR_EL3 = X[t, 64];
```

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