

PMZR_EL0, Performance Monitors Zero with Mask

The PMZR_EL0 characteristics are:

Purpose

Zero the set of counters specified by the mask written to PMZR_EL0.

Configuration

External register PMZR_EL0 bits [63:0] are architecturally mapped to AArch64 System register [PMZR_EL0\[63:0\]](#).

This register is present only when FEAT_PMUv3_EXT64 is implemented and FEAT_PMUv3p9 is implemented. Otherwise, direct accesses to PMZR_EL0 are res0.

PMZR_EL0 is in the Core power domain.

Attributes

PMZR_EL0 is a 64-bit register.

This register is part of the [PMU](#) block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
RES0																											
C	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4

Bits [63:33]

Reserved, res0.

F<m>, bit [m+32], for m = 0
When FEAT_PMUv3_ICNTR is implemented:

Zero fixed-function counter <m>.

F<m>	Meaning
0b0	Write is ignored.

0b1	Set fixed-function counter <m> to zero.
-----	---

Writing 1 to PMZR_EL0.F0 sets PMU.PMICNTR_EL0 to zero.

Otherwise:

Reserved, res0.

C, bit [31]

Zero PMU.PMCCNTR_EL0.

C	Meaning
0b0	Write is ignored.
0b1	Set PMU.PMCCNTR_EL0 to zero.

P<m>, bit [m], for m = 30 to 0

Zero [PMEVCNTR<m>_EL0](#).

P<m>	Meaning
0b0	Write is ignored.
0b1	Set PMEVCNTR<m>_EL0 to zero.

Accessing PMZR_EL0

Accesses to this register use the following encodings:

Accessible at offset 0xCA0 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **WI**.
- Otherwise, accesses to this register are **WO**.

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

