# VNCR_EL2, Virtual Nested Control Register

The VNCR_EL2 characteristics are:

## Purpose

When FEAT_NV2 is implemented, holds the base address that is used to define the memory location that is accessed by transformed reads and writes of System registers.

## Configuration

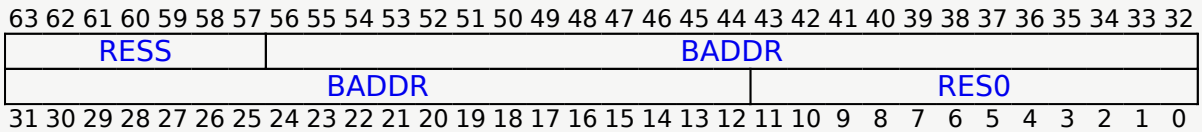
This register is present only when FEAT_NV2 is implemented. Otherwise, direct accesses to VNCR_EL2 are undefined.

This register has no effect if EL2 is not enabled in the current Security state.

## Attributes

VNCR_EL2 is a 64-bit register.

## Field descriptions




### RESS, bits [63:57]

Reserved, Sign extended. If the bits marked as RESS do not all have the same value, then there is a constrained unpredictable choice between:

- Generating an EL2 translation regime Translation abort on use of the VNCR_EL2 register. If FEAT_D128 is implemented:
- If the virtual address space for EL2 supports 56 bits, bits[63:57] of VNCR_EL2 are treated as the same value as bit[56] for all purposes other than reading back the register.
- If the virtual address space for EL2 supports 56 bits, bits[63:57] of VNCR_EL2 are treated as the same value as bit[56].
- If the virtual address space for EL2 supports 52 bits, bits[63:53] of VNCR_EL2 are treated as the same value as bit[52] for all purposes other than reading back the register.

- If the virtual address space for EL2 supports 52 bits, bits[63:53] of VNCR_EL2 are treated as the same value as bit[52].
- Bits[63:49] of VNCR_EL2 are treated as the same value as bit[48] for all purposes other than reading back the register.
- Bits[63:49] of VNCR_EL2 are treated as the same value as bit[48] for all purposes.

Where the EL2 translation regime has upper and lower address ranges, bit[56] is used to select between those address ranges to determine the number of bits supported by the address space.

**BADDR, bits [56:12]**

Base Address. If the virtual address space for EL2 does not support more than 48 bits, then bits [56:49] are RESS. If the virtual address space for EL2 does not support more than 52 bits, then bits [56:53] are RESS

When a register read/write is transformed to be a Load or Store, the address of the load/store is to SignOffset(VNCR_EL2.BADDR:Offset<11:0>, 64).

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

**Bits [11:0]**

Reserved, res0.

## Accessing VNCR_EL2

Accesses to this register use the following encodings in the System register encoding space:

### MRS <Xt>, VNCR_EL2

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b100 | 0b0010 | 0b0010 | 0b000 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        X[t, 64] = NVMem[0x0B0];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
```

```
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    X[t, 64] = VNCR_EL2;
elsif PSTATE.EL == EL3 then
    X[t, 64] = VNCR_EL2;
```

## MSR VNCR_EL2, <Xt>

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b100 | 0b0010 | 0b0010 | 0b000 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x0B0] = X[t, 64];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    VNCR_EL2 = X[t, 64];
elsif PSTATE.EL == EL3 then
    VNCR_EL2 = X[t, 64];
```



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