

UMINV

Unsigned minimum reduction to scalar

Unsigned minimum horizontally across all lanes of a vector, and place the result in the SIMD&FP scalar destination register. Inactive elements in the source vector are treated as the maximum unsigned integer for the element size.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	size	0	0	1	0	1	1	0	0	1	Pg													
U																															

UMINV <V><d>, <Pg>, <Zn>.<T>

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Vd);
boolean unsigned = TRUE;
```

Assembler Symbols

<V>

Is a width specifier, encoded in “size”:

size	<V>
00	B
01	H
10	S
11	D

<d>

Is the number [0-31] of the destination SIMD&FP register, encoded in the “Vd” field.

<Pg>

Is the name of the governing scalable predicate register P0-P7, encoded in the “Pg” field.

<Zn>

Is the name of the source scalable vector register, encoded in the “Zn” field.

<T>

Is the size specifier, encoded in “size”:

size	<T>
00	B
01	H
10	S
11	D

Operation

```
CheckSVEEnabled();  
constant integer VL = CurrentVL;  
constant integer PL = VL DIV 8;  
constant integer elements = VL DIV esize;  
bits(PL) mask = P[g, PL];  
bits(VL) operand = if AnyActiveElement(mask, esize) then Z[n, VL] else  
integer minimum = if unsigned then (2^esize - 1) else (2^(esize-1) - 1)  
  
for e = 0 to elements-1  
    if ActivePredicateElement(mask, e, esize) then  
        integer element = Int(Elem[operand, e, esize], unsigned);  
        minimum = Min(minimum, element);  
  
V[d, esize] = minimum<esize-1:0>;
```

Operational information

If FEAT_SVE2 is implemented or FEAT_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its operand registers when its governing predicate register contains the same value for each execution.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its operand registers when its governing predicate register contains the same value for each execution.
 - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode
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