

SPMSELR_EL0, System Performance Monitors Select Register

The SPMSELR_EL0 characteristics are:

Purpose

Selects the System PMU and event counter registers to access.

Configuration

This register is present only when FEAT_SPMU is implemented. Otherwise, direct accesses to SPMSELR_EL0 are undefined.

Attributes

SPMSELR_EL0 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
RES0																SYSPMUSEL				RES0		BANK									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:10]

Reserved, res0.

SYSPMUSEL, bits [9:4]

System PMU Select. Selects a System PMU <s> to access.

Values 0x20 to 0x3F are reserved.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [3:2]

Reserved, res0.

BANK, bits [1:0]

System PMU bank access control. Selects a bank of 16 System PMU event counters and related controls to access.

BANK	Meaning
0b00	Select event counters 0 to 15.
0b01	Select event counters 16 to 31.
0b10	Select event counters 32 to 47.
0b11	Select event counters 48 to 63.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing SPMSELR_ELO

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, SPMSELR_ELO

op0	op1	CRn	CRm	op2
0b10	0b011	0b1001	0b1100	0b101

```
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
    when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
    && IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
    SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
    && IsFeatureImplemented(FEAT_FGT2) &&
    HDFGRTR2_EL2.nSPMSELR_ELO == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = SPMSELR_ELO;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
    when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
```

```

        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nSPMSELR_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            X[t, 64] = SPMSELR_EL0;
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            else
                X[t, 64] = SPMSELR_EL0;
    elsif PSTATE.EL == EL3 then
        X[t, 64] = SPMSELR_EL0;

```

MSR SPMSELR_EL0, <Xt>

op0	op1	CRn	CRm	op2
0b10	0b011	0b1001	0b1100	0b101

```

if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nSPMSELR_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else

```

```

        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMSELR_EL0 = X[t, 64];
    elsif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
        && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
            UNDEFINED;
        elsif EL2Enabled() &&
        IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
        SCR_EL3.FGTEn2 == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() &&
        IsFeatureImplemented(FEAT_FGT2) &&
        HDFGWTR2_EL2.nSPMSELR_EL0 == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            SPMSELR_EL0 = X[t, 64];
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
        && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            SPMSELR_EL0 = X[t, 64];
    elsif PSTATE.EL == EL3 then
        SPMSELR_EL0 = X[t, 64];

```

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

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