TRBDEVID, Device Configuration Register

The TRBDEVID characteristics are:

Purpose

Provides discovery information for the component.

For additional information, see the CoreSight Architecture Specification.

Configuration

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBDEVID are res0.

TRBDEVID is in the Core power domain.

Attributes

TRBDEVID is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																												MPAM			

Bits [31:4]

Reserved, res0.

MPAM, bits [3:0]

MPAM extensions. Indicates support for Memory Partitioning and Monitoring (MPAM) and the Trace Buffer MPAM extensions.

MPAM	Meaning
0b0000	MPAM not implemented by Trace Buffer Unit.
0b0001	MPAM implemented by Trace Buffer Unit, using default PARTID and PMG values.
0b0010	Trace Buffer MPAM extensions implemented.

When FEAT_MPAM is not implemented by the PE, this field reads as `0b0000`.

When FEAT_MPAM is implemented by the PE, the value `0b0000` is not permitted.

FEAT_TRBE_MPAM implements the functionality identified by the value `0b0010`.

Accessing TRBDEVID

TRBDEVID can be accessed through the external debug interface:

Component	Offset	Instance
TRBE	`0xFC8`	TRBDEVID

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94