PMEVTYPER<n>_EL0, Performance Monitors Event Type Registers, n = 0 - 30

The PMEVTYPER<n>_EL0 characteristics are:

Purpose

Configures event counter <n>, where <n> is 0 to 30.

Configuration

External register PMEVTYPER<n>_EL0 bits [63:0] are architecturally mapped to AArch64 System register PMEVTYPER<n>_EL0[63:0].

External register PMEVTYPER<n>_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMEVTYPER<n>[31:0].

This register is present only when FEAT_PMUv3_EXT is implemented. Otherwise, direct accesses to PMEVTYPER<n>_EL0 are res0.

PMEVTYPER<n>_EL0 is in the Core power domain.

If event counter n is not implemented:

- When IsCorePowered() && !DoubleLockStatus() && ! OSLockStatus() && AllowExternalPMUAccess(), accesses are res0.
- Otherwise, it is constrained unpredictable whether accesses to this register are res0 or generate an error response.

Attributes

PMEVTYPER<n>_EL0 is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
TC			TE	RES0	SYNC	RES0																TH									
P	U	NSK	NSU	NSH	M	MT	SH	T	RLK	RLU	RLH	RES0				evtCount[15:10]						evtCount[9:0]									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

TC, bits [63:61]
When FEAT_PMUv3_EDGE is implemented and PMU.PMEVTYPER<n>_EL0.TE == 1:

Threshold Control.

Defines the threshold function. In the description of this field:

- V_B is the value the event specified by PMU.PMEVTYPER<n>_EL0 would increment the counter by on a processor cycle if the threshold function is disabled.
- TH is the value of PMEVTYPER<n>.TH.

Comparisons treat V_B and TH as unsigned integer values.

TC	Meaning
0b001	Equal to not-equal. The counter increments by 1 on each processor cycle when V_B is not equal to TH and V_B was equal to TH on the previous processor cycle.
0b010	Equal to/from not-equal. The counter increments by 1 on each processor cycle when either: • V_B is not equal to TH and V_B was equal to TH on the previous processor cycle. • V_B is equal to TH and V_B was not equal to TH on the previous processor cycle.
0b011	Not-equal to equal. The counter increments by 1 on each processor cycle when V_B is equal to TH and V_B was not equal to TH on the previous processor cycle.
0b101	Less-than to greater-than-or-equal. The counter increments by 1 on each processor cycle when V_B is greater than or equal to TH and V_B was less than TH on the previous processor cycle.

`0b110`	Less-than to/from greater-than-or-equal. The counter increments by 1 on each processor cycle when either: • V_B is greater than or equal to TH and V_B was less than TH on the previous processor cycle. • V_B is less than TH and V_B was greater than or equal to TH on the previous processor cycle.
`0b111`	Greater-than-or-equal to less-than. The counter increments by 1 on each processor cycle when V_B is less than TH and V_B was greater than or equal to TH on the previous processor cycle.

All other values are reserved.

The reset behavior of this field is:

- On a Warm reset:
  - When AArch32 is supported, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

When ((FEAT_PMUv3_EDGE is implemented and PMU.PMEVTYPER<n>_EL0.TE == 0) or FEAT_PMUv3_EDGE is not implemented) and FEAT_PMUv3_TH is implemented:

Threshold Control.

Defines the threshold function. In the description of this field:

- V_B is the value the event specified by PMU.PMEVTYPER<n>_EL0 would increment the counter by on a processor cycle if the threshold function is disabled.
- TH is the value of PMEVTYPER<n>.TH.

Comparisons treat V_B and TH as unsigned integer values.

TC	Meaning

0b000	Not-equal. The counter increments by V_B on each processor cycle when V_B is not equal to TH. If TH is zero, the threshold function is disabled.
0b001	Not-equal, count. The counter increments by 1 on each processor cycle when V_B is not equal to TH.
0b010	Equals. The counter increments by V_B on each processor cycle when V_B is equal to TH.
0b011	Equals, count. The counter increments by 1 on each processor cycle when V_B is equal to TH.
0b100	Greater-than-or-equal. The counter increments by V_B on each processor cycle when V_B is greater than or equal to TH.
0b101	Greater-than-or-equal, count. The counter increments by 1 on each processor cycle when V_B is greater than or equal to TH.
0b110	Less-than. The counter increments by V_B on each processor cycle when V_B is less than TH.
0b111	Less-than, count. The counter increments by 1 on each processor cycle when V_B is less than TH.

The reset behavior of this field is:

- On a Warm reset:
  - When AArch32 is supported, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Threshold Control.

Defines the threshold function. In the description of this field:

- V_B is the value the event specified by PMU.PMEVTYPER<n>_EL0 would increment the counter by on a processor cycle if the threshold function is disabled.
- TH is the value of PMEVTYPER<n>.TH.

Comparisons treat V_B and TH as unsigned integer values.

TE, bit [60]
When FEAT_PMUv3_EDGE is implemented:

Threshold Edge. Enables the edge condition. When PMEVTYPER<n>.TE is 1, the event counter increments on cycles when the result of the threshold condition changes. See PMEVTYPER<n>.TC for more information.

TE	Meaning
0b0	Threshold edge condition disabled.
0b1	Threshold edge condition enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [59]

Reserved, res0.

SYNC, bit [58]
When FEAT_SEBEP is implemented:

Synchronous Mode. Controls whether a PMU exception generated by the counter is synchronous or asynchronous.

SYNC	Meaning
0b0	Asynchronous PMU exception is enabled.
0b1	Synchronous PMU exception is enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [57:44]

Reserved, res0.

TH, bits [43:32]
When FEAT_PMUv3_TH is implemented:

Threshold value. Provides the unsigned value for the threshold function defined by PMEVTYPER<n>_EL0.TC.

If PMEVTYPER<n>_EL0.TC is `0b000` and PMEVTYPER<n>_EL0.TH is zero, then the threshold function is disabled.

If PMMIR_EL1.THWIDTH is less than 12, then bits PMEVTYPER<n>_EL0.TH[11:PMMIR_EL1.THWIDTH] are res0. This accounts for the behavior when writing a value greater-than-or-equal-to $2^{(\text{PMMIR\_EL1.THWIDTH})}$.

The reset behavior of this field is:

- On a Warm reset:
  - When AArch32 is supported, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

P, bit [31]

EL1 filtering. Controls counting events in EL1.

P	Meaning
`0b0`	This field has no effect on filtering of events.
`0b1`	Events in EL1 are not counted.

If Secure and Non-secure states are implemented, then counting events in Non-secure EL1 is further controlled by PMEVTYPER<n>_EL0.NSK.

If FEAT_RME is implemented, then counting events in Realm EL1 is further controlled by PMEVTYPER<n>_EL0.RLK.

If EL3 is implemented, then counting events in EL3 is further controlled by PMEVTYPER<n>_EL0.M.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

U, bit [30]

EL0 filtering. Controls counting events in EL0.

U	Meaning
0b0	This field has no effect on filtering of events.
0b1	Events in EL0 are not counted.

If Secure and Non-secure states are implemented, then counting events in Non-secure EL0 is further controlled by PMEVTYPER<n>_EL0.NSU.

If FEAT_RME is implemented, then counting events in Realm EL0 is further controlled by PMEVTYPER<n>_EL0.RLU.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

NSK, bit [29]
When EL3 is implemented:

Non-secure EL1 filtering. Controls counting events in Non-secure EL1. If PMEVTYPER<n>_EL0.NSK is not equal to PMEVTYPER<n>_EL0.P, then events in Non-secure EL1 are not counted. Otherwise, PMEVTYPER<n>_EL0.NSK has no effect on filtering of events in Non-secure EL1.

NSK	Meaning
0b0	When PMEVTYPER<n>_EL0.P == 0, this field has no effect on filtering of events. When PMEVTYPER<n>_EL0.P == 1, events in Non-secure EL1 are not counted.
0b1	When PMEVTYPER<n>_EL0.P == 0, events in Non-secure EL1 are not counted. When PMEVTYPER<n>_EL0.P == 1, this field has no effect on filtering of events.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

NSU, bit [28]
When EL3 is implemented:

Non-secure EL0 filtering. Controls counting events in Non-secure EL0. If PMEVTYPER<n>_EL0.NSU is not equal to PMEVTYPER<n>_EL0.U, then events in Non-secure EL0 are not counted. Otherwise, PMEVTYPER<n>_EL0.NSU has no effect on filtering of events in Non-secure EL0.

NSU	Meaning
0b0	When PMEVTYPER<n>_EL0.U == 0, this field has no effect on filtering of events. When PMEVTYPER<n>_EL0.U == 1, events in Non-secure EL0 are not counted.
0b1	When PMEVTYPER<n>_EL0.U == 0, events in Non-secure EL0 are not counted. When PMEVTYPER<n>_EL0.U == 1, this field has no effect on filtering of events.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

NSH, bit [27]
When EL2 is implemented:

EL2 filtering. Controls counting events in EL2.

NSH	Meaning
0b0	Events in EL2 are not counted.

0b1	This field has no effect on filtering of events.

If EL3 is implemented and FEAT_SEL2 is implemented, then counting events in Secure EL2 is further controlled by PMEVTYPER<n>_EL0.SH.

If FEAT_RME is implemented, then counting events in Realm EL2 is further controlled by PMEVTYPER<n>_EL0.RLH.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

M, bit [26]
When EL3 is implemented:

EL3 filtering. Controls counting events in EL3. If PMEVTYPER<n>_EL0.M is not equal to PMEVTYPER<n>_EL0.P, then events in EL3 are not counted. Otherwise, PMEVTYPER<n>_EL0.M has no effect on filtering of events in EL3.

M	Meaning
0b0	When PMEVTYPER<n>_EL0.P == 0, this field has no effect on filtering of events. When PMEVTYPER<n>_EL0.P == 1, events in EL3 are not counted.
0b1	When PMEVTYPER<n>_EL0.P == 0, events in EL3 are not counted. When PMEVTYPER<n>_EL0.P == 1, this field has no effect on filtering of events.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

MT, bit [25]
When (FEAT_MTPMU is implemented and enabled) or an IMPLEMENTATION DEFINED multi-threaded PMU Extension is implemented:

Multithreading.

MT	Meaning
0b0	Count events only on controlling PE.
0b1	Count events from any PE with the same affinity at level 1 and above as this PE.

Note

- When the lowest level of affinity consists of logical PEs that are implemented using a multi-threading type approach, an implementation is described as multi-threaded. That is, the performance of PEs at the lowest affinity level is highly interdependent.
- Events from a different thread of a multithreaded implementation are not Attributable to the thread counting the event.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

SH, bit [24]
When EL3 is implemented and FEAT_SEL2 is implemented:

Secure EL2 filtering. Controls counting events in Secure EL2. If PMEVTYPER<n>_EL0.SH is equal to PMEVTYPER<n>_EL0.NSH, then events in Secure EL2 are not counted. Otherwise, PMEVTYPER<n>_EL0.SH has no effect on filtering of events in Secure EL2.

SH	Meaning

0b0	When PMEVTYPER<n>_EL0.NSH == 0, events in Secure EL2 are not counted. When PMEVTYPER<n>_EL0.NSH == 1, this field has no effect on filtering of events.
0b1	When PMEVTYPER<n>_EL0.NSH == 0, this field has no effect on filtering of events. When PMEVTYPER<n>_EL0.NSH == 1, events in Secure EL2 are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When !IsSecureEL2Enabled(), access to this field is **RES0**.
- Otherwise, access to this field is **RW**.

Otherwise:

Reserved, res0.

T, bit [23]
When FEAT_TME is implemented:

Transactional state filtering bit. Controls counting of Attributable events in Non-transactional state.

T	Meaning
0b0	This bit has no effect on the filtering of events.
0b1	Do not count Attributable events in Non-transactional state.

For each Unattributable event, it is implementation defined whether the filtering applies.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

RLK, bit [22]
When FEAT_RME is implemented:

Realm EL1 (kernel) filtering bit. Controls counting in Realm EL1.

If the value of this bit is equal to the value of the PMEVTYPER<n>_EL0.P bit, events in Realm EL1 are counted.

Otherwise, events in Realm EL1 are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

RLU, bit [21]
When FEAT_RME is implemented:

Realm EL0 (unprivileged) filtering bit. Controls counting in Realm EL0.

If the value of this bit is equal to the value of the PMEVTYPER<n>_EL0.U bit, events in Realm EL0 are counted.

Otherwise, events in Realm EL0 are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

RLH, bit [20]
When FEAT_RME is implemented:

Realm EL2 filtering bit. Controls counting in Realm EL2.

If the value of this bit is not equal to the value of the PMEVTYPER<n>_EL0.NSH bit, events in Realm EL2 are counted.

Otherwise, events in Realm EL2 are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [19:16]

Reserved, res0.

evtCount[15:10], bits [15:10]
When FEAT_PMUv3p1 is implemented:

Extension to evtCount[9:0]. For more information, see evtCount[9:0].

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

evtCount[9:0], bits [9:0]

Event to count. The event number of the event that is counted by event counter PMU.PMEVCNTR<n>_EL0.

Software must program this field with an event that is supported by the PE being programmed.

The ranges of event numbers allocated to each type of event are shown in 'Allocation of the PMU event number space'.

If FEAT_PMUv3p8 is implemented and PMEVTYPER<n>_EL0.evtCount is programmed to an event that is reserved or not supported by the PE, no events are counted and the value returned by a direct or external read of the PMEVTYPER<n>_EL0.evtCount field is the value written to the field.

Note

Arm recommends this behavior for all implementations of FEAT_PMUv3.

Otherwise, if PMEVTYPER<n>_EL0.evtCount is programmed to an event that is reserved or not supported by the PE, the behavior depends on the value written:

- For the range `0x0000` to `0x003F`, no events are counted and the value returned by a direct or external read of the PMEVTYPER<n>_EL0.evtCount field is the value written to the field.
- If FEAT_PMUv3p1 is implemented, for the range `0x4000` to `0x403F`, no events are counted and the value returned by a direct or external read of the PMEVTYPER<n>_EL0.evtCount field is the value written to the field.
- For other values, it is unpredictable what event, if any, is counted, and the value returned by a direct or external read of the PMEVTYPER<n>_EL0.evtCount field is unknown.

Note

unpredictable means the event must not expose privileged information.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMEVTYPER<n>_EL0

If FEAT_PMUv3_EXT32 is implemented, and at least one of FEAT_PMUv3_TH or FEAT_PMUv3p8 is implemented, then bits [63:32] of this interface are accessible at offset `0xA00` + (4*n). Otherwise accesses at this offset are implementation defined.

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT64 is implemented

[63:0] Accessible at offset 0x400 + (8 * n) from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

When FEAT_PMUv3_EXT32 is implemented

[31:0] Accessible at offset 0x400 + (4 * n) from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

When FEAT_PMUv3_EXT32 is implemented and (FEAT_PMUv3_TH is implemented or FEAT_PMUv3p8 is implemented)

[63:32] Accessible at offset 0xA00 + (4 * n) from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

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