CTIDEVCTL, CTI Device Control register

The CTIDEVCTL characteristics are:

Purpose

Provides target-specific device controls

Configuration

CTIDEVCTL is in the Debug power domain.

This register is present only when FEAT_DoPD is implemented. Otherwise, direct accesses to CTIDEVCTL are res0.

Attributes

CTIDEVCTL is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																														RCE	OSUCE

Bits [31:2]

Reserved, res0.

RCE, bit [1]

Reset Catch Enable.

RCE	Meaning
0b0	Reset Catch debug event disabled.
0b1	Reset Catch debug event enabled.

The reset behavior of this field is:

- On an External debug reset, this field resets to 0.

OSUCE, bit [0]

OS Unlock Catch Enable

OSUCE	Meaning

0b0	OS Unlock Catch debug event disabled.
0b1	OS Unlock Catch debug event enabled.

The reset behavior of this field is:

- On an External debug reset, this field resets to 0.

Accessing CTIDEVCTL

CTIDEVCTL can be accessed through the external debug interface:

Component	Offset	Instance
CTI	0x150	CTIDEVCTL

This interface is accessible as follows:

- When SoftwareLockStatus(), accesses to this register are **RO**.
- When !SoftwareLockStatus(), accesses to this register are **RW**.

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