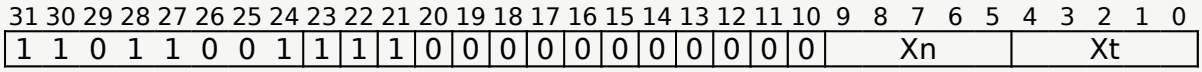
LDGM

Load Tag Multiple reads a naturally aligned block of N Allocation Tags, where the size of N is identified in GMID_EL1.BS, and writes the Allocation Tag read from address A to the destination register at 4*A<7:4>+3:4*A<7:4>. Bits of the destination register not written with an Allocation Tag are set to 0.

This instruction is undefined at EL0.

This instruction generates an Unchecked access.

Integer
(FEAT_MTE2)



LDGM <Xt>, [<Xn|SP>]

```
if !IsFeatureImplemented(FEAT_MTE2) then UNDEFINED;
integer t = UInt(Xt);
integer n = UInt(Xn);
```

Assembler Symbols

<Xt>	Is the 64-bit name of the general-purpose destination register, encoded in the "Xt" field.
<Xn|SP>	Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Xn" field.

Operation

```
if PSTATE.EL == EL0 then
    UNDEFINED;

bits(64) data = Zeros(64);
bits(64) address;

if n == 31 then
    CheckSPAlignment();
    address = SP[];
else
    address = X[n, 64];

integer size = 4 * (2 ^ (UInt(GMID_EL1.BS)));
address = Align(address, size);
constant integer count = size >> LOG2_TAG_GRANULE;
integer index = UInt(address<LOG2_TAG_GRANULE+3:LOG2_TAG_GRANULE>);
AccessDescriptor accdesc = CreateAccDescLDGSTG(MemOp_LOAD);

for i = 0 to count-1
```

```
    bits(4) tag = AArch64.MemTag[address, accdesc];
    Elem[data, index, 4] = tag;
    address = address + TAG_GRANULE;
    index = index + 1;

X[t, 64] = data;
```

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56