

TRCVMIDCCTLR1, Virtual Context Identifier Comparator Control Register 1

The TRCVMIDCCTLR1 characteristics are:

Purpose

Virtual Context Identifier Comparator mask values for the [TRCVMIDCVR<n>](#) registers, where n=4-7.

Configuration

External register TRCVMIDCCTLR1 bits [31:0] are architecturally mapped to AArch64 System register [TRCVMIDCCTLR1\[31:0\]](#).

This register is present only when FEAT_ETE is implemented, FEAT_TRC_EXT is implemented, $\text{UInt}(\text{TRCIDR4.NUMVMIDC}) > 0x4$ and $\text{UInt}(\text{TRCIDR2.VMIDSIZE}) > 0$. Otherwise, direct accesses to TRCVMIDCCTLR1 are res0.

Attributes

TRCVMIDCCTLR1 is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22
COMP7[7]	COMP7[6]	COMP7[5]	COMP7[4]	COMP7[3]	COMP7[2]	COMP7[1]	COMP7[0]	COMP6[7]	COMP6[6]

COMP7[<m>], bit [m+24], for m = 7 to 0
When $\text{UInt}(\text{TRCIDR4.NUMVMIDC}) > 7$:

TRCVMIDCVR7 mask control. Specifies the mask value that the trace unit applies to TRCVMIDCVR7. Each bit in this field corresponds to a byte in TRCVMIDCVR7.

COMP7[<m>]	Meaning
0b0	The trace unit includes TRCVMIDCVR7[(m \hat{A} —8+7):(m \hat{A} —8)] when it performs the Virtual context identifier comparison.

0b1	The trace unit ignores TRCVMIDCVR7[(m \tilde{A} —8+7):(m \tilde{A} —8)] when it performs the Virtual context identifier comparison.
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This bit is res0 if m \geq [TRCIDR2.VMIDSIZE](#).

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

COMP6[<m>], bit [m+16], for m = 7 to 0
When UInt(TRCIDR4.NUMVMIDC) > 6:

TRCVMIDCVR6 mask control. Specifies the mask value that the trace unit applies to TRCVMIDCVR6. Each bit in this field corresponds to a byte in TRCVMIDCVR6.

COMP6[<m>]	Meaning
0b0	The trace unit includes TRCVMIDCVR6[(m \tilde{A} —8+7):(m \tilde{A} —8)] when it performs the Virtual context identifier comparison.
0b1	The trace unit ignores TRCVMIDCVR6[(m \tilde{A} —8+7):(m \tilde{A} —8)] when it performs the Virtual context identifier comparison.

This bit is res0 if m \geq [TRCIDR2.VMIDSIZE](#).

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

COMP5[<m>], bit [m+8], for m = 7 to 0**When UInt(TRCIDR4.NUMVMIDC) > 5:**

TRCVMIDCVR5 mask control. Specifies the mask value that the trace unit applies to TRCVMIDCVR5. Each bit in this field corresponds to a byte in TRCVMIDCVR5.

COMP5[<m>]	Meaning
0b0	The trace unit includes TRCVMIDCVR5[(m—8+7):(m—8)] when it performs the Virtual context identifier comparison.
0b1	The trace unit ignores TRCVMIDCVR5[(m—8+7):(m—8)] when it performs the Virtual context identifier comparison.

This bit is res0 if m >= [TRCIDR2.VMIDSIZE](#).

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

COMP4[<m>], bit [m], for m = 7 to 0**When UInt(TRCIDR4.NUMVMIDC) > 4:**

TRCVMIDCVR4 mask control. Specifies the mask value that the trace unit applies to TRCVMIDCVR4. Each bit in this field corresponds to a byte in TRCVMIDCVR4.

COMP4[<m>]	Meaning
0b0	The trace unit includes TRCVMIDCVR4[(m—8+7):(m—8)] when it performs the Virtual context identifier comparison.

0b1

The trace unit ignores TRCVMIDCVR4[(m \hat{A} —8+7):(m \hat{A} —8)] when it performs the Virtual context identifier comparison.

This bit is res0 if m \geq [TRCIDR2](#).VMIDSIZE.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Accessing TRCVMIDCCTL1

If software uses the [TRCVMIDCVR<n>](#) registers, where n=4-7, then it must program this register.

If software sets a mask bit to 1 then it must program the relevant byte in [TRCVMIDCVR<n>](#) to 0x00.

If any bit is 1 and the relevant byte in [TRCVMIDCVR<n>](#) is not 0x00, the behavior of the Virtual Context Identifier Comparator is constrained unpredictable. In this scenario the comparator might match unexpectedly or might not match.

Writes are constrained unpredictable if the trace unit is not in the Idle state.

TRCVMIDCCTL1 can be accessed through the external debug interface:

Component	Offset	Instance
ETE	0x68C	TRCVMIDCCTL1

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or !IsTraceCorePowered(), accesses to this register generate an error response.
 - Otherwise, accesses to this register are **RW**.
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