

STSMAXH, STSMAXLH

Atomic signed maximum on halfword in memory, without return, atomically loads a 16-bit halfword from memory, compares it against the value held in a register, and stores the larger value back to memory, treating the values as signed numbers.

- STSMAXH does not have release semantics.
- STSMAXLH stores to memory with release semantics, as described in [Load-Acquire, Store-Release](#).

For information about memory accesses, see [Load/Store addressing modes](#).

This is an alias of [LDSDMAXH](#), [LDSDMAXAH](#), [LDSDMAXALH](#), [LDSDMAXLH](#). This means:

- The encodings in this description are named to match the encodings of [LDSDMAXH](#), [LDSDMAXAH](#), [LDSDMAXALH](#), [LDSDMAXLH](#).
- The description of [LDSDMAXH](#), [LDSDMAXAH](#), [LDSDMAXALH](#), [LDSDMAXLH](#) gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

Integer (FEAT_LSE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	0	0	0	0	R	1			Rs			0	1	0	0	0	0			Rn			1	1	1	1	1
size				A								opc												Rt							

No memory ordering (R == 0)

STSMAXH <Ws>, [[Xn](#) | SP]

is equivalent to

[LDSDMAXH](#) <Ws>, WZR, [[Xn](#) | SP]

and is always the preferred disassembly.

Release (R == 1)

STSMAXLH <Ws>, [[Xn](#) | SP]

is equivalent to

[LDSDMAXLH](#) <Ws>, WZR, [[Xn](#) | SP]

and is always the preferred disassembly.

Assembler Symbols

- <Ws> Is the 32-bit name of the general-purpose register holding the data value to be operated on with the contents of the memory location, encoded in the "Rs" field.
- <Xn|SP> Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field.

Operation

The description of [LDSMAXH](#), [LDSMAXAH](#), [LDSMAXALH](#), [LDSMAXLH](#) gives the operational pseudocode for this instruction.

Operational information

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

Base Instructions	SIMD&FP Instructions	SVE Instructions	SME Instructions	Index by Encoding
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[Sh](#)
[Pseu](#)

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56
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