RCWCAS, RCWCASA, RCWCASL, RCWCASAL

Read Check Write Compare and Swap doubleword in memory reads a 64-bit doubleword from memory, and compares it against the value held in a register. If the comparison is equal, the value in a second register is conditionally written to memory. Storing back to memory is conditional on RCW Checks. If the write is performed, the read and the write occur atomically such that no other modification of the memory location can take place between the read and the write. This instruction updates the condition flags based on the result of the update of memory.

- `RCWCASA` and `RCWCASAL` load from memory with acquire semantics.
- `RCWCASL` and `RCWCASAL` store to memory with release semantics.
- `RCWCAS` has neither acquire nor release semantics.

Integer
(FEAT_THE)

31	30	29	28	27	26	25	24	23	22	21	20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5	4 3 2 1 0
0	0	0	1	1	0	0	1	A	R	1	Rs	0 0 0 0 1 0	Rn	Rt
	S													

RCWCAS (A == 0 && R == 0)

```
RCWCAS <Xs>, <Xt>, [<Xn|SP>]
```

RCWCASA (A == 1 && R == 0)

```
RCWCASA <Xs>, <Xt>, [<Xn|SP>]
```

RCWCASAL (A == 1 && R == 1)

```
RCWCASAL <Xs>, <Xt>, [<Xn|SP>]
```

RCWCASL (A == 0 && R == 1)

```
RCWCASL <Xs>, <Xt>, [<Xn|SP>]
```

```
if !IsFeatureImplemented(FEAT_THE) then UNDEFINED;
integer t = UInt(Rt);
integer n = UInt(Rn);
integer s = UInt(Rs);

boolean acquire = A == '1';
boolean release = R == '1';
boolean tagchecked = n != 31;
```

Assembler Symbols

<Xs>	Is the 64-bit name of the general-purpose register to be compared and loaded, encoded in the "Rs" field.
<Xt>	Is the 64-bit name of the general-purpose register to be conditionally stored, encoded in the "Rt" field.
<Xn|SP>	Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field.

Operation

```
if IsD128Enabled(PSTATE.EL) then UNDEFINED;
bits(64) address;
bits(64) newdata = X[t, 64];
bits(64) compdata = X[s, 64];
bits(64) readdata;
bits(4) nzcv;

AccessDescriptor accdesc = CreateAccDescRCW(MemAtomicOp_CAS, FALSE, acq

if n == 31 then
    CheckSPAlignment();
    address = SP[];
else
    address = X[n, 64];

(nzcv, readdata) = MemAtomicRCW(address, compdata, newdata, accdesc);

PSTATE.<N,Z,C,V> = nzcv;
X[s, 64] = readdata;    // Return the old value when s!=31
```

Operational information

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

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