

BFC

Bitfield Clear sets a bitfield of $\langle\text{width}\rangle$ bits at bit position $\langle\text{lsb}\rangle$ of the destination register to zero, leaving the other destination bits unchanged.

This is an alias of [BFM](#). This means:

- The encodings in this description are named to match the encodings of [BFM](#).
- The description of [BFM](#) gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

Leaving other bits unchanged (FEAT_ASMv8p2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
sf	0	1	1	0	0	1	1	0	N	immr					imms					1	1	1	1	1	Rd						
opc										Rn																					

32-bit (sf == 0 && N == 0)

BFC $\langle\text{Wd}\rangle$, $\# \langle\text{lsb}\rangle$, $\# \langle\text{width}\rangle$

is equivalent to

[BFM](#) $\langle\text{Wd}\rangle$, WZR, $\#(-\langle\text{lsb}\rangle \text{ MOD } 32)$, $\#(\langle\text{width}\rangle-1)$

and is the preferred disassembly when $\text{UInt}(\text{imms}) < \text{UInt}(\text{immr})$.

64-bit (sf == 1 && N == 1)

BFC $\langle\text{Xd}\rangle$, $\# \langle\text{lsb}\rangle$, $\# \langle\text{width}\rangle$

is equivalent to

[BFM](#) $\langle\text{Xd}\rangle$, XZR, $\#(-\langle\text{lsb}\rangle \text{ MOD } 64)$, $\#(\langle\text{width}\rangle-1)$

and is the preferred disassembly when $\text{UInt}(\text{imms}) < \text{UInt}(\text{immr})$.

Assembler Symbols

$\langle\text{Wd}\rangle$	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.
$\langle\text{Xd}\rangle$	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.
$\langle\text{lsb}\rangle$	For the 32-bit variant: is the bit number of the lsb of the destination bitfield, in the range 0 to 31.

For the 64-bit variant: is the bit number of the lsb of the destination bitfield, in the range 0 to 63.

<width> For the 32-bit variant: is the width of the bitfield, in the range 1 to 32-<lsb>.

For the 64-bit variant: is the width of the bitfield, in the range 1 to 64-<lsb>.

Operation

The description of [BFM](#) gives the operational pseudocode for this instruction.

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56

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