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External Registers

ERRERICRO, Error Recovery Interrupt Configuration Register 0

The ERRERICRO characteristics are:

Purpose

Error Recovery Interrupt configuration register.

Configuration

This register is present only when (the Error Recovery Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRERICRO are res0.

ERRERICRO is implemented only as part of a memory-mapped group of error records.

Attributes

ERRERICRO is a 64-bit register.

Field descriptions

When the Error Recovery Interrupt is implemented, the implementation uses the recommended layout for the ERRIRQCR registers and the implementation uses simple interrupts:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

RES0
RES0

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits [63:0]

Reserved, res0.

When the implementation uses message-signaled interrupts, the Error Recovery Interrupt is implemented and the implementation uses the recommended layout for the **ERRIRQCR** registers:

63 62 61 60 59 58 57 56	55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

RES0	ADDR									
	ADDR								RE	S 0
21 20 20 20 27 26 25 24	22 22 21 20 10 10 17 16 15 14 12 12 11 10 0		7		ᆫ	1	$\overline{}$	$\overline{}$	1	$\overline{}$

Bits [63:56]

Reserved, res0.

ADDR, bits [55:2]

Message Signaled Interrupt address. (ERRERICRO.ADDR << 2) is the address that the component writes to when signaling the Error Recovery Interrupt. Bits [1:0] of the address are always zero.

The physical address size supported by the component is implementation defined. Unimplemented high-order physical address bits are res0.

The reset behavior of this field is:

• On an Error recovery reset, this field resets to an architecturally unknown value.

Bits [1:0]

Reserved, res0.

When the implementation does not use the recommended layout for the ERRIRQCR registers:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

05 02 01 00 55 50 57 50 55 51 55 52 51 50 15 10 17 10 15 11 15 12 11 10 55 50 57 50 55 51 55 52									
IMPLEMENTATION DEFINED									
IMPLEMENTATION DEFINED									
II II ZZI IZIVI VITORI ZZI INIZZ									
IMPLEMENTATION DEFINED									
IMPLEMENTATION DEFINED									

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

IMPLEMENTATION DEFINED, bits [63:0]

implementation defined.

Accessing ERRERICRO

If the implementation does not use the recommended layout for the ERRIRQCR registers then accesses to ERRERICRO are implementation defined.

ERRERICRO can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
RAS	0xE90	ERRERICR0

This interface is accessible as follows:

- When the implementation uses message-signaled interrupts, (an
 access is Non-secure or an access is Realm), the implementation
 uses the recommended layout for the ERRIRQCR registers and
 ERRERICR2.NSMSI configures the physical address space for
 message-signaled interrupts as Secure, accesses to this register are
 RO.
- Otherwise, accesses to this register are **RW**.

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