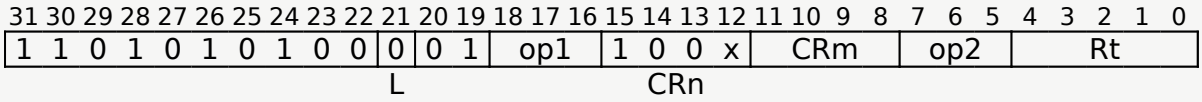
TLBI

TLB Invalidate operation. For more information, see *op0==0b01, cache maintenance, TLB maintenance, and address translation instructions*.

This is an alias of SYS. This means:

- The encodings in this description are named to match the encodings of SYS.
- The description of SYS gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.




```
TLBI <tlbi_op>{, <Xt>}
```

is equivalent to

```
SYS #<op1>, <Cn>, <Cm>, #<op2>{, <Xt>}
```

and is the preferred disassembly when `SysOp(op1,CRn,CRm,op2) == Sys_TLBI`.

Assembler Symbols

<op1>	Is a 3-bit unsigned immediate, in the range 0 to 7, encoded in the "op1" field.
<Cn>	Is a name 'Cn', with 'n' in the range 0 to 15, encoded in the "CRn" field.
<Cm>	Is a name 'Cm', with 'm' in the range 0 to 15, encoded in the "CRm" field.
<op2>	Is a 3-bit unsigned immediate, in the range 0 to 7, encoded in the "op2" field.

<tlbi_op>

Is a TLBI instruction name, as listed for the TLBI system instructio
group, encoded in “op1:CRn:CRm:op2”:

op1	CRn	CRm	op2	<tlbi_op>	Architectura Feature
000	1000	0001	000	VMALLE1OS	FEAT_TLBIOS
000	1000	0001	001	VAE1OS	FEAT_TLBIOS
000	1000	0001	010	ASIDE1OS	FEAT_TLBIOS
000	1000	0001	011	VAAE1OS	FEAT_TLBIOS
000	1000	0001	101	VALE1OS	FEAT_TLBIOS
000	1000	0001	111	VAALE1OS	FEAT_TLBIOS
000	1000	0010	001	RVAE1IS	FEAT_TLBIRAN
000	1000	0010	011	RVAAE1IS	FEAT_TLBIRAN
000	1000	0010	101	RVALE1IS	FEAT_TLBIRAN
000	1000	0010	111	RVAALE1IS	FEAT_TLBIRAN
000	1000	0011	000	VMALLE1IS	–
000	1000	0011	001	VAE1IS	–
000	1000	0011	010	ASIDE1IS	–
000	1000	0011	011	VAAE1IS	–
000	1000	0011	101	VALE1IS	–
000	1000	0011	111	VAALE1IS	–
000	1000	0101	001	RVAE1OS	FEAT_TLBIRAN
000	1000	0101	011	RVAAE1OS	FEAT_TLBIRAN
000	1000	0101	101	RVALE1OS	FEAT_TLBIRAN
000	1000	0101	111	RVAALE1OS	FEAT_TLBIRAN
000	1000	0110	001	RVAE1	FEAT_TLBIRAN
000	1000	0110	011	RVAAE1	FEAT_TLBIRAN
000	1000	0110	101	RVALE1	FEAT_TLBIRAN
000	1000	0110	111	RVAALE1	FEAT_TLBIRAN
000	1000	0111	000	VMALLE1	–
000	1000	0111	001	VAE1	–
000	1000	0111	010	ASIDE1	–
000	1000	0111	011	VAAE1	–
000	1000	0111	101	VALE1	–
000	1000	0111	111	VAALE1	–
000	1001	0001	000	VMALLE1OSNXS	FEAT_XS
000	1001	0001	001	VAE1OSNXS	FEAT_XS
000	1001	0001	010	ASIDE1OSNXS	FEAT_XS
000	1001	0001	011	VAAE1OSNXS	FEAT_XS
000	1001	0001	101	VALE1OSNXS	FEAT_XS
000	1001	0001	111	VAALE1OSNXS	FEAT_XS
000	1001	0010	001	RVAE1ISNXS	FEAT_XS
000	1001	0010	011	RVAAE1ISNXS	FEAT_XS
000	1001	0010	101	RVALE1ISNXS	FEAT_XS
000	1001	0010	111	RVAALE1ISNXS	FEAT_XS
000	1001	0011	000	VMALLE1ISNXS	FEAT_XS
000	1001	0011	001	VAE1ISNXS	FEAT_XS
000	1001	0011	010	ASIDE1ISNXS	FEAT_XS
000	1001	0011	011	VAAE1ISNXS	FEAT_XS
000	1001	0011	101	VALE1ISNXS	FEAT_XS
000	1001	0011	111	VAALE1ISNXS	FEAT_XS
000	1001	0101	001	RVAE1OSNXS	FEAT_XS
000	1001	0101	011	RVAAE1OSNXS	FEAT_XS
000	1001	0101	101	RVALE1OSNXS	FEAT_XS
000	1001	0101	111	RVAALE1OSNXS	FEAT_XS
000	1001	0110	001	RVAE1NXS	FEAT_XS
000	1001	0110	011	RVAAE1NXS	FEAT_XS

<Xt>	Is the 64-bit name of the optional general-purpose source register, defaulting to '11111', encoded in the "Rt" field.

Operation

The description of SYS gives the operational pseudocode for this instruction.

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56