# CNTPCT, Counter-timer Physical Count

The CNTPCT characteristics are:

## Purpose

Holds the 64-bit physical count value.

## Configuration

It is implementation defined whether CNTPCT is implemented in the Core power domain or in the Debug power domain.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

## Attributes

CNTPCT is a 64-bit register.

## Field descriptions

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Physical count value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Physical count value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:0]**

Physical count value.

The reset behavior of this field is:

- On a Timer reset, this field resets to an architecturally unknown value.

## Accessing CNTPCT

CNTPCT can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame, as a RO register.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.

- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- CNTPCT is accessible in that frame, as a RO register, if the value of CNTACR<n>.RPCT is 1.
- Otherwise, the CNTPCT address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTPCT is accessible in that frame if both:
  - CNTPCT is accessible in the corresponding CNTBaseN frame.
  - The value of CNTEL0ACR.EL0PCTEN is 1.
- Otherwise, the CNTPCT address in that frame is RAZ/WI.

If the implementation supports 64-bit atomic accesses, then the CNTPCT register must be accessible as an atomic 64-bit value.

**CNTPCT can be accessed through the memory-mapped interfaces:**

| Component | Frame | Offset | Instance | Range |
|---|---|---|---|---|
| Timer | CNTBaseN | 0x000 | CNTPCT | 31:0 |

Accesses on this interface are **RO**.

| Component | Frame | Offset | Instance | Range |
|---|---|---|---|---|
| Timer | CNTBaseN | 0x004 | CNTPCT | 63:32 |

Accesses on this interface are **RO**.

| Component | Frame | Offset | Instance | Range |
|---|---|---|---|---|
| Timer | CNTEL0BaseN | 0x000 | CNTPCT | 31:0 |

Accesses on this interface are **RO**.

| Component | Frame | Offset | Instance | Range |
|---|---|---|---|---|
| Timer | CNTEL0BaseN | 0x004 | CNTPCT | 63:32 |

Accesses on this interface are **RO**.