GITS_CTLR, ITS Control Register

The GITS_CTLR characteristics are:

Purpose

Controls the operation of an ITS.

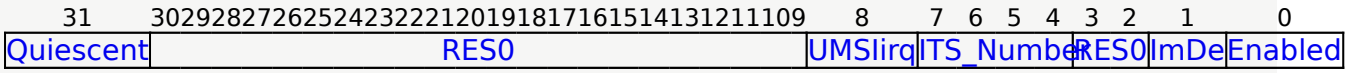
Configuration

The ITS_Number (bits [7:4]) and bit [1] fields apply only in FEAT_GICv4 implementations, and are res0 in FEAT_GICv3 implementations.

Attributes

GITS_CTLR is a 32-bit register.

Field descriptions



Quiescent, bit [31]

Read-only. Indicates completion of all ITS operations when GITS_CTLR.Enabled == 0.

Quiescent	Meaning
0b0	The ITS is not quiescent and cannot be powered down.
0b1	The ITS is quiescent and can be powered down.

For the ITS to be considered inactive, there must be no transactions in progress. In addition, all operations required to ensure that mapping data is consistent with external memory must be complete.

Note

In distributed GIC implementations, this bit is set to 1 only after the ITS forwards any operations that have not yet been completed to the Redistributors and receives confirmation that all such

operations have reached the appropriate Redistributor.

In FEAT_GICv3, FEAT_GICv3p1, and FEAT_GICv4, when GITS_CTLR.Enabled == 1, the value of GITS_CTLR.Quiescent is unknown.

In FEAT_GICv4p1, when GITS_CTLR.Enabled == 1, the value of GITS_CTLR.Quiescent reads as 1 until the write to Enabled has taken effect and then reads as 0.

The reset behavior of this field is:

- On a GIC reset, this field resets to `1`.

Bits [30:9]

Reserved, res0.

UMSIirq, bit [8]

Unmapped MSI reporting interrupt enable.

UMSIirq	Meaning
`0b0`	The ITS does not assert an interrupt signal when GITS_STATUSR.UMSI is 1.
`0b1`	The ITS asserts an interrupt signal when GITS_STATUSR.UMSI is 1.

If GITS_TYPER.UMSIirq is 0, this field is res0.

The reset behavior of this field is:

- On a Warm reset, this field resets to `0`.

ITS_Number, bits [7:4]

In FEAT_GICv3 implementations this field is res0.

In FEAT_GICv4 implementations with more than one ITS instance, this field indicates the ITS number for use with 'VMOVP GICv4.0' in ARMÂ® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

When GITS_TYPER.VMOVP is 1, this field may be implemented as res0.

It is implementation defined whether this field is programmable or RO.

If this field is programmable, changing this field when GITS_CTLR.Quiescent == 0 or GITS_CTLR.Enabled == 1 is unpredictable.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

Bits [3:2]

Reserved, res0.

ImDe, bit [1]

In GICv3 implementations, this bit is res0.

In GICv4 implementations, this bit is implementation defined.

The reset behavior of this field is:

- On a GIC reset, this field resets to `0`.

Enabled, bit [0]

Controls whether the ITS is enabled:

Enabled	Meaning
`0b0`	The ITS is not enabled. Writes to GITS_TRANSLATER are ignored and no further command queue entries are processed.
`0b1`	The ITS is enabled. Writes to GITS_TRANSLATER result in interrupt translations and the command queue is processed.

If a write to this register changes this field from 1 to 0, the ITS must ensure that both:

- Any caches containing mapping data are made consistent with external memory.
- GITS_CTLR.Quiescent == 0 until all caches are consistent with external memory.

Changing GITS_CTLR.Enabled from 0 to 1 when GITS_CTLR.Quiescent is 0 results in unpredictable behavior.

The reset behavior of this field is:

- On a GIC reset, this field resets to `0`.

Accessing GITS_CTLR

GITS_CTLR can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
GIC ITS control	0x0000	GITS_CTLR

Accesses on this interface are **RW**.

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