ID_AA64PFR2_EL1, AArch64 Processor Feature Register 2

The ID_AA64PFR2_EL1 characteristics are:

Purpose

Reserved for future expansion of information about implemented PE features in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

Configuration

There are no configuration notes.

Attributes

ID_AA64PFR2_EL1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
RES0																				MTEFAR				MTESTOREONLY				MTEPERM			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:12]

Reserved, res0.

MTEFAR, bits [11:8]

Information reported in FAR_ELx on a synchronous exception due to a Tag Check Fault. Defined values are:

MTEFAR	Meaning
0b0000	On a synchronous exception due to a Tag Check Fault, FAR_ELx[63:60] is unknown. Support for Memory Tagging when Address tagging is enabled.

0b0001	On a synchronous exception due to a Tag Check Fault, FAR_ELx[63:60] is not unknown. This feature is identified as FEAT_MTE_TAGGED_FAR.

All other values are reserved.

This field is valid when ID_AA64PFR1_EL1.MTE >= 0b0010 and ID_AA64PFR1_EL1.MTEX >= 0b0001.

FEAT_MTE4 implements the functionality identified by the value 0b0001.

From Armv8.9, the only permitted value is 0b0001.

MTESTOREONLY, bits [7:4]

Store-only Tag checking, identified as FEAT_MTE_STORE_ONLY. Defined values are:

MTESTOREONLY	Meaning
0b0000	FEAT_MTE_STORE_ONLY is not supported.
0b0001	FEAT_MTE_STORE_ONLY is supported.

All other values are reserved.

This field is valid when ID_AA64PFR1_EL1.MTE >= 0b0010 and ID_AA64PFR1_EL1.MTEX >= 0b0001.

FEAT_MTE4 implements the functionality identified by the value 0b0001.

From Armv8.9, the only permitted value is 0b0001.

MTEPERM, bits [3:0]

Tag access permissions. Defined values are:

MTEPERM	Meaning
0b0000	FEAT_MTE_PERM is not supported.
0b0001	FEAT_MTE_PERM is supported.

All other values are reserved.

This field is valid when ID_AA64PFR1_EL1.MTE >= 0b0010.

Accessing ID_AA64PFR2_EL1

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, ID_AA64PFR2_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0100	0b010

```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() &&
(IsFeatureImplemented(FEAT_FGT) || !
IsZero(ID_AA64PFR2_EL1) || boolean
IMPLEMENTATION_DEFINED "ID_AA64PFR2_EL1 trapped by
HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AA64PFR2_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64PFR2_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64PFR2_EL1;
```


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