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# PMCIDR2, Performance Monitors Component Identification Register 2

The PMCIDR2 characteristics are:

## **Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Component Identification scheme'.

## **Configuration**

This register is present only when FEAT\_PMUv3\_EXT is implemented and an implementation implements PMCIDR2. Otherwise, direct accesses to PMCIDR2 are res0.

If FEAT\_DoPD is implemented, this register is in the Core power domain. If FEAT\_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

### **Attributes**

PMCIDR2 is a 32-bit register.

This register is part of the **PMU** block.

# Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RES0	PRMBL 2

#### Bits [31:8]

Reserved, res0.

#### PRMBL 2, bits [7:0]

Preamble.

Reads as  $0 \times 05$ .

Access to this field is **RO**.

# **Accessing PMCIDR2**

Accesses to this register use the following encodings:

## Accessible at offset 0xFF8 from PMU

- When FEAT\_DoPD is implemented and !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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