AArch64
Instructions

Index by Encoding

External Registers

# SPMROOTCR\_EL3, System Performance Monitors Root and Realm Control Register

The SPMROOTCR EL3 characteristics are:

## **Purpose**

Controls observability of Root and Realm events by System PMU <s>.

## **Configuration**

This register is present only when FEAT\_RME is implemented and FEAT\_SPMU is implemented. Otherwise, direct accesses to SPMROOTCR EL3 are undefined.

## **Attributes**

SPMROOTCR EL3 is a 64-bit register.

## Field descriptions

63 626160595857565554535251504948474645444342414039383736 35 34 33 32

| IMPLEMENTATION DEFINED | NAO RESO RLO RTO |
31 302928272625242322212019181716151413121110 9 8 7 6 5 4 3 2 1 0

### **IMPLEMENTATION DEFINED, bits [63:32]**

implementation defined observation controls. Additional implementation defined bits to control certain types of filter or events.

## **IMPL**, bit [31]

Indicates SPMROOTCR\_EL3 is present.

The reset behavior of this field is:

• On a Warm reset, this field resets to an architecturally unknown value.

Access to this field is **RO**.

#### Bits [30:4]

Reserved, res0.

#### **NAO**, bit [3]

### When System PMU <s> can count or monitor non-attributable events:

Non-attributable Observation. Controls whether events or monitorable characteristics not attributable with any source can be monitored.

NAO	Meaning
0b0	Events not attributable with any
	event source are not counted.
0b1	Counting non-attributable events
	is not prevented by this field.

When both SPMROOTCR\_EL3 and <u>SPMSCR\_EL1</u> are implemented, non-attributable events are counted only if both SPMROOTCR\_EL3.NAO is 1 and <u>SPMSCR\_EL1</u>.{NAO, SO} is nonzero.

SPMROOTCR\_EL3.NAO has the opposite reset polarity to SPMSCR\_EL1.NAO.

The reset behavior of this field is:

• On a Warm reset, this field resets to 1.

#### Otherwise:

Reserved, res0.

#### Bit [2]

Reserved, res0.

#### **RLO, bit [1]**

Realm Observation. Controls whether events or monitorable characteristics attributable to a Realm event source can be monitored.

RLO	Meaning
0d0	Events attributable to a Realm
	event source are not counted.
0b1	Events attributable to a Realm
	event source are counted.

The reset behavior of this field is:

• On a Warm reset, this field resets to 0.

### **RTO, bit [0]**

Root Observation. Controls whether events or monitorable characteristics attributable to a Root event source can be monitored.

RTO	Meaning
0d0	Events attributable to a Root
	event source are not counted.
0b1	Events attributable to a Root
	event source are counted.

The reset behavior of this field is:

• On a Warm reset, this field resets to 0.

# Accessing SPMROOTCR\_EL3

To access SPMROOTCR\_EL3 for System PMU <s>, set <a href="https://spmselr.google.com/spmselr.google.g

Accesses to this register use the following encodings in the System register encoding space:

# MRS <Xt>, SPMR00TCR\_EL3

op0	op1	CRn	CRm	op2
0b10	0b110	0b1001	0b1110	0b111

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] =
SPMROOTCR_EL3[UInt(SPMSELR_EL0.SYSPMUSEL)];
```

# MSR SPMR00TCR\_EL3, <Xt>

op0	op1	CRn	CRm	op2
0b10	0b110	0b1001	0b1110	0b111

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    SPMROOTCR_EL3[UInt(SPMSELR_EL0.SYSPMUSEL)] =
X[t, 64];
```

AArch32 Registers AArch64 Registers

AArch32 Instructions AArch64
Instructions

Index by Encoding

External Registers

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.