

## BRBTGT<n>\_EL1, Branch Record Buffer Target Address Register <n>, n = 0 - 31

The BRBTGT<n>\_EL1 characteristics are:

### Purpose

The target address of Branch record n + ([BRBFCCR\\_EL1](#).BANK  $\bar{\wedge}$  32).

### Configuration

This register is present only when FEAT\_BRBE is implemented. Otherwise, direct accesses to BRBTGT<n>\_EL1 are undefined.

### Attributes

BRBTGT<n>\_EL1 is a 64-bit register.

### Field descriptions

|         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 63      | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| ADDRESS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ADDRESS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

#### ADDRESS, bits [63:0]

Target virtual address of the Branch record.

When an indirect write occurs with a value with ADDRESS bits [63:P] being other than all zeroes or all ones, an unknown value which is not all zeroes or all ones is written to bits [63:P]. P is defined as the virtual address size supported by the PE, as returned by `DebugAddrTop()`. The value in bits [P-1:0] is the value written.

When an indirect write occurs with a value with ADDRESS bits [63:P] being all zeroes or all ones, the written value is written to bits [63:0], and a read of the register returns the written value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- Access is **RES0** if any of the following are true:
  - BRBINF<n>\_EL1.VALID == 0b00
  - BRBINF<n>\_EL1.VALID == 0b10
- Otherwise, access to this field is **RO**.

## Accessing BRBTGT<n>\_EL1

BRBTGT<n>\_EL1 is res0 if  $n + (\text{BRBFCR\_EL1.BANK} \tilde{-} 32) \geq \text{BRBIDR0\_EL1.NUMREC}$ .

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, BRBTGT<m>\_EL1 ; Where m = 0-31

| op0  | op1   | CRn    | CRm    | op2       |
|------|-------|--------|--------|-----------|
| 0b10 | 0b001 | 0b1000 | m[3:0] | m[4]:0b10 |

```
integer m = UInt(op2<2>:CRm<3:0>);

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
    when SDD == '1'" && MDCR_EL3.SBRBE != '11' &&
    SCR_EL3.NS == '0' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD ==
    '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && MDCR_EL3.SBRBE == 'x0'
    && SCR_EL3.NS == '1' then
        UNDEFINED;
    elsif EL2Enabled() &&
    IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
    SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.nBRBDATA == '0'
    then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.SBRBE != '11' &&
    SCR_EL3.NS == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        elsif HaveEL(EL3) && MDCR_EL3.SBRBE == 'x0' &&
    SCR_EL3.NS == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
```

```

        elsif m + (UInt(BRBFCE_EL1.BANK) * 32) >=
NUM_BRBE_RECORDS then
            X[t, 64] = Zeros(64);
        else
            X[t, 64] = BRBTGT_EL1[m];
        elsif PSTATE.EL == EL2 then
            if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.SBRBE != '11' &&
SCR_EL3.NS == '0' then
                UNDEFINED;
            elsif Halted() && HaveEL(EL3) && EDSCR.SDD ==
'1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && MDCR_EL3.SBRBE == 'x0'
&& SCR_EL3.NS == '1' then
                UNDEFINED;
            elsif HaveEL(EL3) && MDCR_EL3.SBRBE != '11' &&
SCR_EL3.NS == '0' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch64.SystemAccessTrap(EL3, 0x18);
                elsif HaveEL(EL3) && MDCR_EL3.SBRBE == 'x0' &&
SCR_EL3.NS == '1' then
                    if Halted() && EDSCR.SDD == '1' then
                        UNDEFINED;
                    else
                        AArch64.SystemAccessTrap(EL3, 0x18);
                    elsif m + (UInt(BRBFCE_EL1.BANK) * 32) >=
NUM_BRBE_RECORDS then
                        X[t, 64] = Zeros(64);
                    else
                        X[t, 64] = BRBTGT_EL1[m];
                elsif PSTATE.EL == EL3 then
                    if m + (UInt(BRBFCE_EL1.BANK) * 32) >=
NUM_BRBE_RECORDS then
                        X[t, 64] = Zeros(64);
                    else
                        X[t, 64] = BRBTGT_EL1[m];

```

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