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Pseu

BFM

Bitfield Move is usually accessed via one of its aliases, which are always preferred for disassembly.

If <imms> is greater than or equal to <immr>, this copies a bitfield of (<imms>-<immr>+1) bits starting from bit position <immr> in the source register to the least significant bits of the destination register.

If <imms> is less than <immr>, this copies a bitfield of (<imms>+1) bits from the least significant bits of the source register to bit position (regsize-<immr>) of the destination register, where regsize is the destination register size of 32 or 64 bits.

In both cases the other bits of the destination register remain unchanged. This instruction is used by the aliases <u>BFC</u>, <u>BFI</u>, and <u>BFXIL</u>.

31 30 29 2	28 27	26	25	24	23	22	21 20 19 18 17 16	15 14 13 12 11 10	9	8	7	6	5	4	3	2	1	0
sf 0 1	1 0	0	1	1	0	Ν	immr	imms			Rn					Rd		
onc																		

```
32-bit (sf == 0 \&\& N == 0)
```

```
BFM <Wd>, <Wn>, #<immr>, #<imms>
```

64-bit (sf == 1 && N == 1)

```
BFM <Xd>, <Xn>, #<immr>, #<imms>

integer d = UInt(Rd);
integer n = UInt(Rn);
constant integer datasize = 32 << UInt(sf);

integer r;
bits(datasize) wmask;
bits(datasize) tmask;

if sf == '1' && N != '1' then UNDEFINED;
if sf == '0' && (N != '0' || immr<5> != '0' || imms<5> != '0') then UNDEFINED;

if under the under th
```

Assembler Symbols

<wd></wd>	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.
<wn></wn>	Is the 32-bit name of the general-purpose source register, encoded in the "Rn" field.
<xd></xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.

Is the 64-bit name of the general-purpose source register, encoded in the "Rn" field.
For the 32-bit variant: is the right rotate amount, in the range 0 to 31, encoded in the "immr" field.
For the 64-bit variant: is the right rotate amount, in the range 0 to 63, encoded in the "immr" field.
For the 32-bit variant: is the leftmost bit number to be moved from the source, in the range 0 to 31, encoded in the "imms" field.
For the 64-bit variant: is the leftmost bit number to be moved from the source, in the range 0 to 63, encoded in the "imms" field.

Alias Conditions

Alias	Is preferred when						
BFC	Rn == '11111' && <u>UInt</u> (imms) < <u>UInt</u> (immr)						
<u>BFI</u>	Rn != '11111' && <u>UInt</u> (imms) < <u>UInt</u> (immr)						
BFXIL	<pre>UInt(imms) >= UInt(immr)</pre>						

Operation

```
bits(datasize) dst = X[d, datasize];
bits(datasize) src = X[n, datasize];

// perform bitfield move on low bits
bits(datasize) bot = (dst AND NOT(wmask)) OR (ROR(src, r) AND wmask);

// combine extension bits and result bits
X[d, datasize] = (dst AND NOT(tmask)) OR (bot AND tmask);
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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Internal version only: is a v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56 Pseu

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