

## FMOV (register)

Floating-point Move register without conversion. This instruction copies the floating-point value in the SIMD&FP source register to the SIMD&FP destination register.

Depending on the settings in the [CPACR\\_EL1](#), [CPTR\\_EL2](#), and [CPTR\\_EL3](#) registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	1	1	1	1	0	f	t	y	p	e	1	0	0	0	0	0	0	1	0	0	0	0	Rn				Rd			
opc																																

### Half-precision (ftype == 11) (FEAT\_FP16)

FMOV <Hd>, <Hn>

### Single-precision (ftype == 00)

FMOV <Sd>, <Sn>

### Double-precision (ftype == 01)

FMOV <Dd>, <Dn>

```
if ftype == '10' || (ftype == '11' && !IsFeatureImplemented(FEAT_FP16))
integer d = UInt(Rd);
integer n = UInt(Rn);

constant integer esize = 8 << UInt(ftype EOR '10');
```

## Assembler Symbols

- <Dd> Is the 64-bit name of the SIMD&FP destination register, encoded in the "Rd" field.
- <Dn> Is the 64-bit name of the SIMD&FP source register, encoded in the "Rn" field.
- <Hd> Is the 16-bit name of the SIMD&FP destination register, encoded in the "Rd" field.
- <Hn> Is the 16-bit name of the SIMD&FP source register, encoded in the "Rn" field.
- <Sd> Is the 32-bit name of the SIMD&FP destination register, encoded in the "Rd" field.

<Sn> Is the 32-bit name of the SIMD&FP source register, encoded in the "Rn" field.

## Operation

```
CheckFPEnabled64();  
bits(128) result = 0<127:0>;  
bits(esize) operand = V[n, esize];  
Elem[result, 0, esize] = operand;  
V[d, 128] = result;
```

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
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