GICD_INMIR<n>, Non-maskable Interrupt Registers, x = 0 to 31, n = 0 - 31

The GICD_INMIR<n> characteristics are:

Purpose

Holds whether the corresponding SPI has the non-maskable property.

Configuration

This register is present only when FEAT_GICv3_NMI is implemented. Otherwise, direct accesses to GICD_INMIR<n> are res0.

When GICR_TYPER.NMI is 0, this register is res0.

The number of implemented GICD_INMIR<n> registers is (GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

Attributes

GICD_INMIR<n> is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	
NMI31	NMI30	NMI29	NMI28	NMI27	NMI26	NMI25	NMI24	NMI23	NMI22	NMI21	NMI20	NMI19	NMI18	NMI17	NM

NMI<x>, bit [x], for x = 31 to 0

Non-maskable property.

NMI<x>	Meaning
0b0	Interrupt does not have the non-maskable property.
0b1	Interrupt has the non-maskable property.

This bit is res0 when the corresponding interrupt is configured as Group 0.

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_INMI<n> number, n, is given by n = (m DIV 32).
- The offset of the required GICD_INMI is (`0xF80` + (4*n)).
- The bit number of the required in this register is (m MOD 32).

Accessing GICD_INMIR<n>

For SGIs and PPIs:

- The field for that interrupt is res0 and an implementation is permitted to make the field RAZ/WI in this case.
- Equivalent functionality is provided by GICR_INMIR0.

When affinity routing is not enabled for the Security state of an interrupt in GICD_IGROUPR<n>E, the corresponding bit is res0.

Bits corresponding to unimplemented interrupts are RAZ/WI.

When GICD_CTLR.DS==0, bits corresponding to Group 0 and Secure Group 1 interrupts are RAZ/WI to Non-secure accesses.

Note

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

GICD_INMIR<n> can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Distributor	Dist_base	`0x0F80` + (4 * n)	GICD_INMIR<n>

Accesses on this interface are **RW**.
