

FRECPX

Floating-point Reciprocal exponent (scalar). This instruction finds an approximate reciprocal exponent for the source SIMD&FP register and writes the result to the destination SIMD&FP register.

This instruction can generate a floating-point exception. Depending on the settings in *FPCR*, the exception results in either a flag being set in *FPSR* or a synchronous exception being generated. For more information, see *Floating-point exception traps*.

Depending on the settings in the *CPACR_EL1*, *CPTR_EL2*, and *CPTR_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

It has encodings from 2 classes: [Half-precision](#) and [Single-precision and double-precision](#)

Half-precision (FEAT_FP16)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0	1	1	1	1	0	0	1	1	1	1	1	1	0											
																Rn								Rd							

FRECPX <Hd>, <Hn>

```
if !IsFeatureImplemented(FEAT_FP16) then UNDEFINED;

integer d = UInt(Rd);
integer n = UInt(Rn);

constant integer esize = 16;
```

Single-precision and double-precision

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0	1	sz	1	0	0	0	0	1	1	1	1	1	1	0										
																Rn								Rd							

FRECPX <V><d>, <V><n>

```
integer d = UInt(Rd);
integer n = UInt(Rn);

constant integer esize = 32 << UInt(sz);
```

Assembler Symbols

- <Hd> Is the 16-bit name of the SIMD&FP destination register, encoded in the "Rd" field.
- <Hn> Is the 16-bit name of the SIMD&FP source register, encoded in the "Rn" field.

<V>

Is a width specifier, encoded in "sz":

sz	<V>
0	S
1	D

<d>

Is the number of the SIMD&FP destination register, encoded in the "Rd" field.

<n>

Is the number of the SIMD&FP source register, encoded in the "Rn" field.

Operation

```
CheckFPEnabled64();
bits(esize) operand = V[n, esize];

FPCRTYPE fpcr = FPCR[];
boolean merge = IsMerging(fpcr);
bits(128) result = if merge then V[d, 128] else Zeros(128);

Elem[result, 0, esize] = FPRecpX(operand, fpcr);

V[d, 128] = result;
```

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode
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