AMPIDR1, Activity Monitors Peripheral Identification Register 1

The AMPIDR1 characteristics are:

Purpose

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

It is implementation defined whether AMPIDR1 is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is optional.

This register is present only when FEAT_AMUv1 is implemented.

Attributes

AMPIDR1 is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
RES0	DES_0	PART_1

Bits [31:8]

Reserved, res0.

DES_0, bits [7:4]

Designer, least significant nibble of JEP106 ID code.

For Arm Limited, this field is `0b1011`.

This field has an implementation defined value.

Access to this field is **RO**.

PART_1, bits [3:0]

Part number, most significant nibble.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing AMPIDR1

AMPIDR1 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
AMU	0xFE4	AMPIDR1

Accesses on this interface are **RO**.

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