SPMCGCR<n>_EL1, Counter Group Configuration Register <n>, n = 0 - 1

The SPMCGCR<n>_EL1 characteristics are:

Purpose

Describes the configuration of counter groups in System PMU <s>.

Configuration

This register is present only when FEAT_SPMU is implemented. Otherwise, direct accesses to SPMCGCR<n>_EL1 are undefined.

Attributes

SPMCGCR<n>_EL1 is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56	55 54 53 52 51 50 49 48	47 46 45 44 43 42 41 40	39 38 37 36 35 34 33 32
N7	N6	N5	N4
N3	N2	N1	N0
31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

N<m>, bits [8m+7:8m], for m = 7 to 0

Number of counters in group nÃ—8+m.

The maximum size of each counter group depends on the number of implemented groups and the largest implemented counter size. For more information, see SPMCFGR_EL1.NCG.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing SPMCGCR<n>_EL1

To access SPMCGCR<n>_EL1 for System PMU <s>, set SPMSELR_EL0.SYSPMUSEL to s.

SPMCGCR<n>_EL1 reads-as-zero if any of the following are true:

- The System PMU selected by SPMSELR_EL0.SYSPMUSEL is not implemented.
- SPMCFGR_EL1.NCG is zero.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, SPMCGCR<m>_EL1 ; Where m = 0-1

op0	op1	CRn	CRm	op2
0b10	0b000	0b1001	0b1101	0b00:m[0]

```
integer m = UInt(op2<0>);

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nSPMID == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMCGCR_EL1[UInt(SPMSELR_EL0.SYSPMUSEL)];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMCGCR_EL1[UInt(SPMSELR_EL0.SYSPMUSEL)];
elsif PSTATE.EL == EL3 then
```

```
    X[t, 64] =
SPMCGCR_EL1[UInt(SPMSELR_EL0.SYSPMUSEL)];
```

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