

GICR_ICFGR<n>E, Interrupt configuration registers, n = 2 - 5

The GICR_ICFGR<n>E characteristics are:

Purpose

Determines whether the corresponding PPI in the extended PPI range is edge-triggered or level-sensitive.

Configuration

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ICFGR<n>E are res0.

A copy of this register is provided for each Redistributor.

Attributes

GICR_ICFGR<n>E is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Int_conf0	Int_conf1	Int_conf2	Int_conf3	Int_conf4	Int_conf5	Int_conf6	Int_conf7	Int_conf8	Int_conf9	Int_conf10	Int_conf11	Int_conf12	Int_conf13	Int_conf14	Int_conf15	Int_conf16	Int_conf17	Int_conf18	Int_conf19	Int_conf20	Int_conf21	Int_conf22	Int_conf23	Int_conf24	Int_conf25	Int_conf26	Int_conf27	Int_conf28	Int_conf29	Int_conf30	Int_conf31

Int_conf<x>, bits [2x+1:2x], for x = 15 to 0

Indicates whether the interrupt is level-sensitive or edge-triggered.

Int_conf[0] (bit [2x]) is res0.

Int_conf<x>	Meaning
0b00	The corresponding interrupt is level-sensitive.
0b10	The corresponding interrupt is edge-triggered.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

For each supported extended PPI, it is implementation defined whether software can program the corresponding Int_config field.

Accessing GICR_ICFGR<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICFGR<n>E, the corresponding bit is res0.

When [GICD_CTLR](#).DS==0, a register bit that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

GICR_ICFGR<n>E can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Redistributor	SIG_base	0x0C00 + (4 * n)	GICR_ICFGR<n>E

Accesses on this interface are **RW**.

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

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