

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	1	0	1	1	1	Zm			0	Rv	1	1	1	Zn			0	1	off3						
SZ																		S													

```
BFMLS ZA.H[<Wv>, <offs>{, VGx4}], { <Zn1>.H-<Zn4>.H }, <Zm>.H
```

```
if !HaveSME2() || !IsFeatureImplemented(FEAT_SVE_B16B16) then UNDEFINED
integer v = UInt('010':Rv);
integer n = UInt(Zn);
integer m = UInt('0':Zm);
integer offset = UInt(off3);
boolean sub_op = TRUE;
constant integer nreg = 4;
```

Assembler Symbols

<Wv>	Is the 32-bit name of the vector select register W8-W11, encoded in the "Rv" field.
<offs>	Is the vector select offset, in the range 0 to 7, encoded in the "off3" field.
<Zn1>	Is the name of the first scalable vector register of a multi-vector sequence, encoded as "Zn".
<Zn4>	Is the name of the fourth scalable vector register of a multi-vector sequence, encoded as "Zn" plus 3 modulo 32.
<Zn2>	Is the name of the second scalable vector register of a multi-vector sequence, encoded as "Zn" plus 1 modulo 32.
<Zm>	Is the name of the second source scalable vector register Z0-Z15, encoded in the "Zm" field.

Operation

```
CheckStreamingSVEAndZAAEnabled();
constant integer VL = CurrentVL;
constant integer elements = VL DIV 16;
integer vectors = VL DIV 8;
integer vstride = vectors DIV nreg;
bits(32) vbase = X[v, 32];
integer vec = (UInt(vbase) + offset) MOD vstride;
bits(VL) result;

for r = 0 to nreg-1
  bits(VL) operand1 = Z[(n+r) MOD 32, VL];
  bits(VL) operand2 = Z[m, VL];
  bits(VL) operand3 = ZAvector[vec, VL];
  for e = 0 to elements-1
    bits(16) element1 = Elem[operand1, e, 16];
    bits(16) element2 = Elem[operand2, e, 16];
    bits(16) element3 = Elem[operand3, e, 16];
    if sub_op then element1 = BFNeg(element1);
    Elem[result, e, 16] = BFMulAdd_ZA(element3, element1, element2,
    ZAvector[vec, VL] = result;
  vec = vec + vstride;
```

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode
no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56

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