Move general-purpose register to a vector element. This instruction copies the contents of the source general-purpose register to the specified vector element in the destination SIMD&FP register.

This instruction can insert data into individual elements within a SIMD&FP register without clearing the remaining bits to zero.

Depending on the settings in the *CPACR\_EL1*, *CPTR\_EL2*, and *CPTR\_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

This is an alias of INS (general). This means:

- The encodings in this description are named to match the encodings of <u>INS (general)</u>.
- The description of <u>INS (general)</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

is equivalent to

and is always the preferred disassembly.

## **Assembler Symbols**

<Vd>

Is the name of the SIMD&FP destination register, encoded in the "Rd" field.

<Ts>

Is an element size specifier, encoded in "imm5":

imm5	<ts></ts>
x0000	RESERVED
xxxx1	В
xxx10	Н
xx100	S
x1000	D

<index>

Is the element index encoded in "imm5":

imm5	<index></index>
x0000	RESERVED
xxxx1	imm5<4:1>
xxx10	imm5<4:2>
xx100	imm5<4:3>
x1000	imm5<4>

<R>

Is the width specifier for the general-purpose source register, encoded in "imm5":

imm5	<r></r>		
x0000	RESERVED		
xxxx1	W		
xxx10	W		
xx100	W		
x1000	X		

<n>

Is the number [0-30] of the general-purpose source register or ZR (31), encoded in the "Rn" field.

## **Operation**

The description of <u>INS (general)</u> gives the operational pseudocode for this instruction.

## **Operational information**

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel; Build timestamp: 2023-09-18T17:56

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Sh Pseu