GICM_CLRSPI_SR, Clear Secure SPI Pending Register

The GICM_CLRSPI_SR characteristics are:

Purpose

Removes the pending state from a valid SPI.

A write to this register changes the state of a pending SPI to inactive, and the state of an active and pending SPI to active.

Configuration

This register is present only when GICM_TYPER.SR == 1 and GICM_TYPER.CLR == 1. Otherwise, direct accesses to GICM_CLRSPI_SR are res0.

When GICD_CTLR.DS == 1, this register is WI.

Attributes

GICM_CLRSPI_SR is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
RES0	INTID

Bits [31:13]

Reserved, res0.

INTID, bits [12:0]

This field is an alias of GICD_CLRSPI_SR.

Accessing GICM_CLRSPI_SR

Writes to this register have no effect if:

- The value is written by a Non-secure access.
- The value written specifies an invalid SPI.
- The SPI is not pending.

16-bit accesses to bits [15:0] of this register must be supported.

GICM_CLRSPI_SR can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Distributor	MSI_base	0x0058	GICD_CLRSPI_SR

This interface is accessible as follows:

- When GICD_CTLR.DS == 1, accesses to this register are **WI**.
- When GICD_CTLR.DS == 0 and an access is Secure, accesses to this register are **WO**.
- When GICD_CTLR.DS == 0 and an access is Non-secure, accesses to this register are **WI**.
- When GICD_CTLR.DS == 0, FEAT_RME is implemented and an access is Root, accesses to this register are **WO**.
- When GICD_CTLR.DS == 0, FEAT_RME is implemented and an access is Realm, accesses to this register are **WI**.

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