

GCSPUSHM, Guarded Control Stack Push

The GCSPUSHM characteristics are:

Purpose

Decrements the current Guarded control stack pointer register by the size of a Guarded control stack procedure return record and stores an entry to the Guarded control stack.

Configuration

This instruction is present only when FEAT_GCS is implemented. Otherwise, direct accesses to GCSPUSHM are undefined.

Attributes

GCSPUSHM is a 64-bit System instruction.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
input for Guarded control stack procedure return record																															
input for Guarded control stack procedure return record																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:0]

Input value for Guarded control stack procedure return record.

Executing GCSPUSHM

Accesses to this instruction use the following encodings in the System instruction encoding space:

GCSPUSHM <Xt>

op0	op1	CRn	CRm	op2
0b01	0b011	0b0111	0b0111	0b000

```
if PSTATE.EL == EL0 then
    if (!EL2Enabled() || HCR_EL2.TGE != '1') &&
```

```

GCSCRE0_EL1.PUSHMEN == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elseif EL2Enabled() && HCR_EL2.TGE == '1' &&
GCSCRE0_EL1.PUSHMEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    GCSPUSHM(X[t, 64]);
elseif PSTATE.EL == EL1 then
    if GCSCR_EL1.PUSHMEN == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elseif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGITR_EL2.nGCSPUSHM_EL1 ==
'0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        GCSPUSHM(X[t, 64]);
elseif PSTATE.EL == EL2 then
    if GCSCR_EL2.PUSHMEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        GCSPUSHM(X[t, 64]);
elseif PSTATE.EL == EL3 then
    if GCSCR_EL3.PUSHMEN == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        GCSPUSHM(X[t, 64]);

```

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.