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Pseu

MOVS (predicated)

Move predicates (zeroing), setting the condition flags

Read active elements from the source predicate and place in the corresponding elements of the destination predicate. Inactive elements in the destination predicate register are set to zero. Sets the first (N), none (Z), !last (C) condition flags based on the predicate result, and the V flag to zero.

This is an alias of ANDS. This means:

- The encodings in this description are named to match the encodings of ANDS.
- The description of <u>ANDS</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

is equivalent to

ANDS
$$\langle Pd \rangle$$
.B, $\langle Pq \rangle / Z$, $\langle Pn \rangle$.B, $\langle Pn \rangle$.B

and is the preferred disassembly when S == '1' && Pn == Pm.

Assembler Symbols

<pd></pd>	Is the name of the destination scalable predicate register,
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

encoded in the "Pd" field.

<Pg> Is the name of the governing scalable predicate register,

encoded in the "Pg" field.

<Pn> Is the name of the first source scalable predicate register.

encoded in the "Pn" field.

Operation

The description of <u>ANDS</u> gives the operational pseudocode for this instruction.

Operational information

If FEAT_SVE2 is implemented or FEAT_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its operand registers when its governing predicate register contains the same value for each execution.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its operand registers when its governing predicate register contains the same value for each execution.
 - The values of the NZCV flags.

If FEAT_SME is implemented and the PE is in Streaming SVE mode, then any subsequent instruction which is dependent on the NZCV condition flags written by this instruction might be significantly delayed.

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