

Zero ZA quad-vector groups

It has encodings from 3 classes: One ZA quad-vector , Two ZA quad-vectors and Four ZA quad-vectors

[illegible]

```
if !HaveSME2p1() then UNDEFINED;
integer v = UInt('010':Rv);
integer offset = UInt(off2:'00');
constant integer ngrp = 1;
constant integer nvec = 4;
```

[illegible]

```
if !HaveSME2p1() then UNDEFINED;
integer v = UInt('010':Rv);
integer offset = UInt(o1:'00');
constant integer ngrp = 2;
constant integer nvec = 4;
```

[illegible]

ZERO ZA.D[<Wv>, <offs1>:<offs4>, VGx4]

```
if !HaveSME2p1() then UNDEFINED;
integer v = UInt('010':Rv);
integer offset = UInt(o1:'00');
constant integer ngrp = 4;
constant integer nvec = 4;
```

Assembler Symbols

<Wv>	Is the 32-bit name of the vector select register W8-W11, encoded in the "Rv" field.
<offs1>	<p>For the one ZA quad-vector variant: is the vector select offset, pointing to first of four consecutive vectors, encoded as "off2" field times 4.</p> <p>For the four ZA quad-vectors and two ZA quad-vectors variant: is the vector select offset, pointing to first of four consecutive vectors, encoded as "o1" field times 4.</p>
<offs4>	<p>For the one ZA quad-vector variant: is the vector select offset, pointing to last of four consecutive vectors, encoded as "off2" field times 4 plus 3.</p> <p>For the four ZA quad-vectors and two ZA quad-vectors variant: is the vector select offset, pointing to last of four consecutive vectors, encoded as "o1" field times 4 plus 3.</p>

Operation

```
CheckStreamingSVEAndZAEEnabled();
constant integer VL = CurrentVL;
integer vectors = VL DIV 8;
integer vstride = vectors DIV ngrp;
bits(32) vbase = X[v, 32];
integer vec = (UInt(vbase) + offset) MOD vstride;
vec = vec - (vec MOD nvec);

for r = 0 to ngrp-1
    for i = 0 to nvec-1
        ZAvector[vec + i, VL] = Zeros(VL);
    vec = vec + vstride;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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