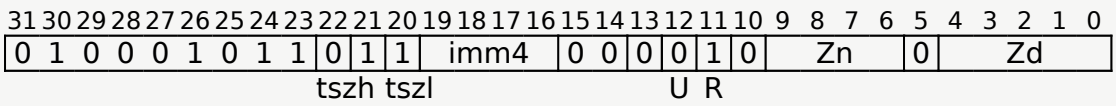
SQRSHRUN

Signed saturating rounding shift right unsigned narrow by immediate and interleave

Shift right by an immediate value, the signed integer value in each element of the group of two source vectors and place the two-way interleaved rounded results in the half-width destination elements. Each result element is saturated to the half-width N-bit element's unsigned integer range 0 to (2^N)-1. The immediate shift amount is an unsigned value in the range 1 to 16.
This instruction is unpredicated.

SVE2
(FEAT_SVE2p1)



SQRSHRUN <Zd>.H, { <Zn1>.S-<Zn2>.S }, #<const>

```
if !HaveSME2() && !HaveSVE2p1() then UNDEFINED;
constant integer esize = 16;
integer n = UInt(Zn:'0');
integer d = UInt(Zd);
integer shift = esize - UInt(imm4);
```

Assembler Symbols

<Zd>	Is the name of the destination scalable vector register, encoded in the "Zd" field.
<Zn1>	Is the name of the first scalable vector register of a multi-vector sequence, encoded as "Zn" times 2.
<Zn2>	Is the name of the second scalable vector register of a multi-vector sequence, encoded as "Zn" times 2 plus 1.
<const>	Is the immediate shift amount, in the range 1 to 16, encoded in the "imm4" field.

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV (2 * esize);
bits(VL) result;
```

```
for e = 0 to elements-1
    for i = 0 to 1
        bits(VL) operand = Z[n+i, VL];
        bits(2 * esize) element = Elem[operand, e, 2 * esize];
        integer res = (SInt(element) + (1 << (shift-1))) >> shift;
        Elem[result, 2*e + i, esize] = UnsignedSat(res, esize);

Z[d, VL] = result;
```

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