ID_AA64ZFR0_EL1, SVE Feature ID Register 0

The ID_AA64ZFR0_EL1 characteristics are:

Purpose

Provides additional information about the implemented features of the AArch64 Scalable Vector Extension instruction set, when one or more of FEAT_SVE and FEAT_SME is implemented.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

Configuration

Note

Prior to the introduction of the features described by this register, this register was unnamed and reserved, res0 from EL1, EL2, and EL3.

If FEAT_SME is implemented and FEAT_SVE is not implemented, then SVE instructions can only be executed when the PE is in Streaming SVE mode and the instructions are legal to execute in Streaming SVE mode.

Attributes

ID_AA64ZFR0_EL1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0				F64MM				F32MM				RES0				I8MM				SM4				RES0				SHA3			
RES0				B16B16				BF16				BitPerm				RES0								AES				SVEver			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:60]

Reserved, res0.

F64MM, bits [59:56]

Indicates support for SVE FP64 double-precision floating-point matrix multiplication instructions. Defined values are:

F64MM	Meaning
0b0000	Double-precision matrix multiplication and related SVE instructions are not implemented.
0b0001	Double-precision variant of the FMMLA instruction, and the LD1RO* instructions are implemented. The 128-bit element variants of the SVE TRN1, TRN2, UZP1, UZP2, ZIP1, and ZIP2 instructions are also implemented.

All other values are reserved.

FEAT_F64MM implements the functionality identified by 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the instructions described by nonzero values of this field, irrespective of the value of this field.

F32MM, bits [55:52]

Indicates support for the SVE FP32 single-precision floating-point matrix multiplication instruction. Defined values are:

F32MM	Meaning
0b0000	Single-precision matrix multiplication instruction is not implemented.
0b0001	Single-precision variant of the FMMLA instruction is implemented.

All other values are reserved.

FEAT_F32MM implements the functionality identified by 0b0001.

From Arm v8.2, the permitted values are 0b0000 and 0b0001.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not

attempt to execute the instructions described by nonzero values of this field, irrespective of the value of this field.

Bits [51:48]

Reserved, res0.

I8MM, bits [47:44]

Indicates support for SVE Int8 matrix multiplication instructions. Defined values are:

I8MM	Meaning
0b0000	SVE Int8 matrix multiplication instructions are not implemented.
0b0001	SVE SMMLA, SUDOT, UMMLA, USMMLA, and USDOT instructions are implemented.

All other values are reserved.

FEAT_I8MM implements the functionality identified by 0b0001.

When Advanced SIMD and SVE are both implemented, this field must return the same value as ID_AA64ISAR1_EL1.I8MM.

From Armv8.6, the only permitted value is 0b0001.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the SVE instructions SMMLA, UMMLA, and USMMLA, irrespective of the value of this field.

SM4, bits [43:40]

Indicates support for SVE SM4 instructions. Defined values are:

SM4	Meaning
0b0000	SVE SM4 instructions are not implemented.
0b0001	SVE SM4E and SM4EKEY instructions are implemented.

All other values are reserved.

FEAT_SVE_SM4 implements the functionality identified by 0b0001.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the instructions described by nonzero values of this field, irrespective of the value of this field.

Bits [39:36]

Reserved, res0.

SHA3, bits [35:32]

Indicates support for the SVE SHA3 instructions. Defined values are:

SHA3	Meaning
0b0000	SVE SHA3 instructions are not implemented.
0b0001	SVE RAX1 instruction is implemented.

All other values are reserved.

FEAT_SVE_SHA3 implements the functionality identified by 0b0001.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the instructions described by nonzero values of this field, irrespective of the value of this field.

However, if both FEAT_SME2p1 and FEAT_SVE_SHA3 are implemented, then the SVE RAX1 instruction can be executed when the PE is in Streaming SVE mode regardless of whether FEAT_SME_FA64 is implemented and enabled.

Bits [31:28]

Reserved, res0.

B16B16, bits [27:24]

Indicates support for SVE2.1 non-widening BFloat16 instructions. Defined values are:

B16B16	Meaning
0b0000	SVE2.1 non-widening BFloat16 instructions are not implemented.
0b0001	SVE2.1 non-widening BFloat16 instructions are implemented.

FEAT_B16B16 implements the functionality identified by 0b0001.

This field must indicate the same level of support as ID_AA64SMFR0_EL1.B16B16.

If one or more of FEAT_SVE2p1 and FEAT_SME2p1 is implemented, the values 0b0000 and 0b0001 are permitted.

Otherwise, the only permitted value is 0b0000.

BF16, bits [23:20]

Indicates support for SVE BFloat16 instructions. Defined values are:

BF16	Meaning
0b0000	SVE BFloat16 instructions are not implemented.
0b0001	SVE BFCVT, BFCVTNT, BFDOT, BFMLALB, BFMLALT, and BFMMLA instructions are implemented.
0b0010	As 0b0001, but the FPCR.EBF field is also supported.

All other values are reserved.

FEAT_BF16 adds the functionality identified by 0b0001.

FEAT_EBF16 adds the functionality identified by 0b0010.

This field must return the same value as ID_AA64ISAR1_EL1.BF16.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the SVE instruction BFMMLA, irrespective of the value of this field.

From Armv8.6 and Armv9.1, the value 0b0000 is not permitted.

BitPerm, bits [19:16]

Indicates support for SVE bit permute instructions. Defined values are:

BitPerm	Meaning
0b0000	SVE bit permute instructions are not implemented.
0b0001	SVE BDEP, BEXT, and BGRP instructions are implemented.

All other values are reserved.

FEAT_SVE_BitPerm implements the functionality identified by `0b0001`.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the instructions described by nonzero values of this field, irrespective of the value of this field.

Bits [15:8]

Reserved, res0.

AES, bits [7:4]

Indicates support for SVE AES instructions. Defined values are:

AES	Meaning
`0b0000`	SVE AES* instructions are not implemented.
`0b0001`	SVE AESE, AESD, AESMC, and AESIMC instructions are implemented.
`0b0010`	As `0b0001`, plus 64-bit source element variants of SVE PMULLB and PMULLT instructions are implemented.

All other values are reserved.

FEAT_SVE_AES implements the functionality identified by the value `0b0001`.

FEAT_SVE_PMULL128 implements the functionality identified by the value `0b0010`.

The permitted values are `0b0000` and `0b0010`.

When the PE is in Streaming SVE mode and it is not known whether FEAT_SME_FA64 is implemented and enabled, software should not attempt to execute the instructions described by nonzero values of this field, irrespective of the value of this field.

SVEver, bits [3:0]

Indicates support for SVE instructions when one or more of FEAT_SME and FEAT_SVE is implemented. Defined values are:

SVEver	Meaning
`0b0000`	The SVE instructions are implemented.

0b0001	As 0b0000, and adds the mandatory SVE2 instructions.
0b0010	As 0b0001, and adds the mandatory SVE2.1 instructions.

All other values are reserved.

From Armv9, if this register is present, the value 0b0000 is not permitted.

FEAT_SVE2 implements the functionality identified by 0b0001 when the PE is not in Streaming SVE mode.

FEAT_SME implements the functionality identified by 0b0001 when the PE is in Streaming SVE mode.

FEAT_SME2p1 implements the functionality identified by 0b0010 when the PE is in Streaming SVE mode.

FEAT_SVE2p1 implements the functionality identified by 0b0010 when the PE is not in Streaming SVE mode.

From Armv9.4, the value 0b0001 is not permitted.

Accessing ID_AA64ZFR0_EL1

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, ID_AA64ZFR0_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0100	0b100

```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() &&
(IsFeatureImplemented(FEAT_FGT) || !
IsZero(ID_AA64ZFR0_EL1) || boolean
IMPLEMENTATION_DEFINED "ID_AA64ZFR0_EL1 trapped by
HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
```

```
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            X[t, 64] = ID_AA64ZFR0_EL1;
    elsif PSTATE.EL == EL2 then
        X[t, 64] = ID_AA64ZFR0_EL1;
    elsif PSTATE.EL == EL3 then
        X[t, 64] = ID_AA64ZFR0_EL1;
```

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94