GITS_CBASER, ITS Command Queue Descriptor

The GITS CBASER characteristics are:

Purpose

Specifies the base address and size of the ITS command queue.

Configuration

Bits [63:32] and bits [31:0] are accessible separately.

Attributes

GITS_CBASER is a 64-bit register.

Field descriptions

63	62	616059	585756	5555453	52	5150494847464544	43 42 41	4039383	3736353	43332
Valid	RESC	InnerCa	ettes0	OuterC	Rd 540	Phy	/sical_Ac	ddress		
Physical_Address					Shar Rall	560 ty	Size			
31	30	292827	262524	1232221	20	1918171615141312	1110 9	8 7 6	5 4 3 2	1 0

Valid, bit [63]

Indicates whether software has allocated memory for the command queue:

Valid	Meaning
0b0	No memory is allocated for the
	command queue.
0b1	Memory is allocated to the
	command queue.

The reset behavior of this field is:

• On a GIC reset, this field resets to 0.

Bit [62]

Reserved, res0.

InnerCache, bits [61:59]

Indicates the Inner Cacheability attributes of accesses to the command queue. The possible values of this field are:

InnerCache	Meaning
0b000	Device-nGnRnE.
0b001	Normal Inner Non- cacheable.
0b010	Normal Inner Cacheable Read-allocate, Write- through.
0b011	Normal Inner Cacheable Read-allocate, Write-back.
0b100	Normal Inner Cacheable Write-allocate, Write- through.
0b101	Normal Inner Cacheable Write-allocate, Write- back.
0b110	Normal Inner Cacheable Read-allocate, Write- allocate, Write-through.
0b111	Normal Inner Cacheable Read-allocate, Write- allocate, Write-back.

The reset behavior of this field is:

• On a GIC reset, this field resets to an architecturally unknown value.

Bits [58:56]

Reserved, res0.

OuterCache, bits [55:53]

Indicates the Outer Cacheability attributes of accesses to the command queue. The possible values of this field are:

OuterCache	Meaning
0b000	Memory type defined in
	InnerCache field. For
	Normal memory, Outer
	Cacheability is the same
	as Inner Cacheability.
0b001	Normal Outer Non-cacheable.

Ok	0010	Normal Outer Cacheable Read-allocate, Write- through.	
Ok	0011	Normal Outer Cacheable Read-allocate, Write-back.	
Ok	0100	Normal Outer Cacheable Write-allocate, Write- through.	
Ol	0101	Normal Outer Cacheable Write-allocate, Write- back.	
Ok	o110	Normal Outer Cacheable Read-allocate, Write- allocate, Write-through.	
Ol	o111	Normal Outer Cacheable Read-allocate, Write- allocate, Write-back.	

It is implementation defined whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

The reset behavior of this field is:

• On a GIC reset, this field resets to an architecturally unknown value.

Bit [52]

Reserved, res0.

Physical Address, bits [51:12]

Bits [51:12] of the base physical address of the command queue. Bits [11:0] of the base address are 0.

In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are res0.

If bits [15:12] are not all zeros, behavior is a constrained unpredictable choice:

- Bits [15:12] are treated as if all the bits are zero. The value read back from those bits is either the value written or zero.
- The result of the calculation of an address for a command queue read can be corrupted.

The reset behavior of this field is:

• On a GIC reset, this field resets to an architecturally unknown value.

Shareability, bits [11:10]

Indicates the Shareability attributes of accesses to the command queue. The possible values of this field are:

Shareability	Meaning
0b00	Non-shareable.
0b01	Inner Shareable.
0b10	Outer Shareable.
0b11	Reserved. Treated as 0b00.

It is implementation defined whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

The reset behavior of this field is:

• On a GIC reset, this field resets to an architecturally unknown value.

Bits [9:8]

Reserved, res0.

Size, bits [7:0]

The number of 4KB pages of physical memory allocated to the command queue, minus one.

The reset behavior of this field is:

• On a GIC reset, this field resets to an architecturally unknown value.

The command queue is a circular buffer and wraps at Physical Address [47:0] + (4096 * (Size + 1)).

Note

When this register is successfully written, the value of GITS CREADR is set to zero.

Accessing GITS_CBASER

When <u>GITS_CTLR</u>.Enabled == 1 or <u>GITS_CTLR</u>.Quiescent == 0, writing this register is unpredictable.

GITS_CBASER can be accessed through the memory-mapped interfaces:

Component	Offset	Instance	
GIC ITS control	0x0080	GITS_CBASER	

Accesses on this interface are RW.

AArch32	AArch64	AArch32	AArch64	Index by	<u>External</u>
<u>Registers</u>	<u>Registers</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding	<u>Registers</u>

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