Index by

Encoding

Base

Instructions

Test bit and Branch if Zero compares the value of a test bit with zero, and conditionally branches to a label at a PC-relative offset if the comparison is equal. It provides a hint that this is not a subroutine call or return. This instruction does not affect condition flags.

31 30	29	28	27	26	25	24	23 22 21 20 19	18 17 16 15 14 13 12 11 10 9 8 7 6 5	4	3	2	1	0
b5 0	1	1	0	1	1	0	b40	imm14	Rt				
ор													

```
TBZ <R><t>, #<imm>, <label>
```

```
integer t = <u>UInt</u>(Rt);
constant integer datasize = 32 << UInt(b5);</pre>
integer bit_pos = UInt(b5:b40);
bits (64) offset = SignExtend (imm14:'00', 64);
```

Assembler Symbols

<R>

Is a width specifier, encoded in "b5":

b 5	<r></r>					
0	W					
1	X					

In assembler source code an 'X' specifier is always permitted, but a 'W' specifier is only permitted when the bit number is less than 32.

<t>>

Is the number [0-30] of the general-purpose register to be tested or the name ZR (31), encoded in the "Rt" field.

<imm>

<label>

Is the bit number to be tested, in the range 0 to 63, encoded in "b5:b40".

Is the program label to be conditionally branched to. Its offset from the address of this instruction, in the range +/-32KB, is encoded as "imm14" times 4.

Operation

```
bits (datasize) operand = X[t, datasize];
if operand<br/>bit_pos> == op then
    BranchTo(PC64 + offset, BranchType DIR, TRUE);
else
    BranchNotTaken (BranchType_DIR, TRUE);
```

BaseSIMD&FPSVESMEIndex byInstructionsInstructionsInstructionsInstructions

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56

Sh Pseu

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.