

## HFGITR2\_EL2, Hypervisor Fine-Grained Instruction Trap Register 2

The HFGITR2\_EL2 characteristics are:

### Purpose

Provides instruction trap controls.

### Configuration

This register is present only when FEAT\_FGT2 is implemented. Otherwise, direct accesses to HFGITR2\_EL2 are undefined.

### Attributes

HFGITR2\_EL2 is a 64-bit register.

### Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
RES0																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

#### Bits [63:0]

Reserved, res0.

### Accessing HFGITR2\_EL2

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, HFGITR2\_EL2

op0	op1	CRn	CRm	op2
0b11	0b100	0b0011	0b0001	0b111

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
```

```

        if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
            X[t, 64] = NVMem[0x310];
        elsif EL2Enabled() && HCR_EL2.NV == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
        && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
        when SDD == '1'" && SCR_EL3.FGTEn2 == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.FGTEn2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            X[t, 64] = HFGITR2_EL2;
    elsif PSTATE.EL == EL3 then
        X[t, 64] = HFGITR2_EL2;

```

## MSR HFGITR2\_EL2, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b100	0b0011	0b0001	0b111

```

    if PSTATE.EL == EL0 then
        UNDEFINED;
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
            NVMem[0x310] = X[t, 64];
        elsif EL2Enabled() && HCR_EL2.NV == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
        && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
        when SDD == '1'" && SCR_EL3.FGTEn2 == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.FGTEn2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            HFGITR2_EL2 = X[t, 64];
    elsif PSTATE.EL == EL3 then
        HFGITR2_EL2 = X[t, 64];

```

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.