PMIIDR, Performance Monitors Implementation Identification Register

The PMIIDR characteristics are:

Purpose

Provides discovery information about the Performance Monitor component.

Configuration

This register is present only when (FEAT_PMUv3_EXT32 is implemented and an implementation implements PMIIDR) or FEAT_PMUv3_EXT64 is implemented. Otherwise, direct accesses to PMIIDR are res0.

Attributes

PMIIDR is a:

- 64-bit register when FEAT_PMUv3_EXT64 is implemented
- 32-bit register otherwise

This register is part of the PMU block.

Field descriptions

When FEAT_PMUv3_EXT64 is implemented:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32																															
RES0																															
ProductID												Variant				Revision				Implementer[11:8]				RES0				Implementer[6:0]			
31 30 29 28 27 26 25 24 23 22 21 20												19 18 17 16				15 14 13 12				11 10 9 8				7 6 5 4				3 2 1 0			

Bits [63:32]

Reserved, res0.

ProductID, bits [31:20]

Part number, bits [11:0]. The part number is selected by the designer of the component.

Matches the PMU.PMPIDR1.PART_1, PMU.PMPIDR0.PART_0 fields if present.

This field has an implementation defined value.

Access to this field is **RO**.

Variant, bits [19:16]

Component major revision.

Defines either a variant of the component defined by PMIIDR.ProductID, or the major revision of the component.

When defining a major revision, PMIIDR.Variant and PMIIDR.Revision together form the revision number of the component, with this field being the most significant part.

When a component is changed, PMIIDR.Variant or PMIIDR.Revision is increased to ensure that software can differentiate between different revisions of the component. If this field is increased, PMIIDR.Revision should be set to `0b0000`.

Matches the PMU.PMPIDR2.REVISION field, if present.

This field has an implementation defined value.

Access to this field is **RO**.

Revision, bits [15:12]

Component minor revision.

PMIIDR.Variant and PMIIDR.Revision together form the revision number of the component, with this field being the least significant part.

When a component is changed, PMIIDR.Variant or PMIIDR.Revision is increased to ensure that software can differentiate between different revisions of the component. If PMIIDR.Variant field is increased, this field should be set to `0b0000`, otherwise the value in this field should be increased.

Matches the PMU.PMPIDR3.REVAND field, if present.

This field has an implementation defined value.

Access to this field is **RO**.

Implementer, bits [11:8, 6:0]

JEDEC-assigned JEP106 identifcation code of the designer of the component.

Bits [11:8] are the JEP106 bank identifier minus 1 and bits [6:0] are the JEP106 identification code for the designer of the component.

Note

For Arm Limited, the JEP106 bank is 5 and the JEP106 identification code is `0x3B`, meaning PMIIDR[11:0] has the value `0x43B`.

Bits [11:8] match the PMU.PMPIDR4.DES_2 field, if present.

Bits[6:0] match the {PMPIDR2.DES1, PMPIDR1.DES_0} fields if present.

This field has an implementation defined value.

The Implementer field is split as follows:

- Implementer[10:7] is PMIIDR[11:8].
- Implementer[6:0] is PMIIDR[6:0].

Access to this field is **RO**.

Bit [7]

Reserved, res0.

Otherwise:

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7	6 5 4 3 2 1 0
ProductID	Variant	Revision	Implementer[10:7]	RES0	Implementer[6:0]

ProductID, bits [31:20]

Part number, bits [11:0]. The part number is selected by the designer of the component.

Matches the PMU.PMPIDR1.PART_1, PMU.PMPIDR0.PART_0 fields if present.

This field has an implementation defined value.

Access to this field is **RO**.

Variant, bits [19:16]

Component major revision.

Defines either a variant of the component defined by PMIIDR.ProductID, or the major revision of the component.

When defining a major revision, PMIIDR.Variant and PMIIDR.Revision together form the revision number of the component, with this field being the most significant part.

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When a component is changed, PMIIDR.Variant or PMIIDR.Revision is increased to ensure that software can differentiate between different revisions of the component. If PMIIDR.Variant field is increased, this field should be set to `0b0000`, otherwise the value in this field should be increased.

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Access to this field is **RO**.

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Access to this field is **RO**.

Bit [7]

Reserved, res0.

Accessing PMIIDR

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT64 is implemented

Accessible at offset 0xE08 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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