

## TRCDEVTYPE, Device Type Register

The TRCDEVTYPE characteristics are:

### Purpose

Provides discovery information for the component. If the part number field is not recognized, a debugger can report the information that is provided by TRCDEVTYPE about the component instead.

For additional information, see the CoreSight Architecture Specification.

### Configuration

This register is present only when FEAT\_ETE is implemented and FEAT\_TRC\_EXT is implemented. Otherwise, direct accesses to TRCDEVTYPE are res0.

### Attributes

TRCDEVTYPE is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																								SUB			MAJOR				

#### Bits [31:8]

Reserved, res0.

#### SUB, bits [7:4]

Component sub-type.

SUB	Meaning
0b0001	When MAJOR == 0x3 (Trace source): Associated with a PE.

This field reads as 0x1.

#### MAJOR, bits [3:0]

Component major type.

MAJOR	Meaning
0b0011	Trace source.

Other values are defined by the CoreSight Architecture.

This field reads as 0x3.

## Accessing TRCDEVTYPE

External debugger accesses to this register are unaffected by the OS Lock.

**TRCDEVTYPE can be accessed through the external debug interface:**

Component	Offset	Instance
ETE	0xFCC	TRCDEVTYPE

This interface is accessible as follows:

- When !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.