ERRCIDR1, Component Identification Register 1

The ERRCIDR1 characteristics are:

Purpose

Provides discovery information about the component.

For more information, see 'About the Component Identification scheme'.

Configuration

Implementation of this register is optional.

ERRCIDR1 is implemented only as part of a memory-mapped group of error records.

Attributes

ERRCIDR1 is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

| RES0 | CLASS | PRMBL_1 |

Bits [31:8]

Reserved, res0.

CLASS, bits [7:4]

Component class.

CLASS	Meaning
0b1111	Generic peripheral with implementation defined register layout.

Other values are defined by the CoreSight Architecture.

This field reads as `0xF`.

PRMBL_1, bits [3:0]

Component identification preamble, segment 1.

Reads as `0b0000`.

Access to this field is **RO**.

Accessing ERRCIDR1

ERRCIDR1 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
RAS	`0xFF4`	ERRCIDR1

Accesses on this interface are **RO**.

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