

PMMIR, Performance Monitors Machine Identification Register

The PMMIR characteristics are:

Purpose

Describes Performance Monitors parameters specific to the implementation.

Configuration

This register is present only when FEAT_PMUv3_EXT is implemented and FEAT_PMUv3p4 is implemented. Otherwise, direct accesses to PMMIR are res0.

PMMIR is in the Core power domain.

Attributes

PMMIR is a:

- 64-bit register when FEAT_PMUv3_EXT64 is implemented
- 32-bit register otherwise

This register is part of the [PMU](#) block.

Field descriptions

When FEAT_PMUv3_EXT64 is implemented:

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
RES0				EDGE				THWIDTH				BUS_WIDTH				BUS_SLOTS				SLOTS											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:28]

Reserved, res0.

EDGE, bits [27:24]

PMU event edge detection. Indicates implementation of the FEAT_PMUv3_EDGE feature.

EDGE	Meaning
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0b0000	FEAT_PMUv3_EDGE is not implemented.
0b0001	FEAT_PMUv3_EDGE is implemented.

All other values are reserved.

This field has an implementation defined value.

Access to this field is **RO**.

THWIDTH, bits [23:20]

PMU.PMEVTYPER<n>.TH width. Indicates implementation of the FEAT_PMUv3_TH feature, and, if implemented, the size of the PMU.PMEVTYPER<n>.TH field.

THWIDTH	Meaning
0b0000	FEAT_PMUv3_TH is not implemented.
0b0001	1 bit. PMU.PMEVTYPER<n>.TH[11:1] are res0.
0b0010	2 bits. PMU.PMEVTYPER<n>.TH[11:2] are res0.
0b0011	3 bits. PMU.PMEVTYPER<n>.TH[11:3] are res0.
0b0100	4 bits. PMU.PMEVTYPER<n>.TH[11:4] are res0.
0b0101	5 bits. PMU.PMEVTYPER<n>.TH[11:5] are res0.
0b0110	6 bits. PMU.PMEVTYPER<n>.TH[11:6] are res0.
0b0111	7 bits. PMU.PMEVYPETR<n>.TH[11:7] are res0.
0b1000	8 bits. PMU.PMEVTYPER<n>.TH[11:8] are res0.
0b1001	9 bits. PMU.PMEVTYPER<n>.TH[11:9] are res0.
0b1010	10 bits. PMU.PMEVTYPER<n>.TH[11:10] are res0.

0b1011	11 bits. PMU.PMEVTYPEPER<n>.TH[11] is res0.
0b1100	12 bits.

All other values are reserved.

If FEAT_PMUv3_TH is not implemented, this field is zero.

Otherwise, the largest value that can be written to PMU.PMEVTYPEPER<n>.TH is $2^{(\text{PMMIR.THWIDTH})}$ minus one.

This field has an implementation defined value.

Access to this field is **RO**.

BUS_WIDTH, bits [19:16]

Bus width. Indicates the number of bytes each BUS_ACCESS event relates to. Encoded as $\text{Log}_2(\text{number of bytes})$, plus one.

BUS_WIDTH	Meaning
0b0000	The information is not available.
0b0011	Four bytes.
0b0100	8 bytes.
0b0101	16 bytes.
0b0110	32 bytes.
0b0111	64 bytes.
0b1000	128 bytes.
0b1001	256 bytes.
0b1010	512 bytes.
0b1011	1024 bytes.
0b1100	2048 bytes.

All other values are reserved.

Each transfer is up to this number of bytes. An access might be smaller than the bus width.

When this field is nonzero, each access counted by BUS_ACCESS is at most BUS_WIDTH bytes. An implementation might treat a wide bus as multiple narrower buses, such that a wide access on the bus increments the BUS_ACCESS counter by more than one.

This field has an implementation defined value.

Access to this field is **RO**.

BUS_SLOTS, bits [15:8]

Bus count. The largest value by which the BUS_ACCESS event might increment in a single BUS_CYCLES cycle.

When this field is nonzero, the largest value by which the BUS_ACCESS event might increment in a single BUS_CYCLES cycle is BUS_SLOTS.

If the bus count information is not available, this field will read as zero.

This field has an implementation defined value.

Access to this field is **RO**.

SLOTS, bits [7:0]

Operation width. The largest value by which the STALL_SLOT event might increment in a single cycle. If the STALL_SLOT event is not implemented, this field might read as zero.

This field has an implementation defined value.

Access to this field is **RO**.

Otherwise:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0				EDGE				THWIDTH				BUS WIDTH				BUS SLOTS				SLOTS											

Bits [31:28]

Reserved, res0.

EDGE, bits [27:24]

PMU event edge detection. Indicates implementation of the FEAT_PMUv3_EDGE feature.

EDGE	Meaning
0b0000	FEAT_PMUv3_EDGE is not implemented.
0b0001	FEAT_PMUv3_EDGE is implemented.

All other values are reserved.

This field has an implementation defined value.

Access to this field is **RO**.

THWIDTH, bits [23:20]

PMU.PMEVTYPER<n>.TH width. Indicates implementation of the FEAT_PMUv3_TH feature, and, if implemented, the size of the PMU.PMEVTYPER<n>.TH field.

THWIDTH	Meaning
0b0000	FEAT_PMUv3_TH is not implemented.
0b0001	1 bit. PMU.PMEVTYPER<n>.TH[11:1] are res0.
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0b1011	11 bits. PMU.PMEVTYPER<n>.TH[11] is res0.
0b1100	12 bits.

All other values are reserved.

If FEAT_PMUv3_TH is not implemented, this field is zero.

Otherwise, the largest value that can be written to PMU.PMEVTYPER<n>.TH is $2^{(\text{PMMIR.THWIDTH})}$ minus one.

This field has an implementation defined value.

Access to this field is **RO**.

BUS_WIDTH, bits [19:16]

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0b1100	2048 bytes.

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This field has an implementation defined value.

Access to this field is **RO**.

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When this field is nonzero, the largest value by which the BUS_ACCESS event might increment in a single BUS_CYCLES cycle is BUS_SLOTS.

If the bus count information is not available, this field will read as zero.

This field has an implementation defined value.

Access to this field is **RO**.

SLOTS, bits [7:0]

Operation width. The largest value by which the STALL_SLOT event might increment in a single cycle. If the STALL_SLOT event is not implemented, this field might read as zero.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing PMMIR

If the Core power domain is off or in a low-power state, access on this interface returns an Error.

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT64 is implemented or FEAT_PMUv3p9 is implemented

[63:0] Accessible at offset 0xE40 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

When FEAT_PMUv3_EXT32 is implemented and FEAT_PMUv3p9 is not implemented

[31:0] Accessible at offset 0xE40 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
 - Otherwise, accesses to this register are **RO**.
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