ERRDEVID, Device Configuration Register

The ERRDEVID characteristics are:

Purpose

Provides discovery information for the component.

Configuration

ERRDEVID is implemented only as part of a memory-mapped group of error records.

Attributes

ERRDEVID is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22	21	20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RES0	PFG	RES0	IRQCR	NUM

Bits [31:22]

Reserved, res0.

PFG, bit [21]
When RAS System Architecture v2 is implemented:

Common Fault Injection Mechanism. Describes whether any Common Fault Injection Mechanism registers are implemented in the same page as this register. Defined values are:

PFG	Meaning
0b0	Any Common Fault Injection Mechanism registers are implemented in the same page as this register.
0b1	Any Common Fault Injection Mechanism registers are implemented in a separate fault injection group page.

Accessing this field has the following behavior:

- When ERRDEVID is part of a fault injection group, access to this field is **RAZ/WI**.
- Otherwise, access to this field is **RO**.

Otherwise:

Reserved, RAZ.

Bit [20]

Reserved, res0.

IRQCR, bits [19:16]

Interrupt Control registers. Describes whether the interrupt control registers are implemented. Defined values are:

IRQCR	Meaning
0b0000	It is implementation defined whether any interrupt control registers are implemented.
0b0001	An implementation defined form of interrupt control registers are implemented.
0b0010	The recommended layout form of interrupt control registers are implemented, for simple interrupts.
0b0011	The recommended layout form of interrupt control registers are implemented, for message-signaled interrupts.
0b1111	Interrupt control registers are not implemented.

All other values are reserved.

Accessing this field has the following behavior:

- When ERRDEVID is part of a RAS agent that is not a System RAS agent, access to this field is **RAO/WI**.
- When ERRDEVID is part of a fault injection group, access to this field is **RAZ/WI**.
- Otherwise, access to this field is **RO**.

NUM, bits [15:0]

Highest numbered index of the error records in this group, plus one. Each implemented record is owned by a node. A node might own multiple records.

This manual describes a group of error records accessed via a standard 4KB memory-mapped peripheral. For a 4KB peripheral, up to 24 error records can be accessed if the Common Fault Injection Model is implemented, and up to 56 otherwise.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing ERRDEVID

ERRDEVID can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
RAS	`0xFC8`	ERRDEVID

Accesses on this interface are **RO**.

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