TRCVISSCTLR, ViewInst Start/Stop Control Register

The TRCVISSCTLR characteristics are:

Purpose

Use this to select, or read, the Single Address Comparators for the ViewInst start/stop function.

Configuration

External register TRCVISSCTLR bits [31:0] are architecturally mapped to AArch64 System register TRCVISSCTLR[31:0].

This register is present only when FEAT_ETE is implemented, FEAT_TRC_EXT is implemented and UInt(TRCIDR4.NUMACPAIRS) > 0. Otherwise, direct accesses to TRCVISSCTLR are res0.

Attributes

TRCVISSCTLR is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	
STOP[15]	STOP[14]	STOP[13]	STOP[12]	STOP[11]	STOP[10]	STOP[9]	STOP[8]	STOP[7]	STOP[6]	STOP[5]	S

STOP[<m>], bit [m+16], for m = 15 to 0

Selects whether Single Address Comparator <m> is used with the ViewInst start/stop function, for the purpose of stopping trace.

STOP[<m>]</m>	Meaning
0b0	The Single Address
	Comparator $< m >$, is not
	selected as a stop
	resource.
0b1	The Single Address
	Comparator $< m >$, is
	selected as a stop
	resource.

This bit is res0 if $m \ge 2 \tilde{A} - \frac{TRCIDR4}{NUMACPAIRS}$.

The reset behavior of this field is:

• On a Trace unit reset, this field resets to an architecturally unknown value.

START[< m>], bit [m], for m = 15 to 0

Selects whether Single Address Comparator <m> is used with the ViewInst start/stop function, for the purpose of starting trace.

START[<m>]</m>	Meaning
0b0	The Single Address
	Comparator $< m >$, is not
	selected as a start
	resource.
0b1	The Single Address
	Comparator $< m >$, is
	selected as a start
	resource.

This bit is res0 if $m \ge 2 \tilde{A} - TRCIDR4.NUMACPAIRS$.

The reset behavior of this field is:

• On a Trace unit reset, this field resets to an architecturally unknown value.

Accessing TRCVISSCTLR

Must be programmed if TRCIDR4.NUMACPAIRS > 0b0000.

For any 2 comparators selected for the ViewInst start/stop function, the comparator containing the lower address must be a lower numbered comparator.

Writes are constrained unpredictable if the trace unit is not in the Idle state.

TRCVISSCTLR can be accessed through the external debug interface:

Component	Offset	Instance		
ETE	0x088	TRCVISSCTLR		

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or ! IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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