GCSPR_EL1, Guarded Control Stack Pointer (EL1)

The GCSPR_EL1 characteristics are:

Purpose

Contains the Guarded control stack pointer at EL1.

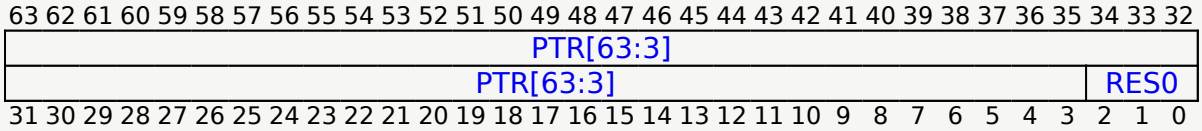
Configuration

This register is present only when FEAT_GCS is implemented. Otherwise, direct accesses to GCSPR_EL1 are undefined.

Attributes

GCSPR_EL1 is a 64-bit register.

Field descriptions



PTR[63:3], bits [63:3]

EL1 Guarded control stack pointer bits [63:3].

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [2:0]

Reserved, res0.

Accessing GCSPR_EL1

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, GCSPR_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0010	0b0101	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGRTR_EL2.nGCS_EL1 == '0'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        X[t, 64] = NVMem[0x8C0];
    else
        X[t, 64] = GCSPR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HCR_EL2.E2H == '1' then
        X[t, 64] = GCSPR_EL2;
    else
        X[t, 64] = GCSPR_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = GCSPR_EL1;
```

MSR GCSPR_EL1, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b0010	0b0101	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGWTR_EL2.nGCS_EL1 == '0'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        NVMem[0x8C0] = X[t, 64];
    else
        GCSPR_EL1 = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HCR_EL2.E2H == '1' then
        GCSPR_EL2 = X[t, 64];
    else
        GCSPR_EL1 = X[t, 64];
elsif PSTATE.EL == EL3 then
    GCSPR_EL1 = X[t, 64];
```

MRS <Xt>, GCSPR_EL12

op0	op1	CRn	CRm	op2
0b11	0b101	0b0010	0b0101	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101'
then
        X[t, 64] = NVMem[0x8C0];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
```

```
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD ==
'1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && SCR_EL3.GCSEn == '0'
then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0'
then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            X[t, 64] = GCSPR_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) &&
HCR_EL2.E2H == '1' then
        X[t, 64] = GCSPR_EL1;
    else
        UNDEFINED;
```

MSR GCSPR_EL12, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b101	0b0010	0b0101	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101'
then
        NVMem[0x8C0] = X[t, 64];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD ==
'1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && SCR_EL3.GCSEn == '0'
then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0'
then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
```

```
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            GCSPR_EL1 = X[t, 64];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) &&
HCR_EL2.E2H == '1' then
        GCSPR_EL1 = X[t, 64];
    else
        UNDEFINED;
```

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