

## TRCIDR12, ID Register 12

The TRCIDR12 characteristics are:

### Purpose

Returns the tracing capabilities of the trace unit.

### Configuration

External register TRCIDR12 bits [31:0] are architecturally mapped to AArch64 System register [TRCIDR12\[31:0\]](#).

This register is present only when FEAT\_ETE is implemented and FEAT\_TRC\_EXT is implemented. Otherwise, direct accesses to TRCIDR12 are res0.

### Attributes

TRCIDR12 is a 32-bit register.

### Field descriptions

|                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <a href="#">NUMCONDKEY</a> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

#### NUMCONDKEY, bits [31:0]

When **TRCIDR0.TRCCOND == 1**:

Indicates the number of conditional instruction right-hand keys. Conditional instruction tracing is not implemented in ETE and this field is reserved for other trace architectures. Allocated in other trace architectures.

#### Otherwise:

Reserved, res0.

### Accessing TRCIDR12

**TRCIDR12 can be accessed through the external debug interface:**

| Component | Offset | Instance |
|-----------|--------|----------|
| ETE       | 0x190  | TRCIDR12 |

This interface is accessible as follows:

- When OSLockStatus() or !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

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