ID_AFR0_EL1, AArch32 Auxiliary Feature Register 0

The ID_AFR0_EL1 characteristics are:

Purpose

Provides information about the implementation defined features of the PE in AArch32 state.

Must be interpreted with the Main ID Register, MIDR_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

Configuration

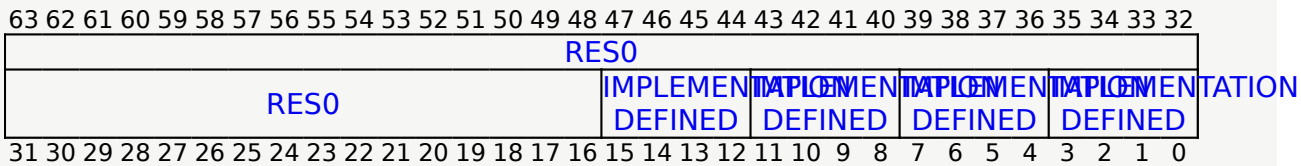
AArch64 System register ID_AFR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_AFR0[31:0].

Attributes

ID_AFR0_EL1 is a 64-bit register.

Field descriptions

When AArch32 is supported:



Bits [63:16]

Reserved, res0.

IMPLEMENTATION DEFINED, bits [15:12]

implementation defined.

IMPLEMENTATION DEFINED, bits [11:8]

implementation defined.

IMPLEMENTATION DEFINED, bits [7:4]

implementation defined.

IMPLEMENTATION DEFINED, bits [3:0]

implementation defined.

Otherwise:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
UNKNOWN
UNKNOWN
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits [63:0]

Reserved, unknown.

Accessing ID_AFR0_EL1

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, ID_AFR0_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0001	0b011

```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AFR0_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = ID_AFR0_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ID_AFR0_EL1;
```

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