PMCNTEN, Performance Monitors Count Enable register

The PMCNTEN characteristics are:

Purpose

Enables the Cycle Count Register, PMU.PMCCNTR_EL0, and any implemented event counters PMEVCNTR<n>.

Configuration

External register PMCNTEN bits [63:0] are architecturally mapped to AArch64 System register PMCNTENSET_EL0[63:0] when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMCNTEN bits [63:0] are architecturally mapped to AArch64 System register PMCNTENCLR_EL0[63:0] when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMCNTEN bits [31:0] are architecturally mapped to AArch32 System register PMCNTENSET[31:0].

External register PMCNTEN bits [31:0] are architecturally mapped to AArch32 System register PMCNTENCLR[31:0].

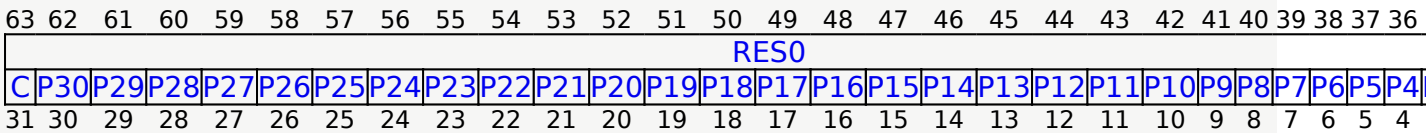
This register is present only when FEAT_PMUv3_EXT64 is implemented. Otherwise, direct accesses to PMCNTEN are res0.

Attributes

PMCNTEN is a 64-bit register.

This register is part of the PMU block.

Field descriptions



Bits [63:33]

Reserved, res0.

F0, bit [32]
When FEAT_PMUv3_ICNTR is implemented:

PMU.PMICNTR_EL0 counter enable. Enables the instruction counter.

F0	Meaning
0b0	PMU.PMICNTR_EL0 disabled.
0b1	PMU.PMICNTR_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

C, bit [31]

PMU.PMCCNTR_EL0 enable. Enables the cycle counter register. Possible values are:

C	Meaning
0b0	PMU.PMCCNTR_EL0 is disabled.
0b1	PMU.PMCCNTR_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

P<n>, bit [n], for n = 30 to 0

Event counter enable for PMU.PMEVCNTR<n>_EL0.

If PMU.PMCFGR.N is less than 31, bits [30:PMU.PMCFGR.N] are RAZ/WI.

P<n>	Meaning
0b0	PMU.PMEVCNTR<n>_EL0 is disabled.
0b1	PMU.PMEVCNTR<n>_EL0 is enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMCNTEN

Accesses to this register use the following encodings:

Accessible at offset 0xC10 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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