TRCIDR4, ID Register 4

The TRCIDR4 characteristics are:

Purpose

Returns the tracing capabilities of the trace unit.

Configuration

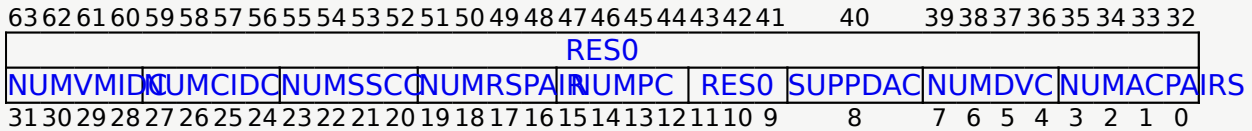
AArch64 System register TRCIDR4 bits [31:0] are architecturally mapped to External register TRCIDR4[31:0].

This register is present only when FEAT_ETE is implemented and FEAT_TRC_SR is implemented. Otherwise, direct accesses to TRCIDR4 are undefined.

Attributes

TRCIDR4 is a 64-bit register.

Field descriptions



Bits [63:32]

Reserved, res0.

NUMVMIDC, bits [31:28]

Indicates the number of Virtual Context Identifier Comparators that are available for tracing.

NUMVMIDC	Meaning
0b0000	No Virtual Context Identifier Comparators are available.
0b0001	The implementation has one Virtual Context Identifier Comparator.

0b0010	The implementation has two Virtual Context Identifier Comparators.
0b0011	The implementation has three Virtual Context Identifier Comparators.
0b0100	The implementation has four Virtual Context Identifier Comparators.
0b0101	The implementation has five Virtual Context Identifier Comparators.
0b0110	The implementation has six Virtual Context Identifier Comparators.
0b0111	The implementation has seven Virtual Context Identifier Comparators.
0b1000	The implementation has eight Virtual Context Identifier Comparators.

All other values are reserved.

NUMCIDC, bits [27:24]

Indicates the number of Context Identifier Comparators that are available for tracing.

NUMCIDC	Meaning
0b0000	No Context Identifier Comparators are available.
0b0001	The implementation has one Context Identifier Comparator.
0b0010	The implementation has two Context Identifier Comparators.
0b0011	The implementation has three Context Identifier Comparators.
0b0100	The implementation has four Context Identifier Comparators.
0b0101	The implementation has five Context Identifier Comparators.
0b0110	The implementation has six Context Identifier Comparators.

0b0111	The implementation has seven Context Identifier Comparators.
0b1000	The implementation has eight Context Identifier Comparators.

All other values are reserved.

NUMSSCC, bits [23:20]

Indicates the number of Single-shot Comparator Controls that are available for tracing.

NUMSSCC	Meaning
0b0000	No Single-shot Comparator Controls are available.
0b0001	The implementation has one Single-shot Comparator Control.
0b0010	The implementation has two Single-shot Comparator Controls.
0b0011	The implementation has three Single-shot Comparator Controls.
0b0100	The implementation has four Single-shot Comparator Controls.
0b0101	The implementation has five Single-shot Comparator Controls.
0b0110	The implementation has six Single-shot Comparator Controls.
0b0111	The implementation has seven Single-shot Comparator Controls.
0b1000	The implementation has eight Single-shot Comparator Controls.

All other values are reserved.

NUMRSPAIR, bits [19:16]

Indicates the number of resource selector pairs that are available for tracing.

NUMRSPAIR	Meaning

0b0000	The implementation has zero resource selectors.
0b0001	The implementation has two resource selector pairs.
0b0010	The implementation has three resource selector pairs.
0b0011	The implementation has four resource selector pairs.
0b0100	The implementation has five resource selector pairs.
0b0101	The implementation has six resource selector pairs.
0b0110	The implementation has seven resource selector pairs.
0b0111	The implementation has eight resource selector pairs.
0b1000	The implementation has nine resource selector pairs.
0b1001	The implementation has ten resource selector pairs.
0b1010	The implementation has eleven resource selector pairs.
0b1011	The implementation has twelve resource selector pairs.
0b1100	The implementation has thirteen resource selector pairs.
0b1101	The implementation has fourteen resource selector pairs.
0b1110	The implementation has fifteen resource selector pairs.
0b1111	The implementation has sixteen resource selector pairs.

All other values are reserved.

NUMPC, bits [15:12]

Indicates the number of PE Comparator Inputs that are available for tracing.

NUMPC	Meaning
0b0000	No PE Comparator Inputs are available.
0b0001	The implementation has one PE Comparator Input.
0b0010	The implementation has two PE Comparator Inputs.
0b0011	The implementation has three PE Comparator Inputs.
0b0100	The implementation has four PE Comparator Inputs.
0b0101	The implementation has five PE Comparator Inputs.
0b0110	The implementation has six PE Comparator Inputs.
0b0111	The implementation has seven PE Comparator Inputs.
0b1000	The implementation has eight PE Comparator Inputs.

All other values are reserved.

Bits [11:9]

Reserved, res0.

SUPPDAC, bit [8]
When TRCIDR4.NUMACPAIRS != 0b0000:

Indicates whether data address comparisons are implemented. Data address comparisons are not implemented in ETE and are reserved for other trace architectures. Allocated in other trace architectures.

SUPPDAC	Meaning
0b0	Data address comparisons not implemented.
0b1	Data address comparisons implemented.

This field reads as 0.

Otherwise:

Reserved, res0.

NUMDVC, bits [7:4]

Indicates the number of data value comparators. Data value comparators are not implemented in ETE and are reserved for other trace architectures. Allocated in other trace architectures.

NUMDVC	Meaning
0b0000	No data value comparators implemented.
0b0001	One data value comparator implemented.
0b0010	Two data value comparators implemented.
0b0011	Three data value comparators implemented.
0b0100	Four data value comparators implemented.
0b0101	Five data value comparators implemented.
0b0110	Six data value comparators implemented.
0b0111	Seven data value comparators implemented.
0b1000	Eight data value comparators implemented.

All other values are reserved.

This field reads as 0b0000.

NUMACPAIRS, bits [3:0]

Indicates the number of Address Comparator pairs that are available for tracing.

NUMACPAIRS	Meaning
0b0000	No Address Comparator pairs are available.
0b0001	The implementation has one Address Comparator pair.
0b0010	The implementation has two Address Comparator pairs.
0b0011	The implementation has three Address Comparator pairs.

0b0100	The implementation has four Address Comparator pairs.
0b0101	The implementation has five Address Comparator pairs.
0b0110	The implementation has six Address Comparator pairs.
0b0111	The implementation has seven Address Comparator pairs.
0b1000	The implementation has eight Address Comparator pairs.

All other values are reserved.

Accessing TRCIDR4

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, TRCIDR4

op0	op1	CRn	CRm	op2
0b10	0b001	0b0000	0b1100	0b111

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && CPTR_EL3.TTA == '1' then
        UNDEFINED;
    elsif CPACR_EL1.TTA == '1' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && CPTR_EL2.TTA == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.TRCID == '1'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TTA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
```

```
        X[t, 64] = TRCIDR4;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && CPTR_EL3.TTA == '1' then
        UNDEFINED;
    elsif CPTR_EL2.TTA == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TTA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = TRCIDR4;
elsif PSTATE.EL == EL3 then
    if CPTR_EL3.TTA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = TRCIDR4;
```

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