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Pseu

FMOV (scalar, immediate)

Floating-point move immediate (scalar). This instruction copies a floating-point immediate constant into the SIMD&FP destination register.

Depending on the settings in the *CPACR_EL1*, *CPTR_EL2*, and *CPTR_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 0 0 1 1 1 1 1 0 ftype 1 imm8 1 0 0 0 0 0 0 0 Rd
```

```
Half-precision (ftype == 11)
(FEAT_FP16)
```

```
FMOV <Hd>, #<imm>
```

Single-precision (ftype == 00)

```
FMOV <Sd>, #<imm>
```

Double-precision (ftype == 01)

```
FMOV <Dd>, #<imm>
if ftype == '10' || (ftype == '11' && !IsFeatureImplemented(FEAT_FP16))
integer d = UInt(Rd);
constant integer datasize = 8 << UInt(ftype EOR '10');
bits(datasize) imm = VFPExpandImm(imm8, datasize);</pre>
```

Assembler Symbols

| <dd></dd> | Is the 64-bit name of the SIMD&FP | destination register, |
|-----------|---|-----------------------|
| | 1 | |

encoded in the "Rd" field.

<Hd> Is the 16-bit name of the SIMD&FP destination register,

encoded in the "Rd" field.

<Sd> Is the 32-bit name of the SIMD&FP destination register,

encoded in the "Rd" field.

<imm> Is a signed floating-point constant with 3-bit exponent and

normalized 4 bits of precision, encoded in the "imm8" field.

For details of the range of constants available and the encoding of <imm>, see *Modified immediate constants in*

A64 floating-point instructions.

Operation

```
CheckFPEnabled64();
V[d, datasize] = imm;
```

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