PM, PMU Exception Mask

The PM characteristics are:

Purpose

Allows access to the PMU exception Mask bit.

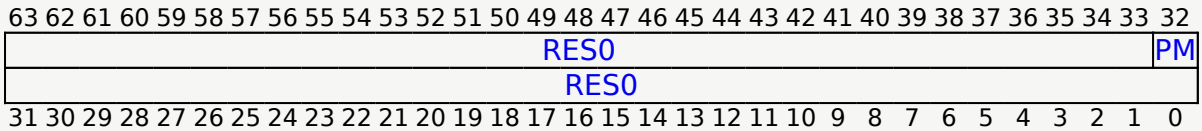
Configuration

This register is present only when FEAT_SEBEP is implemented. Otherwise, direct accesses to PM are undefined.

Attributes

PM is a 64-bit register.

Field descriptions



Bits [63:33]

Reserved, res0.

PM, bit [32]

PMU Exception Mask.

PM	Meaning
0b0	Does not cause the PMU exception to be masked.
0b1	Causes the PMU exception to be masked.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [31:0]

Reserved, res0.

Accessing PM

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, PM

op0	op1	CRn	CRm	op2
0b11	0b000	0b0100	0b0011	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    X[t, 64] = Zeros(31):PSTATE.PM:Zeros(32);
elsif PSTATE.EL == EL2 then
    X[t, 64] = Zeros(31):PSTATE.PM:Zeros(32);
elsif PSTATE.EL == EL3 then
    X[t, 64] = Zeros(31):PSTATE.PM:Zeros(32);
```

MSR PM, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b0100	0b0011	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    PSTATE.PM = X[t, 64]<32>;
elsif PSTATE.EL == EL2 then
    PSTATE.PM = X[t, 64]<32>;
elsif PSTATE.EL == EL3 then
    PSTATE.PM = X[t, 64]<32>;
```

MSR PM, #<imm>

op0	op1	CRn	CRm	op2
0b00	0b001	0b0100	0b001x	0b000

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94