TRBIDR_EL1, Trace Buffer ID Register

The TRBIDR_EL1 characteristics are:

Purpose

Describes constraints on using the Trace Buffer Unit to an external debugger.

Configuration

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBIDR_EL1 are res0.

TRBIDR_EL1 is in the Core power domain.

Attributes

TRBIDR_EL1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																				EA				RES0		RAO	P	Align			

Bits [63:12]

Reserved, res0.

EA, bits [11:8]
From Armv9.3:

External Abort handling. Describes how the PE manages External aborts on writes made by the Trace Buffer Unit to the trace buffer.

EA	Meaning
0b0001	The PE ignores External aborts on writes made by the Trace Buffer Unit.
0b0010	The External abort generates an asynchronous SError exception at the PE.

All other values are reserved.

This field has an implementation defined value.

Access to this field is **RO**.

Otherwise:

Reserved, res0.

Bits [7:6]

Reserved, res0.

Bit [5]

Reserved, RAO.

P, bit [4]

This field reads as an unknown value.

Align, bits [3:0]

Defines the minimum alignment constraint for writes to TRBPTR_EL1 and TRBTRG_EL1.

Align	Meaning
0b0000	Byte.
0b0001	Halfword.
0b0010	Word.
0b0011	Doubleword.
0b0100	16 bytes.
0b0101	32 bytes.
0b0110	64 bytes.
0b0111	128 bytes.
0b1000	256 bytes.
0b1001	512 bytes.
0b1010	1KB.
0b1011	2KB.

All other values are reserved.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing TRBIDR_EL1

TRBIDR_EL1 can be accessed through the external debug interface:

Component	Offset	Instance
TRBE	0x030	TRBIDR_EL1

This interface is accessible as follows:

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalTraceBufferAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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