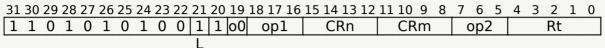
<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	<u>Index by</u>
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<b>Encoding</b>

Sh Pseu

## **MRS**

Move System Register to general-purpose register allows the PE to read an AArch64 System register into a general-purpose register.



```
MRS <Xt>, (<systemreg> | S<op0>_<op1>_<Cn>_<cm>_<op2>)
```

```
AArch64.CheckSystemAccess('1':00, op1, CRn, CRm, op2, Rt, L);
integer t = UInt(Rt);
integer sys_op0 = 2 + UInt(o0);
integer sys_op1 = UInt(op1);
integer sys_op2 = UInt(op2);
integer sys_crn = UInt(CRn);
integer sys_crm = UInt(CRm);
```

## **Assembler Symbols**

<Xt> Is the 64-bit name of the general-purpose destination

register, encoded in the "Rt" field.

<systemreg> Is a System register name, encoded in the

"o0:op1:CRn:CRm:op2".

The System register names are defined in 'AArch64 System

Registers' in the System Register XML.

<0q0>

Is an unsigned immediate, encoded in "o0":

о0	<op0></op0>		
0	2		
1	3		

<op1> Is a 3-bit unsigned immediate, in the range 0 to 7, encoded

in the "op1" field.

<Cn> Is a name 'Cn', with 'n' in the range 0 to 15, encoded in the

"CRn" field.

<Cm> Is a name 'Cm', with 'm' in the range 0 to 15, encoded in the

"CRm" field.

<op2> Is a 3-bit unsigned immediate, in the range 0 to 7, encoded

in the "op2" field.

## Operation

AArch64.SysRegRead(sys\_op0, sys\_op1, sys\_crn, sys\_crm, sys\_op2, t);

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Internal version only: is a v33.64, AdvSIMD v29.12, pseudocode no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56

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