

TRCACVR<n>, Address Comparator Value Register <n>, n = 0 - 15

The TRCACVR<n> characteristics are:

Purpose

Contains the address value.

Configuration

External register TRCACVR<n> bits [63:0] are architecturally mapped to AArch64 System register [TRCACVR<n>\[63:0\]](#).

This register is present only when FEAT_ETE is implemented, FEAT_TRC_EXT is implemented and $\text{UInt}(\text{TRCIDR4.NUMACPAIRS}) * 2 > n$. Otherwise, direct accesses to TRCACVR<n> are res0.

Attributes

TRCACVR<n> is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADDRESS																															
ADDRESS																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ADDRESS, bits [63:0]

Address Value.

The Address Comparators can support implementations that use multiple address widths. When the trace unit compares the ADDRESS field with an address that has a width less than this field, then the address must be zero-extended to the ADDRESS field width. The trace unit then compares all implemented bits. For example, in a system that supports both 32-bit and 64-bit addresses, when the PE is in AArch32 state the comparator must zero-extend the 32-bit address and compare against the full 64 bits that are stored in the TRCACVR<n>. This requires that the trace analyzer always programs all implemented bits of the TRCACVR<n>.

The result of writing a value other than all zeros or all ones to ADDRESS at bits[63:P] is an unknown value, where P is defined as the maximum virtual address size supported by the PE.

The result of writing a value of all zeros or all ones to ADDRESS at bits[63:P] is the written value, and a read of the register returns the written value.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Accessing TRCACVR<n>

Must be programmed if any of the following are true:

- [TRCBBCTLR](#).RANGE[n/2] == 1.
- [TRCRSCTLR<a>](#).GROUP == 0b0100 and [TRCRSCTLR<a>](#).SAC[n] == 1.
- [TRCRSCTLR<a>](#).GROUP == 0b0101 and [TRCRSCTLR<a>](#).ARC[n/2] == 1.
- [TRCVIIECTLR](#).EXCLUDE[n/2] == 1.
- [TRCVIIECTLR](#).INCLUDE[n/2] == 1.
- [TRCVISSCTLR](#).START[n] == 1.
- [TRCVISSCTLR](#).STOP[n] == 1.
- TRCSSCCR<>.ARC[n/2] == 1.
- TRCSSCCR<>.SAC[n] == 1.
- [TRCOCTLR](#).RANGE[n/2] == 1.

Writes are constrained unpredictable if the trace unit is not in the Idle state.

TRCACVR<n> can be accessed through the external debug interface:

Component	Offset	Instance
ETE	0x400 + (8 * n)	TRCACVR<n>

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or !IsTraceCorePowered(), accesses to this register generate an error response.
 - Otherwise, accesses to this register are **RW**.
-

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.