PMOVS, Performance Monitors Overflow Flag Status register

The PMOVS characteristics are:

Purpose

The unsigned overflow flags for the Cycle Count Register, PMU.PMCCNTR_EL0, and each of the implemented event counters PMEVCNTR<n>.

Configuration

External register PMOVS bits [63:0] are architecturally mapped to AArch64 System register PMOVSSET_EL0[63:0] when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMOVS bits [63:0] are architecturally mapped to AArch64 System register PMOVSCLR_EL0[63:0] when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMOVS bits [31:0] are architecturally mapped to AArch32 System register PMOVSSET[31:0].

External register PMOVS bits [31:0] are architecturally mapped to AArch32 System register PMOVSR[31:0].

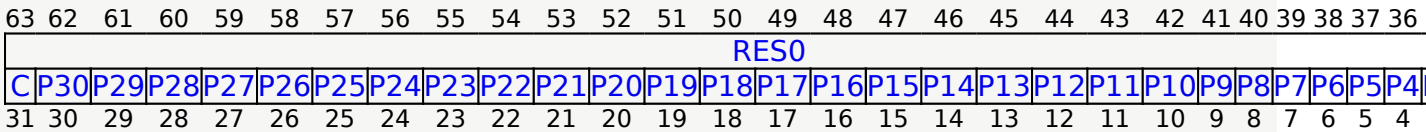
This register is present only when FEAT_PMUv3_EXT64 is implemented. Otherwise, direct accesses to PMOVS are res0.

Attributes

PMOVS is a 64-bit register.

This register is part of the PMU block.

Field descriptions



Bits [63:33]

Reserved, res0.

F0, bit [32]
When FEAT_PMUv3_ICNTR is implemented:

PMU.PMICNTR_EL0 unsigned overflow flag.

F0	Meaning
0b0	PMU.PMICNTR_EL0 has not overflowed.
0b1	PMU.PMICNTR_EL0 has overflowed.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

C, bit [31]

Cycle counter unsigned overflow flag.

C	Meaning
0b0	The cycle counter has not overflowed since this bit was last cleared.
0b1	The cycle counter has overflowed since this bit was last cleared.

PMU.PMCR_EL0.LC controls whether an overflow is detected from unsigned overflow of PMU.PMCCNTR_EL0[31:0] or unsigned overflow of PMU.PMCCNTR_EL0[63:0].

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

P<n>, bit [n], for n = 30 to 0

Event counter unsigned overflow bit for PMU.PMEVCNTR<n>_EL0.

If PMU.PMCFGR.N is less than 31, bits [30:PMU.PMCFGR.N] are RAZ/WI.

P<n>	Meaning
0b0	PMU.PMEVCNTR<n>_EL0 has not overflowed since this bit was last cleared.
0b1	PMU.PMEVCNTR<n>_EL0 has overflowed since this bit was last cleared.

If FEAT_PMUv3p5 is implemented, MDCR_EL2.HLP and PMU.PMCR_EL0.LP control whether an overflow is detected from unsigned overflow of PMU.PMEVCNTR<n>_EL0[31:0] or unsigned overflow of PMU.PMEVCNTR<n>_EL0[63:0].

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMOVS

Accesses to this register use the following encodings:

Accessible at offset 0xC90 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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