	<u>Sh</u>
[<u>Pseu</u>

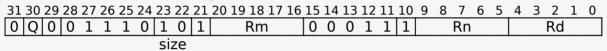
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ORR (vector, register)

Bitwise inclusive OR (vector, register). This instruction performs a bitwise OR between the two source SIMD&FP registers, and writes the result to the destination SIMD&FP register.

Depending on the settings in the *CPACR_EL1*, *CPTR_EL2*, and *CPTR_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

This instruction is used by the alias MOV (vector).



```
ORR <Vd>.<T>, <Vn>.<T>, <Vm>.<T>
integer d = UInt(Rd);
integer n = UInt(Rn);
integer m = UInt(Rm);
constant integer datasize = 64 << UInt(Q);</pre>
```

Assembler Symbols

<Vd> Is the name of the SIMD&FP destination register, encoded

in the "Rd" field.

<T> Is an arrangement specifier, encoded in "Q":

Q	<t></t>	
0	8B	
1	16B	

<Vn> Is the name of the first SIMD&FP source register, encoded

in the "Rn" field.

<Vm> Is the name of the second SIMD&FP source register,

encoded in the "Rm" field.

Alias Conditions

Alias	Is preferred when
MOV (vector)	Rm == Rn

Operation

```
CheckFPAdvSIMDEnabled64();
bits(datasize) operand1 = V[n, datasize];
bits(datasize) operand2 = V[m, datasize];
bits(datasize) result;
```

```
result = operand1 OR operand2;

<u>V</u>[d, datasize] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no_diffs_2023_09_RC2,\ sve\ v2023-06_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$

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