

PMSSCR_EL1, Performance Monitors Snapshot Status and Capture Register

The PMSSCR_EL1 characteristics are:

Purpose

Holds status information about the captured counters and provides a mechanism for software to initiate a sample.

Configuration

This register is present only when FEAT_PMUv3_SS is implemented. Otherwise, direct accesses to PMSSCR_EL1 are res0.

Attributes

PMSSCR_EL1 is a 64-bit register.

This register is part of the [PMU](#) block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															NC
RES0																															SS
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:33]

Reserved, res0.

NC, bit [32]

No Capture. Indicates whether the PMU counters have been captured.

NC	Meaning
0b0	PMU counters captured.
0b1	PMU counters not captured.

The reset behavior of this field is:

- On a Warm reset, this field resets to 1.

Bits [31:1]

Reserved, res0.

SS, bit [0]

Snapshot Capture and Status.

SS	Meaning
0b0	On a read, the Capture event has completed.
0b1	On a read, the Capture event has not completed. On a write, request a Capture event.

A write of 0 to this field is ignored.

It is constrained unpredictable whether a Capture event has completed if this field is modified when the Capture event is ongoing.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

- When SoftwareLockStatus(), access to this field is **RO**.
- When !PMUCaptureEventEnabled(), access to this field is **RO**.
- Otherwise, access to this field is **RW**.

Accessing PMSSCR_EL1

Accesses to this register use the following encodings:

Accessible at offset 0xE30 from PMU

- When !AllowExternalPMSSAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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