

## MVN

Bitwise NOT (vector). This instruction reads each vector element from the source SIMD&FP register, places the inverse of each value into a vector, and writes the vector to the destination SIMD&FP register.

Depending on the settings in the [CPACR\\_EL1](#), [CPTR\\_EL2](#), and [CPTR\\_EL3](#) registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

This is an alias of [NOT](#). This means:

- The encodings in this description are named to match the encodings of [NOT](#).
- The description of [NOT](#) gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Q	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	Rn				Rd					

**MVN** [<Vd>](#) .[<T>](#) , [<Vn>](#) .[<T>](#)

is equivalent to

[NOT](#) [<Vd>](#) .[<T>](#) , [<Vn>](#) .[<T>](#)

and is always the preferred disassembly.

### Assembler Symbols

[<Vd>](#) Is the name of the SIMD&FP destination register, encoded in the "Rd" field.

[<T>](#) Is an arrangement specifier, encoded in "Q":

Q	<a href="#">&lt;T&gt;</a>
0	8B
1	16B

[<Vn>](#) Is the name of the SIMD&FP source register, encoded in the "Rn" field.

### Operation

The description of [NOT](#) gives the operational pseudocode for this instruction.

**Operational information**

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

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<a href="#">Base Instructions</a>	<a href="#">SIMD&amp;FP Instructions</a>	<a href="#">SVE Instructions</a>	<a href="#">SME Instructions</a>	<a href="#">Index by Encoding</a>
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[Sh](#)  
[Pseu](#)

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