FMOV (immediate, predicated)

Move 8-bit floating-point immediate to vector elements (predicated)

Move a floating-point immediate into each active element in the destination vector. Inactive elements in the destination vector register remain unmodified.

This is an alias of FCPY. This means:

- The encodings in this description are named to match the encodings of FCPY.
- The description of FCPY gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31 30 29 28 27 26 25 24	23 22	21 20	19 18 17 16	15 14 13	12 11 10 9 8 7 6 5	4 3 2 1 0
0 0 0 0 0 1 0 1	size	0 1	Pg	1 1 0	imm8	Zd

FMOV `<Zd>.<T>`, `<Pg>/M`, `#<const>`

is equivalent to

FCPY `<Zd>.<T>`, `<Pg>/M`, `#<const>`

and is always the preferred disassembly.

Assembler Symbols

<Zd>   Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T>

Is the size specifier, encoded in "size":

size	<T>
00	RESERVED
01	H
10	S
11	D

<Pg>   Is the name of the governing scalable predicate register, encoded in the "Pg" field.

<const>	Is a floating-point immediate value expressible as $\pm n \cdot 16 \times 2^r$, where n and r are integers such that $16 \leq n \leq 31$ and $-3 \leq r \leq 4$, i.e. a normalized binary floating-point encoding with 1 sign bit, 3-bit exponent, and 4-bit fractional part, encoded in the "imm8" field.

Operation

The description of [FCPY](#) gives the operational pseudocode for this instruction.

Operational information

This instruction might be immediately preceded in program order by a MOVPRFX instruction. The MOVPRFX instruction must conform to all of the following requirements, otherwise the behavior of the MOVPRFX and this instruction is unpredictable:

- The MOVPRFX instruction must be unpredicated, or be predicated using the same governing predicate register and source element size as this instruction.
- The MOVPRFX instruction must specify the same destination register as this instruction.
- The destination register must not refer to architectural register state referenced by any other source operand register of this instruction.