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SYSP

128-bit System instruction.

This instruction is used by the alias **TLBIP**.

System

(FEAT SYSINSTR128)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
CRm
                                       op2
```

SYSP #<op1>, <Cn>, <Cm>, #<op2>{, <Xt1>, <Xt2>}

```
if !IsFeatureImplemented(FEAT_SYSINSTR128) then UNDEFINED;
if Rt<0> == '1' && Rt != '11111' then UNDEFINED;
AArch64.CheckSystemAccess('01', op1, CRn, CRm, op2, Rt, L);
integer t = UInt(Rt);
integer t2 = if t == 31 then 31 else <u>WInt</u>(Rt) + 1;
integer sys_op1 = UInt(op1);
integer sys_op2 = \underline{UInt}(op2);
integer sys_crn = UInt(CRn);
integer sys_crm = UInt(CRm);
```

Assembler Symbols

<op1></op1>	Is a 3-bit unsigned immediate, in the range 0 to 6, encoded in the "op1" field.
<cn></cn>	Is a name 'Cn', with 'n' in the range 8 to 9, encoded in the "CRn" field.
<cm></cm>	Is a name 'Cm', with 'm' in the range 0 to 7, encoded in the "CRm" field.
<op2></op2>	Is a 3-bit unsigned immediate, in the range 0 to 7, encoded in the "op2" field.
<xt1></xt1>	Is the 64-bit name of the first optional general-purpose source register, defaulting to '11111', encoded in the "Rt" field.
<xt2></xt2>	Is the 64-bit name of the second optional general-purpose source register, defaulting to '11111', encoded as "Rt" $+1$. Defaults to '11111' if "Rt" $=$ '11111'.

Alias Conditions

Alias Is preferred when

```
TLBIP CRn == '100x' && SysOp(op1, CRn, CRm, op2) == Sys_TLBIP
```

Operation

```
AArch64.SysInstr128(1, sys_op1, sys_crn, sys_crm, sys_op2, t, t2);
```

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