PMITCTRL, Performance Monitors Integration mode Control register

The PMITCTRL characteristics are:

Purpose

Enables the Performance Monitors to switch from default mode into integration mode, where test software can control directly the inputs and outputs of the PE, for integration testing or topology detection.

Configuration

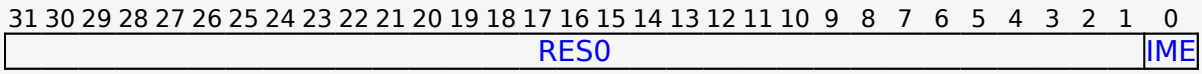
This register is present only when FEAT_PMUv3_EXT32 is implemented and an implementation implements PMITCTRL. Otherwise, direct accesses to PMITCTRL are res0.

Attributes

PMITCTRL is a 32-bit register.

This register is part of the PMU block.

Field descriptions



Bits [31:1]

Reserved, res0.

IME, bit [0]

Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is implementation defined.

IME	Meaning
0b0	Normal operation.
0b1	Integration mode enabled.

The following resets apply:

- If the register is implemented in the Core power domain:
  - On a Cold reset, this field resets to 0.
  - On an External debug reset, the value of this field is unchanged.
  - On a Warm reset, the value of this field is unchanged.
- If the register is implemented in the External debug power domain:
  - On a Cold reset, the value of this field is unchanged.
  - On an External debug reset, this field resets to 0.
  - On a Warm reset, the value of this field is unchanged.

Accessing PMITCTRL

Accesses to this register use the following encodings:

```
Accessible at offset 0xF00 from PMU
```

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus(), accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and ! SoftwareLockStatus(), accesses to this register are **RW**.
- Otherwise, accesses to this register are **IMPDEF**.

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