

# PMPIDR0, Performance Monitors Peripheral Identification Register 0

The PMPIDR0 characteristics are:

## Purpose

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

## Configuration

This register is present only when FEAT\_PMUv3\_EXT is implemented and an implementation implements PMPIDR0. Otherwise, direct accesses to PMPIDR0 are res0.

If FEAT\_DoPD is implemented, this register is in the Core power domain. If FEAT\_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

## Attributes

PMPIDR0 is a 32-bit register.

This register is part of the [PMU](#) block.

## Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																PART 0															

### Bits [31:8]

Reserved, res0.

### PART\_0, bits [7:0]

Part number, least significant byte.

This field has an implementation defined value.

Access to this field is **RO**.

## Accessing PMPIDR0

Accesses to this register use the following encodings:

Accessible at offset 0xFE0 from PMU

- When FEAT\_DoPD is implemented and !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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