

## SPMEVFILT2R<n>\_EL0, System Performance Monitors Event Filter Control Register 2, n = 0 - 63

The SPMEVFILT2R<n>\_EL0 characteristics are:

### Purpose

With [SPMEVTYPER<n>\\_EL0](#) and [SPMEVFILTR<n>\\_EL0](#), configures when event counter [SPMEVCNTR<n>\\_EL0](#) in System PMU <s> increments.

The contents of this register are implementation defined. For more information, see [SPMEVTYPER<n>\\_EL0](#).

### Configuration

This register is present only when FEAT\_SPMU is implemented. Otherwise, direct accesses to SPMEVFILT2R<n>\_EL0 are undefined.

### Attributes

SPMEVFILT2R<n>\_EL0 is a 64-bit register.

### Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
IMPLEMENTATION DEFINED																															
IMPLEMENTATION DEFINED																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

#### IMPLEMENTATION DEFINED, bits [63:0]

implementation defined.

### Accessing SPMEVFILT2R<n>\_EL0

To access SPMEVFILT2R<n>\_EL0 for System PMU <s>, set [SPMSELR\\_EL0](#).SYSPMUSEL to s and [SPMSELR\\_EL0](#).BANK to n[5:4].

SPMEVFILT2R<n>\_EL0 reads-as-zero and ignores writes if event counter <n> is not implemented by System PMU <s>.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, SPMEVFILT2R<m>\_EL0 ; Where m = 0-15

op0	op1	CRn	CRm	op2
0b10	0b011	0b1110	0b011:m[3]	m[2:0]

```
integer m = UInt(CRm<0>:op2<2:0>);

if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
    when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
    && IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
    SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
    && IsFeatureImplemented(FEAT_FGT2) &&
    HDFGRTR2_EL2.nSPMEVTYPErN_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
        SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
        (UInt(SPMSELR_EL0.BANK) * 16) + m];
    elseif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
        && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
        when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
            UNDEFINED;
        elseif EL2Enabled() &&
        IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
        SCR_EL3.FGTEn2 == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() &&
        IsFeatureImplemented(FEAT_FGT2) &&
        HDFGRTR2_EL2.nSPMEVTYPErN_EL0 == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            X[t, 64] =
            SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
            (UInt(SPMSELR_EL0.BANK) * 16) + m];
    elseif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
        && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
```

```

when SDD == '1' && MDCR_EL3.EnPM2 == '0' then
    UNDEFINED;
elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_EL0.BANK) * 16) + m];
elseif PSTATE.EL == EL3 then
    X[t, 64] =
SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_EL0.BANK) * 16) + m];

```

**MSR SPMEVFILT2R<m>\_EL0, <Xt> ; Where m = 0-15**

op0	op1	CRn	CRm	op2
0b10	0b011	0b1110	0b011:m[3]	m[2:0]

```

integer m = UInt(CRm<0>:op2<2:0>);

if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1' && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
    && IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
    && IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nSPMEVTYPErN_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_EL0.BANK) * 16) + m] = X[t, 64];
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1' && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elseif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&

```

```

SCR_EL3.FGTEn2 == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elseif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nSPMEVTYPEr_n_EL0 == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
        (UInt(SPMSELR_EL0.BANK) * 16) + m] = X[t, 64];
elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elseif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
            (UInt(SPMSELR_EL0.BANK) * 16) + m] = X[t, 64];
elseif PSTATE.EL == EL3 then
    SPMEVFILT2R_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
    (UInt(SPMSELR_EL0.BANK) * 16) + m] = X[t, 64];

```

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.