 <u>Base</u>	SIMD&FP	<u>SVE</u>	SME	Index by
<u>Instructions</u>	Instructions	<u>Instructions</u>	Instructions	Encoding

TSB CSYNC

Trace Synchronization Barrier. This instruction is a barrier that synchronizes the trace operations of instructions, see *Trace Synchronization Buffer (TSB CSYNC)*.

If *FEAT TRF* is not implemented, this instruction executes as a NOP.

System (FEAT_TRF)

TSB CSYNC

```
if !IsFeatureImplemented(FEAT_TRF) then <a href="mailto:EndOfInstruction">EndOfInstruction</a>();
```

Operation

TraceSynchronizationBarrier();

<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel ; Build timestamp: 2023-09-18T17:56

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.

Sh Pseud

Sh Pseu