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Base Instructions

SIMD&FP **Instructions**

SVE Instructions

Ir

FTSMUL

Floating-point trigonometric starting value

The ftsmul instruction calculates the initial value for the ftmad instruction. The instruction squares each element in the first source vector and then sets the sign bit to a copy of bit 0 of the corresponding element in the second source register, and places the results in the destination vector. This instruction is unpredicated.

To compute sin(x) or cos(x) the instruction is executed with elements of the first source vector set to x, adjusted to be in the range $-\ddot{\mathbb{I}} \in /4 < x \hat{a} \le \ddot{\mathbb{I}} \in /4$.

The elements of the second source vector hold the corresponding value of the quadrant q number as an integer not a floating-point value. The value q satisfies the relationship (2q-1) \tilde{A} — $\tilde{I} \in /4 < x \hat{a} \le (2q+1) \tilde{A}$ — $\tilde{I} \in /4$.

This instruction is illegal when executed in Streaming SVE mode, unless FEAT SME FA64 is implemented and enabled.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
                                      0 0 0 0 1 1
0 1 1 0 0 1 0 1 size 0
                              Zm
```

```
FTSMUL \langle Zd \rangle . \langle T \rangle , \langle Zn \rangle . \langle T \rangle , \langle Zm \rangle . \langle T \rangle
```

```
if !HaveSVE() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);</pre>
integer n = UInt(Zn);
integer m = UInt(Zm);
integer d = UInt(Zd);
```

Assembler Symbols

< 7.d >

Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T>

Is the size specifier, encoded in "size":

size	<t></t>
0.0	RESERVED
01	Н
10	S
11	D

<Zn>

Is the name of the first source scalable vector register, encoded in the "Zn" field.

<7.m>

Is the name of the second source scalable vector register, encoded in the "Zm" field.

Operation

```
CheckNonStreamingSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV esize;
bits(VL) operand1 = Z[n, VL];
bits(VL) operand2 = Z[m, VL];
bits(VL) result;

for e = 0 to elements-1
    bits(esize) element1 = Elem[operand1, e, esize];
    bits(esize) element2 = Elem[operand2, e, esize];
    Elem[result, e, esize] = FPTrigSMul(element1, element2, FPCR[]);

Z[d, VL] = result;
```

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel ; Build timestamp: 2023-09-18T17:56

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