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Base Instructions

SIMD&FP **Instructions** 

**SVE** Instructions

**SME** Instructions

#### **BEXT**

Gather lower bits from positions selected by bitmask

This instruction gathers bits in each element of the first source vector from the bit positions indicated by non-zero bits in the corresponding mask element of the second source vector to the lowest-numbered contiguous bits of the corresponding destination element, preserving their order, and sets the remaining higher-numbered bits to zero. This instruction is unpredicated.

ID AA64ZFR0 EL1.BitPerm indicates whether this instruction is implemented.

This instruction is illegal when executed in Streaming SVE mode, unless FEAT SME FA64 is implemented and enabled.

# SVE<sub>2</sub> (FEAT\_SVE\_BitPerm)

```
31\ 30\ 29\ 28\ 27\ 26\ 25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0
0 1 0 0 0 1 0 1 size 0
                                   Zm
                                             1 0 1 1 0 0
                                                                     Zn
```

```
BEXT \langle Zd \rangle.\langle T \rangle, \langle Zn \rangle.\langle T \rangle, \langle Zm \rangle.\langle T \rangle
if ! <a href="HaveSVE">HaveSVE2BitPerm</a> () then UNDEFINED;
constant integer esize = 8 << UInt(size);</pre>
integer n = UInt(Zn);
integer m = UInt(Zm);
integer d = UInt(Zd);
```

### **Assembler Symbols**

<Zd>

Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T>

Is the size specifier, encoded in "size":

| size | <t></t> |
|------|---------|
| 0.0  | В       |
| 01   | Н       |
| 10   | S       |
| 11   | D       |

<Zn>

Is the name of the first source scalable vector register, encoded in the "Zn" field.

<Zm>

Is the name of the second source scalable vector register, encoded in the "Zm" field.

## **Operation**

### **Operational information**

### If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

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