

TCO, Tag Check Override

The TCO characteristics are:

Purpose

When FEAT_MTE is implemented, this register allows tag checks to be disabled globally.

When FEAT_MTE2 is not implemented, it is constrained unpredictable whether this register is res0 or behaves as if FEAT_MTE2 is implemented.

Configuration

This register is present only when FEAT_MTE is implemented. Otherwise, direct accesses to TCO are undefined.

Attributes

TCO is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	
RES0																																
RES0						TCO	RES0																									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Bits [63:26]

Reserved, res0.

TCO, bit [25]

Allows memory tag checks to be globally disabled.

TCO	Meaning
0b0	Loads and Stores are not affected by this control.
0b1	Loads and Stores are unchecked.

Bits [24:0]

Reserved, res0.

Accessing TCO

For information about the operation of the MSR (immediate) accessor, see MSR (immediate).

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, TCO

op0	op1	CRn	CRm	op2
0b11	0b011	0b0100	0b0010	0b111

```
if PSTATE.EL == EL0 then
    X[t, 64] = Zeros(38):PSTATE.TCO:Zeros(25);
elsif PSTATE.EL == EL1 then
    X[t, 64] = Zeros(38):PSTATE.TCO:Zeros(25);
elsif PSTATE.EL == EL2 then
    X[t, 64] = Zeros(38):PSTATE.TCO:Zeros(25);
elsif PSTATE.EL == EL3 then
    X[t, 64] = Zeros(38):PSTATE.TCO:Zeros(25);
```

MSR TCO, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b011	0b0100	0b0010	0b111

```
if PSTATE.EL == EL0 then
    PSTATE.TCO = X[t, 64]<25>;
elsif PSTATE.EL == EL1 then
    PSTATE.TCO = X[t, 64]<25>;
elsif PSTATE.EL == EL2 then
    PSTATE.TCO = X[t, 64]<25>;
elsif PSTATE.EL == EL3 then
    PSTATE.TCO = X[t, 64]<25>;
```

MSR TCO, #<imm>

op0	op1	CRn	op2
0b00	0b011	0b0100	0b100

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