

**BFVDOT**

Multi-vector BFloat16 floating-point vertical dot-product by indexed element

The instruction computes the sum-of-products of each vertical pair of BFloat16 values in the corresponding elements of the two first source vectors with the pair of BFloat16 values in the indexed 32-bit group of the corresponding 128-bit segment of the second source vector. The single-precision sum-of-products results are destructively added to the corresponding single-precision elements of the two ZA single-vector groups. The BF16 pairs within the second source vector are specified using an immediate index which selects the same BF16 pair position within each 128-bit vector segment. The element index range is from 0 to 3.

The vector numbers forming the single-vector group within each half of the ZA array are selected by the sum of the vector select register and immediate offset, modulo half the number of ZA array vectors.

The vector group symbol VGx2 indicates that the ZA operand consists of two ZA single-vector groups. The vector group symbol is preferred for disassembly, but optional in assembler source code.

This instruction follows SME2 ZA-targeting BFloat16 numerical behaviors. This instruction is unpredicated.

**SME2**  
**(FEAT\_SME2)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	1	0	1	0	1	Zm			0	Rv	0	i2	Zn			0	1	1	off3						

**BFVDOT** ZA.S[<Wv>, <offs>{, VGx2}], { <Zn1>.H-<Zn2>.H }, <Zm>.H[<index>]

```
if !HaveSME2() then UNDEFINED;
integer v = UInt('010':Rv);
integer n = UInt(Zn:'0');
integer m = UInt('0':Zm);
integer offset = UInt(off3);
integer index = UInt(i2);
```

**Assembler Symbols**

- <Wv> Is the 32-bit name of the vector select register W8-W11, encoded in the "Rv" field.
- <offs> Is the vector select offset, in the range 0 to 7, encoded in the "off3" field.
- <Zn1> Is the name of the first scalable vector register of a multi-vector sequence, encoded as "Zn" times 2.

<Zn2>	Is the name of the second scalable vector register of a multi-vector sequence, encoded as "Zn" times 2 plus 1.
<Zm>	Is the name of the second source scalable vector register Z0-Z15, encoded in the "Zm" field.
<index>	Is the immediate index of a group of two 16-bit elements within each 128-bit vector segment, in the range 0 to 3, encoded in the "i2" field.

## Operation

```

CheckStreamingSVEAndZAEEnabled\(\);
constant integer VL = CurrentVL;
constant integer elements = VL DIV 32;
integer vectors = VL DIV 8;
integer vstride = vectors DIV 2;
integer eltspersegment = 128 DIV 32;
bits(32) vbase = X[v, 32];
integer vec = (UInt(vbase) + offset) MOD vstride;
bits(VL) result;

for r = 0 to 1
    bits(VL) operand1a = Z[n, VL];
    bits(VL) operand1b = Z[n+1, VL];
    bits(VL) operand2 = Z[m, VL];
    bits(VL) operand3 = ZAvector[vec, VL];
    for e = 0 to elements-1
        integer segmentbase = e - (e MOD eltspersegment);
        integer s = segmentbase + index;
        bits(16) elt1_a = Elem[operand1a, 2 * e + r, 16];
        bits(16) elt1_b = Elem[operand1b, 2 * e + r, 16];
        bits(16) elt2_a = Elem[operand2, 2 * s + 0, 16];
        bits(16) elt2_b = Elem[operand2, 2 * s + 1, 16];
        bits(32) sum = Elem[operand3, e, 32];
        sum = BFDotAdd(sum, elt1_a, elt1_b, elt2_a, elt2_b, FPCR[]);
        Elem[result, e, 32] = sum;
        ZAvector[vec, VL] = result;
    vec = vec + vstride;

```

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56

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