

STTRB

Store Register Byte (unprivileged) stores a byte from a 32-bit register to memory. The address that is used for the store is calculated from a base register and an immediate offset.

Memory accesses made by the instruction behave as if the instruction was executed at EL0 if the *Effective value* of PSTATE.UAO is 0 and either:

- The instruction is executed at EL1.
- The instruction is executed at EL2 when the *Effective value* of *HCR_EL2*.{E2H, TGE} is {1, 1}.

Otherwise, the memory access operates with the restrictions determined by the Exception level at which the instruction is executed. For information about memory accesses, see *Load/Store addressing modes*.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|----|----|----|----|-----|----|----|----|----|----|------|----|----|----|----|----|----|----|----|----|----|---|----|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | imm9 | | | | | 1 | 0 | Rn | | | | | Rt | | | | | | | | |
| size | | | | | opc | | | | | | | | | | | | | | | | | | | | | | | | | | |

STTRB <Wt>, [<Xn|SP>{, #<sim>}]

```
bits(64) offset = SignExtend(imm9, 64);
```

Assembler Symbols

| | |
|---------|--|
| <Wt> | Is the 32-bit name of the general-purpose register to be transferred, encoded in the "Rt" field. |
| <Xn SP> | Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field. |
| <sim> | Is the optional signed immediate byte offset, in the range -256 to 255, defaulting to 0 and encoded in the "imm9" field. |

Shared Decode

```
integer n = UInt(Rn);
integer t = UInt(Rt);

boolean tagchecked = n != 31;
```

Operation

```
bits(64) address;
bits(8) data;

boolean privileged = AArch64.IsUnprivAccessPriv();
```

```
AccessDescriptor accdesc = CreateAccDescGPR(MemOp\_STORE, FALSE, privile
if n == 31 then
    CheckSPAlignment();
    address = SP[];
else
    address = X[n, 64];

address = address + offset;

data = X[t, 8];
Mem[address, 1, accdesc] = data;
```

Operational information

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

| Base Instructions | SIMD&FP Instructions | SVE Instructions | SME Instructions | Index by Encoding | Sh Pseu |
|--|--|----------------------------------|----------------------------------|-----------------------------------|-------------------------|
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