

GITS_SGIR, ITS SGI Register

The GITS_SGIR characteristics are:

Purpose

Written by software to signal a virtual SGI for translation by the ITS.

Configuration

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GITS_SGIR are res0.

This register is provided only in FEAT_GICv4p1 implementations.

Attributes

GITS_SGIR is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32		
RES0																vPEID																	
RES0																														vINTID			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Bits [63:48]

Reserved, res0.

vPEID, bits [47:32]

ID of target vPEID.

The size of this field is implementation defined, and is specified by the [GICD_TYPER2.VIL](#) and [GICD_TYPER2.VID](#) fields. Unimplemented bits are res0.

Bits [31:4]

Reserved, res0.

vINTID, bits [3:0]

INTID of virtual SGI.

Accessing GITS_SGIR

64-bit access only.

GITS_SGIR can be accessed through the memory-mapped interfaces:

Component	Offset
GIC ITS control	0x20020

Accesses on this interface are **WO**.

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