# GICD_ITARGETSR<n>, Interrupt Processor Targets Registers, n = 0 - 254

The GICD_ITARGETSR<n> characteristics are:

## Purpose

When affinity routing is not enabled, holds the list of target PEs for the interrupt. That is, it holds the list of CPU interfaces to which the Distributor forwards the interrupt if it is asserted and has sufficient priority.

## Configuration

These registers are available in all configurations of the GIC. When GICD_CTLR.DS==0, these registers are Common.

The number of implemented GICD_ITARGETSR<n> registers is 8*(GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

GICD_ITARGETSR0 to GICD_ITARGETSR7 are Banked for each connected PEwith GICR_TYPER.Processor_Number < 8.

Accessing GICD_ITARGETSR0 to GICD_ITARGETSR7 from a PE with GICR_TYPER.Processor_Number > 7 is constrained unpredictable:

- Register is RAZ/WI.
- An unknown banked copy of the register is accessed.

## Attributes

GICD_ITARGETSR<n> is a 32-bit register.

## Field descriptions

| 31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| CPU_targets_offset_3 | CPU_targets_offset_2 | CPU_targets_offset_1 | CPU_targets_offset_0 |

PEs in the system number from 0, and each bit in a PE targets field refers to the corresponding PE. For example, a value of `0x3` means that the Pending interrupt is sent to PEs 0 and 1. For GICD_ITARGETSR0-GICD_ITARGETSR7, a read of any targets field returns the number of the PE performing the read.

**CPU_targets_offset_3B, bits [31:24]**

PE targets for an interrupt, at byte offset 3.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**CPU_targets_offset_2B, bits [23:16]**

PE targets for an interrupt, at byte offset 2.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**CPU_targets_offset_1B, bits [15:8]**

PE targets for an interrupt, at byte offset 1.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**CPU_targets_offset_0B, bits [7:0]**

PE targets for an interrupt, at byte offset 0.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

The bits that are set to 1 in the PE targets field determine which PEs are targeted:

| Value of PE targets field | Interrupt targets |
|---|---|
| `0bxxxxxxx1` | CPU interface 0 |
| `0bxxxxxx1x` | CPU interface 1 |
| `0bxxxxx1xx` | CPU interface 2 |
| `0bxxxx1xxx` | CPU interface 3 |
| `0bxxx1xxxx` | CPU interface 4 |
| `0bxx1xxxxx` | CPU interface 5 |
| `0bx1xxxxxx` | CPU interface 6 |
| `0b1xxxxxxx` | CPU interface 7 |

For interrupt ID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ITARGETSR<n> number, n, is given by n = m DIV 4.
- The offset of the required GICD_ITARGETSR<n> register is (`0x800` + (4*n)).
- The byte offset of the required Priority field in this register is m MOD 4, where:
    - Byte offset 0 refers to register bits [7:0].
    - Byte offset 1 refers to register bits [15:8].
    - Byte offset 2 refers to register bits [23:16].
    - Byte offset 3 refers to register bits [31:24].

Software can write to these registers at any time. Any change to a targets field value:

- Has no effect on any active interrupt. This means that removing a CPU interface from a targets list does not cancel an active state for interrupts on that CPU interface. There is no effect on interrupts that are active and pending until the active status is cleared, at which time it is treated as a pending interrupt.
- Has an effect on any pending interrupts. This means:
    - Enables the CPU interface to be chosen as a target for the pending interrupt using an implementation defined mechanism.
    - Removing a CPU interface from the target list of a pending interrupt removes the pending state of the interrupt on that CPU interface.

## Accessing GICD_ITARGETSR<n>

These registers are used when affinity routing is not enabled. When affinity routing is enabled for the Security state of an interrupt, the target PEs for an interrupt are defined by GICD_IROUTER<n> and the associated byte in GICD_ITARGETSR<n> is res0. An implementation is permitted to make the byte RAZ/WI in this case.

- These registers are byte-accessible.
- A register field corresponding to an unimplemented interrupt is RAZ/WI.
- A field bit corresponding to an unimplemented CPU interface is RAZ/WI.
- GICD_ITARGETSR0-GICD_ITARGETSR7 are read-only. Each field returns a value that corresponds only to the PE reading the register.
- It is implementation defined which, if any, SPIs are statically configured in hardware. The field for such an SPI is read-only, and returns a value that indicates the PE targets for the interrupt.
- If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any bits that correspond to Group 0 or Secure Group 1

interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.

In a single connected PE implementation, all interrupts target one PE, and these registers are RAZ/WI.

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**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

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**GICD_ITARGETSR<n> can be accessed through the memory-mapped interfaces:**

| Component | Frame | Offset | Instance |
|---|---|---|---|
| GIC Distributor | Dist_base | 0x0800 + (4 * n) | GICD_ITARGETSR<n> |

Accesses on this interface are **RW**.

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