BFADD (unpredicated)

BFloat16 floating-point add vectors (unpredicated)

Add all BFloat16 elements of the second source vector to corresponding elements of the first source vector and place the results in the corresponding elements of the destination vector.
This instruction follows SVE2.1 non-widening BFloat16 numerical behaviors.
This instruction is unpredicated.
ID_AA64ZFR0_EL1.B16B16 indicates whether this instruction is implemented.

SVE2
(FEAT_SVE_B16B16)

31 30 29 28 27 26 25 24	23	22	21	20 19 18 17 16	15 14 13	12 11 10	9 8 7 6 5	4 3 2 1 0
0 1 1 0 0 1 0 1	0	0	0	Zm	0 0 0	0 0 0	Zn	Zd
	size<1>	size<0>						

      BFADD \<Zd\>.H, \<Zn\>.H, \<Zm\>.H

```
if (!HaveSVE2() && !HaveSME2()) || !IsFeatureImplemented(FEAT_SVE_B16B1
integer n = UInt(Zn);
integer m = UInt(Zm);
integer d = UInt(Zd);
```

Assembler Symbols

\<Zd\>   Is the name of the destination scalable vector register, encoded in the "Zd" field.

\<Zn\>   Is the name of the first source scalable vector register, encoded in the "Zn" field.

\<Zm\>   Is the name of the second source scalable vector register, encoded in the "Zm" field.

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer elements = VL DIV 16;
bits(VL) operand1 = Z[n, VL];
bits(VL) operand2 = Z[m, VL];
bits(VL) result;

for e = 0 to elements-1
    bits(16) element1 = Elem[operand1, e, 16];
    bits(16) element2 = Elem[operand2, e, 16];
    Elem[result, e, 16] = BFAdd(element1, element2, FPCR[]);
```

```
Z[d, VL] = result;
```

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56