MOV

Move predicate (unpredicated)

Read all elements from the source predicate and place in the destination predicate. This instruction is unpredicated. Does not set the condition flags.

For programmer convenience, an assembler must also accept predicate-as-counter register names for the source and destination predicate registers.

This is an alias of [ORR (predicates)](#). This means:

- The encodings in this description are named to match the encodings of [ORR (predicates)](#).
- The description of [ORR (predicates)](#) gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19 18 17 16	15	14	13 12 11 10	9	8 7 6 5	4	3 2 1 0
0	0	1	0	0	1	0	1	1	0	0	0	Pm	0	1	Pg	0	Pn	0	Pd

S (below bit 22)

    MOV **<Pd>**.B, **<Pn>**.B

is equivalent to

    ORR **<Pd>**.B, **<Pn>**/Z, **<Pn>**.B, **<Pn>**.B

and is the preferred disassembly when
`S == '0' && Pn == Pm && Pm == Pg.`

Assembler Symbols

<Pd>   Is the name of the destination scalable predicate register, encoded in the "Pd" field.

<Pn>   Is the name of the first source scalable predicate register, encoded in the "Pn" field.

Operation

The description of [ORR (predicates)](#) gives the operational pseudocode for this instruction.

Operational information

If FEAT_SVE2 is implemented or FEAT_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.

- The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
    - The values of the data supplied in any of its registers.
    - The values of the NZCV flags.