EDITCTRL, External Debug Integration mode Control register

The EDITCTRL characteristics are:

Purpose

Enables the external debug to switch from its default mode into integration mode, where test software can control directly the inputs and outputs of the PE, for integration testing or topology detection.

Configuration

The power domain of EDITCTRL is implementation defined.

Implementation of this register is optional.

Attributes

EDITCTRL is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																															IME

Bits [31:1]

Reserved, res0.

IME, bit [0]

Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is implementation defined.

IME	Meaning
0b0	Normal operation.
0b1	Integration mode enabled.

The following resets apply:

- Whichever power domain the register is implemented in, this field resets to 0.

Otherwise, the value of this field is unchanged.

Accessing EDITCTRL

EDITCTRL can be accessed through the external debug interface:

Component	Offset	Instance
Debug	0xF00	EDITCTRL

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus(), accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and ! SoftwareLockStatus(), accesses to this register are **RW**.
- Otherwise, accesses to this register are **IMPDEF**.

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