AMPIDR0, Activity Monitors Peripheral Identification Register 0

The AMPIDR0 characteristics are:

Purpose

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

It is implementation defined whether AMPIDR0 is implemented in the Core power domain or in the Debug power domain.

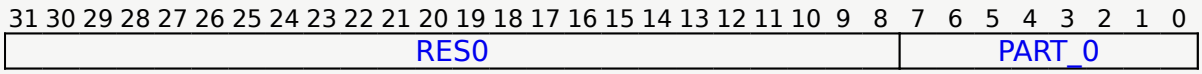
Implementation of this register is optional.

This register is present only when FEAT_AMUv1 is implemented.

Attributes

AMPIDR0 is a 32-bit register.

Field descriptions



Bits [31:8]

Reserved, res0.

PART_0, bits [7:0]

Part number, least significant byte.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing AMPIDR0

AMPIDR0 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
AMU	0xFE0	AMPIDR0

Accesses on this interface are **RO**.

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94