

EDDFR1, External Debug Feature Register 1

The EDDFR1 characteristics are:

Purpose

Provides top level information about the debug system in AArch64.

Configuration

The power domain of EDDFR1 is implementation defined.

Attributes

EDDFR1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ABL_CMPs								RES0				EBEP				ITE				ABLE				PMICNTR				SPMU			
CTX_CMPs								WRPs								BRPs								SYSPMUID							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ABL_CMPs, bits [63:56]

When FEAT_ABLE is implemented:

Number of breakpoints that support address linking, minus 1.

The values 0x40 to 0xFF are reserved.

The value of this field is never greater than either EDDFR1.WRPs or EDDFR1.BRPs.

Otherwise:

Reserved, res0.

Bits [55:52]

Reserved, res0.

EBEP, bits [51:48]

This field either has the same value as [ID_AA64DFR1_EL1.EBEP](#) or reads as zero.

ITE, bits [47:44]

This field either has the same value as [ID_AA64DFR1_EL1.ITE](#) or reads as zero.

ABLE, bits [43:40]

Address Breakpoint Linking Extension. Defined values are:

ABLE	Meaning
0b0000	Address Breakpoint Linking Extension not implemented.
0b0001	Address Breakpoint Linking Extension implemented.

All other values are reserved.

FEAT_ABLE implements the functionality identified by the value 0b0001.

In an implementation that supports AArch64, this field has the same value as [ID_AA64DFR1_EL1.ABLE](#).

PMICNTR, bits [39:36]

This field either has the same value as [ID_AA64DFR1_EL1.PMICNTR](#) or reads as zero.

SPMU, bits [35:32]

This field either has the same value as [ID_AA64DFR1_EL1.SPMU](#) or reads as zero.

CTX_CMPs, bits [31:24]

When FEAT_Debugv8p9 is implemented and EDDFR.CTX_CMPs == 0b1111:

Number of breakpoints that are context-aware, minus 1.

The value 0x00 means 16 breakpoints that are context-aware are implemented. Otherwise, this field is the number of breakpoints that are context-aware, minus 1.

The values 0x01 to 0x0F and 0x40 to 0xFF are reserved.

The value of this field is never greater than EDDFR1.BRPs.

In an implementation that supports AArch64, this field has the same value as [ID_AA64DFR1_EL1.CTX_CMPs](#).

Otherwise:

Reserved, res0.

WRPs, bits [23:16]

When FEAT_Debugv8p9 is implemented and EDDFR.WRPs == 0b1111:

Number of watchpoints, minus 1.

The value 0x00 means 16 watchpoints are implemented. Otherwise, this field is the number of watchpoints, minus 1.

The values 0x01 to 0x0F and 0x40 to 0xFF are reserved.

In an implementation that supports AArch64, this field has the same value as [ID_AA64DFR1_EL1](#).WRPs.

Otherwise:

Reserved, res0.

BRPs, bits [15:8]

When FEAT_Debugv8p9 is implemented and EDDFR.BRPs == 0b1111:

Number of breakpoints, minus 1.

The value 0x00 means 16 breakpoints are implemented. Otherwise, this field is the number of breakpoints, minus 1.

The values 0x01 to 0x0F and 0x40 to 0xFF are reserved.

In an implementation that supports AArch64, this field has the same value as [ID_AA64DFR1_EL1](#).BRPs.

Otherwise:

Reserved, res0.

SYSPMUID, bits [7:0]

This field either has the same value as [ID_AA64DFR1_EL1](#).SYSPMUID or reads as zero.

Accessing EDDFR1

EDDFR1 can be accessed through the external debug interface:

Component	Offset	Instance	Range
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Debug	0xD48	EDDFR1	31:0
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This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **IMPDEF**.

Component	Offset	Instance	Range
Debug	0xD4C	EDDFR1	63:32

This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **IMPDEF**.

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