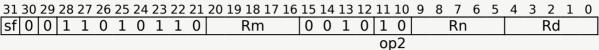
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#### **ASRV**

Arithmetic Shift Right Variable shifts a register value right by a variable number of bits, shifting in copies of its sign bit, and writes the result to the destination register. The remainder obtained by dividing the second source register by the data size defines the number of bits by which the first source register is right-shifted.

This instruction is used by the alias <u>ASR (register)</u>.



32-bit (sf == 0)

```
64-bit (sf == 1)
```

```
ASRV \langle Xd \rangle, \langle Xn \rangle, \langle Xm \rangle
```

ASRV <Wd>, <Wn>, <Wm>

```
integer d = <u>UInt</u>(Rd);
integer n = <u>UInt</u>(Rn);
integer m = <u>UInt</u>(Rm);
constant integer datasize = 32 << <u>UInt</u>(sf);
<u>ShiftType</u> shift_type = <u>DecodeShift</u>(op2);
```

# **Assembler Symbols**

<wd></wd>	Is the 32-bit name of the general-purpose destination
-----------	---

register, encoded in the "Rd" field.

<Wn> Is the 32-bit name of the first general-purpose source

register, encoded in the "Rn" field.

<Wm> Is the 32-bit name of the second general-purpose source

register holding a shift amount from 0 to 31 in its bottom 5

bits, encoded in the "Rm" field.

<Xd> Is the 64-bit name of the general-purpose destination

register, encoded in the "Rd" field.

<Xn> Is the 64-bit name of the first general-purpose source

register, encoded in the "Rn" field.

<Xm> Is the 64-bit name of the second general-purpose source

register holding a shift amount from 0 to 63 in its bottom 6

bits, encoded in the "Rm" field.

### **Operation**

```
bits(datasize) result;
bits(datasize) operand2 = X[m, datasize];

result = ShiftReg(n, shift_type, UInt(operand2) MOD datasize, datasize)
X[d, datasize] = result;
```

## **Operational information**

#### If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel ; Build timestamp: 2023-09-18T17:56

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