PMZR_EL0, Performance Monitors Zero with Mask

The PMZR_EL0 characteristics are:

Purpose

Zero the set of counters specified by the mask written to PMZR_EL0.

Configuration

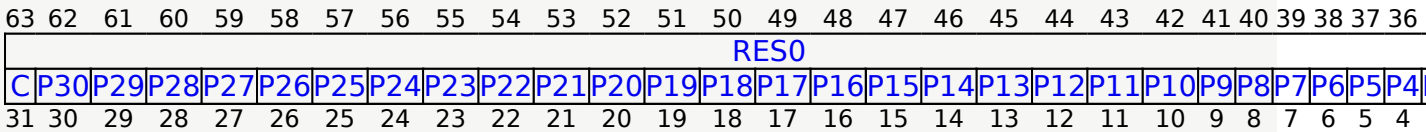
AArch64 System register PMZR_EL0 bits [63:0] are architecturally mapped to External register PMU.PMZR_EL0[63:0] when FEAT_PMUv3_EXT64 is implemented and FEAT_PMUv3p9 is implemented.

This register is present only when FEAT_PMUv3p9 is implemented. Otherwise, direct accesses to PMZR_EL0 are undefined.

Attributes

PMZR_EL0 is a 64-bit register.

Field descriptions



Bits [63:33]

Reserved, res0.

F<m>, bit [m+32], for m = 0
When FEAT_PMUv3_ICNTR is implemented:

Zero fixed-function counter <m>.

F<m>	Meaning
0b0	Write is ignored.
0b1	Set fixed-function counter <m> to zero.

Writing 1 to PMZR_EL0.F0 sets PMICNTR_EL0 to zero.

- This field ignores writes if any of the following are true:
  - All of the following are true:
    - PMUSERENR_EL0.UEN == 0 or PMUACR_EL1.F<m> == 0.
    - Accessed at EL0.
  - All of the following are true:
    - EL3 is implemented.
    - MDCR_EL3.EnPM2 == 0.
    - Accessed at EL2, EL1, or EL0.
  - All of the following are true:
    - FEAT_FGT2 is implemented.
    - EL3 is implemented and SCR_EL3.FGTEn2 == 0, or HDFGWTR2_EL2.nPMICFILTR_EL0 == 0.
    - EL2 is implemented and enabled in the current Security state.
    - Accessed at EL1 or EL0.
    - HCR_EL2.{E2H,TGE} != {1,1}.
  - All of the following are true:
    - Accessed at EL0.
    - PMUSERENR_EL0.IR == 1.
- Otherwise access to this field is WO.

Otherwise:

Reserved, res0.

C, bit [31]

Zero PMCCNTR_EL0.

C	Meaning
0b0	Write is ignored.
0b1	Set PMCCNTR_EL0 to zero.

Accessing this field has the following behavior:

- This field ignores writes if any of the following are true:
  - All of the following are true:
    - Accessed at EL0.
    - PMUSERENR_EL0.UEN == 1.
    - PMUACR_EL1.C == 0.
  - All of the following are true:
    - Accessed at EL0.
    - PMUSERENR_EL0.{UEN,CR} == {1,1}.
- Otherwise access to this field is WO.

P<m>, bit [m], for m = 30 to 0

Zero PMEVCNTR<m>_EL0.

P<m>	Meaning
0b0	Write is ignored.
0b1	Set PMEVCNTR<m>_EL0 to zero.

Accessing this field has the following behavior:

- This field ignores writes if any of the following are true:
  - All of the following are true:
    - Accessed at EL0.
    - PMUSERENR_EL0.UEN == 1.
    - PMUACR_EL1.P<m> == 0.
  - All of the following are true:
    - Accessed at EL0.
    - PMUSERENR_EL0.{UEN,ER} == {1,1}.
  - All of the following are true:
    - EL2 is implemented and enabled in the current Security state.
    - m >= UInt(MDCR_EL2.HPMN).
    - Accessed at EL0 or EL1.
  - m >= UInt(PMCR_EL0.N).
- Otherwise access to this field is W1C.

Accessing PMZR_EL0

Accesses to this register use the following encodings in the System register encoding space:

```
MSR PMZR_EL0, <Xt>
```

op0	op1	CRn	CRm	op2
0b11	0b011	0b1001	0b1101	0b100

```
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
```

```
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nPMZR_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        PMZR_EL0 = X[t, 64];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nPMZR_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        PMZR_EL0 = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        PMZR_EL0 = X[t, 64];
elsif PSTATE.EL == EL3 then
    PMZR_EL0 = X[t, 64];
```