

PMVCIDSR, CONTEXTIDR_EL1 and VMID Sample Register

The PMVCIDSR characteristics are:

Purpose

Contains the sampled CONTEXTIDR_EL1 and VMID values that are captured on reading PMU.PMPCSR.

Configuration

This register is present only when FEAT_PMUv3_EXT64 is implemented and FEAT_PCSRv8p2 is implemented. Otherwise, direct accesses to PMVCIDSR are res0.

If FEAT_PMUv3_EXT32 is implemented, the same content is present in the same location, and can be accessed using PMVIDSR[31:0] and PMCID1SR[31:0].

Note

Before Armv8.2, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of [EDDEVID](#).PCSample.

Attributes

PMVCIDSR is a 64-bit register.

This register is part of the [PMU](#) block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																VMID[15:8]								VMID							
CONTEXTIDR_EL1																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:48]

Reserved, res0.

VMID[15:8], bits [47:40]

When FEAT_VMID16 is implemented:

Extension to VMID[7:0]. For more information, see VMID[7:0].

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

VMID, bits [39:32]

VMID sample. The VMID associated with the most recent PMU.PMPCSR sample. When the most recent PMU.PMPCSR sample was generated:

- This field is set to an unknown value if any of the following apply:
 - EL2 is disabled in the current Security state.
 - The PE is executing at EL2.
 - EL2 is enabled in the current Security state, the PE is executing at EL0, EL2 is using AArch64, HCR_EL2.E2H == 1, and HCR_EL2.TGE == 1.
- Otherwise:
 - If EL2 is using AArch64 and either FEAT_VMID16 is not implemented or [VTCR_EL2.VS](#) is 1, this field is set to [VTTBR_EL2.VMID](#).
 - If EL2 is using AArch64, FEAT_VMID16 is implemented, and [VTCR_EL2.VS](#) is 0, PMVIDSR.VMID[7:0] is set to [VTTBR_EL2.VMID\[7:0\]](#) and PMVIDSR.VMID[15:8] is res0.
 - If EL2 is using AArch32, this field is set to [VTTBR.VMID](#).

Because the value written to PMVIDSR is an indirect read of the VMID value, it is constrained unpredictable whether PMVIDSR is set to the original or new value if PMU.PMPCSR samples:

- An instruction that writes to the VMID value.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CONTEXTIDR_EL1, bits [31:0]

Context ID. The value of CONTEXTIDR that is associated with the most recent PMU.PMPCSR sample. When the most recent PMU.PMPCSR sample is generated:

- If EL1 is using AArch64, then the Context ID is sampled from [CONTEXTIDR_EL1](#).
- If EL1 is using AArch32, then the Context ID is sampled from [CONTEXTIDR](#).
- If EL3 is implemented and is using AArch32, then [CONTEXTIDR](#) is a banked register and this register samples the current banked copy of [CONTEXTIDR](#) for the Security state that is associated with the most recent PMU.PMPCSR sample.

Because the value written to this register is an indirect read of CONTEXTIDR, it is constrained unpredictable whether this register is set to the original or new value if PMU.PMPCSR samples:

- An instruction that writes to CONTEXTIDR.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

Accessing PMVCIDSR

implementation defined extensions to external debug might make the value of this register unknown, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.

Accesses to this register use the following encodings:

Accessible at offset 0x208 from PMU

- When DoubleLockStatus(), or !IsCorePowered() or OSLockStatus(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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