

## LASTB (SIMD&FP scalar)

Extract last element to SIMD&FP scalar register

If there is an active element then extract the last active element from the final source vector register. If there are no active elements, extract the highest-numbered element. Then place the extracted element in the destination SIMD&FP register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	size	1	0	0	0	1	1	1	0	0	Pg	Zn				Vd								
B																															

**LASTB** <V><d>, <Pg>, <Zn>.<T>

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Vd);
boolean isBefore = TRUE;
```

## Assembler Symbols

<V>

Is a width specifier, encoded in "size":

size	<V>
00	B
01	H
10	S
11	D

<d>

Is the number [0-31] of the destination SIMD&FP register, encoded in the "Vd" field.

<Pg>

Is the name of the governing scalable predicate register P0-P7, encoded in the "Pg" field.

<Zn>

Is the name of the source scalable vector register, encoded in the "Zn" field.

<T>

Is the size specifier, encoded in "size":

size	<T>
00	B
01	H
10	S
11	D

## Operation

```
CheckSVEEnabled();  
constant integer VL = CurrentVL;  
constant integer PL = VL DIV 8;  
constant integer elements = VL DIV esize;  
bits(PL) mask = P[g, PL];  
bits(VL) operand = Z[n, VL];  
integer last = LastActiveElement(mask, esize);  
  
if isBefore then  
    if last < 0 then last = elements - 1;  
else  
    last = last + 1;  
    if last >= elements then last = 0;  
V[d, esize] = Elem[operand, last, esize];
```

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