GICR_WAKER, Redistributor Wake Register

The GICR_WAKER characteristics are:

Purpose

Permits software to control the behavior of the WakeRequest power management signal corresponding to the Redistributor. Power management operations follow the rules in 'Power management' in in ARMÂ® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Configuration

A copy of this register is provided for each Redistributor.

Attributes

GICR_WAKER is a 32-bit register.

Field descriptions

31	30:3	2	1
IMPLEMENTATION DEFINED	RES0	ChildrenAsleep	ProcessorSleep

IMPLEMENTATION DEFINED, bit [31]

implementation defined.

Bits [30:3]

Reserved, res0.

ChildrenAsleep, bit [2]

Read-only. Indicates whether the connected PE is quiescent:

ChildrenAsleep	Meaning
0b0	An interface to the connected PE might be active.
0b1	All interfaces to the connected PE are quiescent.

The reset behavior of this field is:

- On a GIC reset, this field resets to `1`.

ProcessorSleep, bit [1]

Indicates whether the Redistributor can assert the **WakeRequest** signal:

ProcessorSleep	Meaning
`0b0`	This PE is not in, and is not entering, a low power state.

0b1	The PE is either in, or is in the process of entering, a low power state. All interrupts that arrive at the Redistributor: • Assert a **WakeRequest** signal. • Are held in the pending state at the Redistributor, and are not communicated to the CPU interface. **Note** When ProcessorSleep == 1, the Redistributor must ensure that any interrupts that are pending on the CPU interface are released. For an implementation that is using the GIC Stream Protocol Interface: • A Quiesce command puts the interface between the Redistributor and the CPU interface in a quiescent state. For more information, see 'Quiesce (IRI)' in ARMÂ® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069). • A Release command releases any interrupts that are pending on the CPU interface. For more information, see 'Release (ICC)' in ARMÂ® Generic Interrupt Controller Architecture Specification, GIC

Note

Before powering down a PE, software must set this bit to 1 and wait until ChildrenAsleep == 1. After powering up a PE, or following a failed powerdown, software must set this bit to 0 and wait until ChildrenAsleep == 0.

Changing ProcessorSleep from 1 to 0 when ChildrenAsleep is not 1 results in unpredictable behavior.

Changing ProcessorSleep from 0 to 1 when the Enable for each interrupt group in the associated CPU interface is not 0 results in unpredictable behavior.

The reset behavior of this field is:

- On a GIC reset, this field resets to `1`.

IMPLEMENTATION DEFINED, bit [0]

implementation defined.

Accessing GICR_WAKER

To ensure a Redistributor is quiescent, software must write to GICR_WAKER with ProcessorSleep == 1, then poll the register until ChildrenAsleep == 1.

Resetting the connected PE when GICR_WAKER.ProcessorSleep==0 or GICR_WAKER.ChildresAsleep==0, can lead to unpredictable behavior in the IRI.

Resetting the IRI when GICR_WAKER.ProcessorSleep==0 or GICR_WAKER.ChildresAsleep==0 can lead to unpredictable behavior in the connected PE.

GICR_WAKER can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Redistributor	RD_base	`0x0014`	GICR_WAKER

This interface is accessible as follows:

- When GICD_CTLR.DS == 1, accesses to this register are **RW**.
- When GICD_CTLR.DS == 0 and an access is Secure, accesses to this register are **RW**.
- When GICD_CTLR.DS == 0 and an access is Non-secure, accesses to this register are **RAZ/WI**.

- When GICD_CTLR.DS == 0, FEAT_RME is implemented and an access is Root, accesses to this register are **RW**.
- When GICD_CTLR.DS == 0, FEAT_RME is implemented and an access is Realm, accesses to this register are **RAZ/WI**.

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