EDHSR, External Debug Halting Syndrome Register

The EDHSR characteristics are:

Purpose

Holds syndrome information for a debug event.

Configuration

EDHSR is in the Core power domain.

This register is present only when FEAT_Debugv8p9 is implemented or (FEAT_Debugv8p2 is implemented and an implementation implements EDHSR). Otherwise, direct accesses to EDHSR are res0.

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Attributes

EDHSR is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																							GCS	RES0							
RES0				WPT				WPTV	WPF	FnP	RES0		VNCR	RES0		FnV	RES0					CM	RES0		WnR	RES0						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:41]

Reserved, res0.

GCS, bit [40]
When FEAT_GCS is implemented and FEAT_Debugv8p9 is implemented:

Guarded control stack data access.

Indicates that the Watchpoint debug event is due to a Guarded control stack data access.

GCS	Meaning
0b0	The Watchpoint debug event is not due to a Guarded control stack data access.

0b1	The Watchpoint debug event is due to a Guarded control stack data access.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [39:24]

Reserved, res0.

WPT, bits [23:18]

Watchpoint number. When EDHSR.WPTV is 1, holds the index of a watchpoint that triggered the Watchpoint debug event.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

WPTV, bit [17]

Watchpoint number valid.

WPTV	Meaning	Applies when
0b0	EDHSR.WPT field is not valid, and holds an unknown value.	When FEAT_Debugv8p9 is not implemented
0b1	EDHSR.WPT field is valid, and holds the number of a watchpoint that triggered the Watchpoint debug event.	

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

WPF, bit [16]

Watchpoint match might be False.

WPF	Meaning	Applies when
0b0	The watchpoint matched the original access or set of contiguous accesses.	
0b1	The watchpoint matched an access or set of contiguous accesses where the lowest accessed address was rounded down to the nearest multiple of 16 bytes and the highest accessed address was rounded up to the nearest multiple of 16 bytes minus 1, but the watchpoint might not have matched the original address of the access or set of contiguous accesses.	When FEAT_SME is implemented or FEAT_SVE is implemented

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

FnP, bit [15]

EDWAR not Precise.

FnP	Meaning	Applies when
0b0	If the EDWAR is valid, it holds the virtual address of an access or sequence of contiguous accesses that triggered the Watchpoint debug event.	
0b1	If the EDWAR is valid, it holds any virtual address within the smallest implemented translation granule that contains the virtual address of an access or set of contiguous accesses that triggered the Watchpoint debug event.	When FEAT_SME is implemented or FEAT_SVE is implemented

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bit [14]

Reserved, res0.

VNCR, bit [13]
When FEAT_Debugv8p9 is implemented:

VNCR_EL2 access. Indicates that the Watchpoint debug event came from use of VNCR_EL2 register by EL1 code.

VNCR	Meaning	Applies when

0b0	The Watchpoint debug event was not generated by the use of VNCR_EL2 by EL1 code.	
0b1	The Watchpoint debug event was generated by the use of VNCR_EL2 by EL1 code.	When FEAT_NV2 is implemented

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [12:11]

Reserved, res0.

FnV, bit [10]

EDWAR not Valid.

FnV	Meaning	Applies when
0b0	EDWAR is valid.	
0b1	EDWAR is not valid, and holds an unknown value.	When FEAT_SME is implemented or FEAT_SVE is implemented

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bit [9]

Reserved, res0.

CM, bit [8]
When FEAT_Debugv8p9 is implemented:

Cache maintenance. Indicates whether the Watchpoint debug event came from a cache maintenance instruction.

CM	Meaning
0b0	The Watchpoint debug event was not generated by the execution of one of the System instructions identified in the description of value 1.
0b1	The Watchpoint debug event was generated by the execution of a cache maintenance instruction. The DC ZVA, DC GVA, and DC GZVA instructions are not cache maintenance instructions, and therefore do not cause this field to be set to 1.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [7]

Reserved, res0.

WnR, bit [6]
When FEAT_Debugv8p9 is implemented:

Write not Read. Indicates whether the Watchpoint debug event was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

WnR	Meaning
0b0	Watchpoint debug event caused by an instruction reading from a memory location.
0b1	Watchpoint debug event caused by an instruction writing to a memory location.

For Watchpoint debug events on cache maintenance instructions, this field is set to 1.

For Watchpoint debug events from an atomic instruction, this field is set to 0 if a read of the location would have generated the Watchpoint debug event, otherwise it is set to 1.

If multiple watchpoints match on the same access, it is unpredictable which watchpoint generates the Watchpoint debug event.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [5:0]

Reserved, res0.

Accessing EDHSR

EDHSR can be accessed through the external debug interface:

Component	Offset	Instance
Debug	0x038	EDHSR

This interface is accessible as follows:

- When DoubleLockStatus(), or !IsCorePowered() or OSLockStatus(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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