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Pseu

ZERO (single-vector)

Zero ZA single-vector groups

The instruction zeroes two or four ZA single-vector groups. The vector numbers forming the single-vector group within each half of or each quarter of the ZA array are selected by the sum of the vector select register and immediate offset, modulo half or quarter the number of ZA array vectors. The vector group symbol, VGx2 or VGx4, indicates that the ZA operand consists of two or four ZA single-vector groups respectively. It has encodings from 2 classes: Two ZA single-vectors and Four ZA single-vectors and Four ZA single-vectors

Two ZA single-vectors (FEAT SME2p1)

```
ZERO ZA.D[<Wv>, <offs>, VGx2]
```

```
if !HaveSME2p1() then UNDEFINED;
integer v = UInt('010':Rv);
integer offset = UInt(off3);
constant integer ngrp = 2;
```

Four ZA single-vectors (FEAT SME2p1)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

1 1 0 0 0 0 0 0 0 0 0 1 1 1 0 0 Rv 0 0 0 0 0 0 0 0 0 0 0 0 6 3

```
ZERO ZA.D[<Wv>, <offs>, VGx4]
```

```
if !HaveSME2p1() then UNDEFINED;
integer v = UInt('010':Rv);
integer offset = UInt(off3);
constant integer ngrp = 4;
```

Assembler Symbols

<Wv> Is the 32-bit name of the vector select register W8-W11,

encoded in the "Rv" field.

<offs> Is the vector select offset, in the range 0 to 7, encoded in

the "off3" field.

Operation

```
CheckStreamingSVEAndZAEnabled();
constant integer VL = CurrentVL;
integer vectors = VL DIV 8;
integer vstride = vectors DIV ngrp;
bits(32) vbase = X[v, 32];
integer vec = (UInt(vbase) + offset) MOD vstride;

for r = 0 to ngrp-1
    ZAvector[vec, VL] = Zeros(VL);
    vec = vec + vstride;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel; Build timestamp: 2023-09-18T17:56

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