PMCGCR0, Counter Group Configuration Register 0

The PMCGCR0 characteristics are:

Purpose

Encodes the number of PMU.PMEVCNTR<n>_EL0 counters implemented.

Configuration

This register is present only when FEAT_PMUv3_ICNTR is implemented. Otherwise, direct accesses to PMCGCR0 are res0.

PMCGCR0 is in the Core power domain.

Attributes

PMCGCR0 is a 32-bit register.

This register is part of the PMU block.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RES0	CG1NC	CG0NC

Bits [31:16]

Reserved, res0.

CG1NC, bits [15:8]

Number of counters in group 1, which comprises the instruction counter PMU.PMICNTR_EL0.

Reads as `0x01`.

Access to this field is **RO**.

CG0NC, bits [7:0]

Number of counters in group 0, which comprises the event counters PMU.PMEVCNTR<n>_EL0 and the cycle counter PMU.PMCCNTR_EL0.

This field reads as PMU.PMCFGR.N.

Accessing PMCGCR0

Accesses to this register use the following encodings:

```
Accessible at offset 0xCE0 from PMU
```

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94