TRCIDR1, ID Register 1

The TRCIDR1 characteristics are:

Purpose

Returns the tracing capabilities of the trace unit.

Configuration

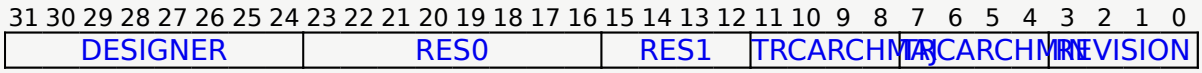
External register TRCIDR1 bits [31:0] are architecturally mapped to AArch64 System register TRCIDR1[31:0].

This register is present only when FEAT_ETE is implemented and FEAT_TRC_EXT is implemented. Otherwise, direct accesses to TRCIDR1 are res0.

Attributes

TRCIDR1 is a 32-bit register.

Field descriptions



DESIGNER, bits [31:24]

Indicates which company designed the trace unit. The permitted values of this field are the same as MIDR_EL1.Implementer.

Bits [23:16]

Reserved, res0.

Bits [15:12]

Reserved, res1.

TRCARCHMAJ, bits [11:8]

Major architecture version.

TRCARCHMAJ	Meaning

0b1111	If both TRCARCHMAJ and TRCARCHMIN == 0xF then refer to TRCDEVARCH.

All other values are reserved.

This field reads as 0b1111.

TRCARCHMIN, bits [7:4]

Minor architecture version.

TRCARCHMIN	Meaning
0b1111	If both TRCARCHMAJ and TRCARCHMIN == 0xF then refer to TRCDEVARCH.

All other values are reserved.

This field reads as 0b1111.

REVISION, bits [3:0]

Implementation revision.

Returns an implementation defined value that identifies the revision of the trace unit.

Arm deprecates any use of this field and recommends that implementations set this field to zero.

Accessing TRCIDR1

TRCIDR1 can be accessed through the external debug interface:

Component	Offset	Instance
ETE	0x1E4	TRCIDR1

This interface is accessible as follows:

- When OSLockStatus() or !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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