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Base Instructions

SIMD&FP **Instructions**

SVE Instructions

SME Instructions

BR

Branch to Register branches unconditionally to an address in a register, with a hint that this is not a subroutine return.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Rn
                                             0
                                               0 0 0 0
                                                Rm
               op
```

```
BR <Xn>
integer n = UInt(Rn);
```

Assembler Symbols

<Xn>

Is the 64-bit name of the general-purpose register holding the address to be branched to, encoded in the "Rn" field.

Operation

```
bits(64) target = X[n, 64];
// Value in BTypeNext will be used to set PSTATE.BTYPE
if InGuardedPage then
    if n == 16 \mid \mid n == 17 then
        BTypeNext = '01';
    else
        BTypeNext = '11';
else
    BTypeNext = '01';
BranchTo(target, BranchType_INDIR, FALSE);
```

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel; Build timestamp: 2023-09-18T17:56

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