

# TRBAUTHSTATUS, Authentication Status Register

The TRBAUTHSTATUS characteristics are:

## Purpose

Provides information about the state of the implementation defined authentication interface for debug.

For additional information, see the CoreSight Architecture Specification.

## Configuration

This register is present only when FEAT\_TRBE\_EXT is implemented. Otherwise, direct accesses to TRBAUTHSTATUS are res0.

TRBAUTHSTATUS is in the Core power domain.

## Attributes

TRBAUTHSTATUS is a 32-bit register.

## Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0				RTNID		RTID		RES0				RLNID		RLID		RES0		SNID		SID		NSNID		NSID							

### Bits [31:28]

Reserved, res0.

### RTNID, bits [27:26]

Root non-invasive debug.

RTNID	Meaning
0b00	Not implemented.

Access to this field is **RO**.

### RTID, bits [25:24]

Root invasive debug.

This field has the same value as [DBGAUTHSTATUS\\_EL1](#).RTID.

#### **Bits [23:16]**

Reserved, res0.

#### **RLNID, bits [15:14]**

Realm non-invasive debug.

<b>RLNID</b>	<b>Meaning</b>
0b00	Not implemented.

Access to this field is **RO**.

#### **RLID, bits [13:12]**

Realm invasive debug.

This field has the same value as [DBGAUTHSTATUS\\_EL1](#).RLID.

#### **Bits [11:8]**

Reserved, res0.

#### **SNID, bits [7:6]**

Secure non-invasive debug.

<b>SNID</b>	<b>Meaning</b>
0b00	Not implemented.

Access to this field is **RO**.

#### **SID, bits [5:4]**

Secure invasive debug.

This field has the same value as [DBGAUTHSTATUS\\_EL1](#).SID.

#### **NSNID, bits [3:2]**

Non-secure non-invasive debug.

<b>NSNID</b>	<b>Meaning</b>
0b00	Not implemented.

Access to this field is **RO**.

**NSID, bits [1:0]**

Non-secure invasive debug.

This field has the same value as [DBGAUTHSTATUS\\_EL1](#).NSID.

**Accessing TRBAUTHSTATUS**

**TRBAUTHSTATUS can be accessed through the external debug interface:**

Component	Offset	Instance
TRBE	0xFB8	TRBAUTHSTATUS

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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