ALLINT, All Interrupt Mask Bit

The ALLINT characteristics are:

Purpose

Allows access to the all interrupt mask bit.

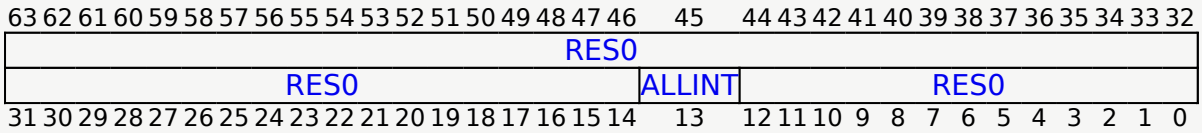
Configuration

This register is present only when FEAT_NMI is implemented. Otherwise, direct accesses to ALLINT are undefined.

Attributes

ALLINT is a 64-bit register.

Field descriptions



Bits [63:14]

Reserved, res0.

ALLINT, bit [13]

All interrupt mask. An interrupt is controlled by PSTATE.ALLINT when all of the following apply:

- SCTLR_ELx.NMI is 1.
- The interrupt is targeted at ELx.
- Execution is at ELx.

ALLINT	Meaning
0b0	This control does not cause any interrupts to be masked.
0b1	If SCTLR_ELx.NMI is 1 and execution is at ELx, an IRQ or FIQ interrupt that is targeted to ELx, with or without Superpriority, is masked.

The value of this bit is set to the inverse value in the SCTLR_ELx.SPINTMASK field on taking an exception to ELx.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [12:0]

Reserved, res0.

Accessing ALLINT

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, ALLINT

op0	op1	CRn	CRm	op2
0b11	0b000	0b0100	0b0011	0b000

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    X[t, 64] = Zeros(50):PSTATE.ALLINT:Zeros(13);
elsif PSTATE.EL == EL2 then
    X[t, 64] = Zeros(50):PSTATE.ALLINT:Zeros(13);
elsif PSTATE.EL == EL3 then
    X[t, 64] = Zeros(50):PSTATE.ALLINT:Zeros(13);
```

MSR ALLINT, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b0100	0b0011	0b000

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && IsHCRXEL2Enabled() &&
HCRX_EL2.TALLINT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        PSTATE.ALLINT = X[t, 64]<13>;
elsif PSTATE.EL == EL2 then
```

```
    PSTATE.ALLINT = X[t, 64]<13>;
elsif PSTATE.EL == EL3 then
    PSTATE.ALLINT = X[t, 64]<13>;
```

MSR ALLINT, #<imm>

op0	op1	CRn	CRm	op2
0b00	0b001	0b0100	0b000x	0b000

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