# EDPRCR, External Debug Power/Reset Control Register

The EDPRCR characteristics are:

## Purpose

Controls the PE functionality related to powerup, reset, and powerdown.

## Configuration

When FEAT_DoPD is implemented, EDPRCR is in the Core power domain. Otherwise, EDPRCR contains fields that are in the Core power domain and fields that are in the Debug power domain.

CORENPDRQ is the only field that is mapped between the EDPRCR and DBGPRCR and DBGPRCR_EL1.

## Attributes

EDPRCR is a 32-bit register.

## Field descriptions

### When FEAT_DoPD is implemented:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | CWRR | CORENPDRQ |

**Bits [31:2]**

Reserved, res0.

**CWRR, bit [1]**
**When FEAT_RME is implemented:**

The PE ignores all writes to this bit.

**Otherwise:**

Warm reset request.

The extent of the reset is implementation defined, but must be one of:

- The request is ignored.
- Only this PE is Warm reset.
- This PE and other components of the system, possibly including other PEs, are Warm reset.

Arm deprecates use of this bit, and recommends that implementations ignore the request.

| CWRR | Meaning |
|---|---|
| 0b0 | No action. |
| 0b1 | Request Warm reset. |

This field is in the Core power domain

The PE ignores writes to this bit if any of the following are true:

- ExternalInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Non-secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE and EL3 is implemented.

In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

- Access is **RAZ/WI** if any of the following are true:
  - OSLockStatus()
  - SoftwareLockStatus()
- Otherwise, access to this field is **WO/RAZ**.

**CORENPDRQ, bit [0]**

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the implementation defined nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

| CORENPDRQ | Meaning |
|---|---|
| 0b0 | If the system responds to a powerdown request, it powers down Core power domain. |
| 0b1 | If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain. |

When this bit reads as unknown, the PE ignores writes to this bit.

This field is in the Core power domain, and permitted accesses to this field map to the DBGPRCR.CORENPDRQ and DBGPRCR_EL1.CORENPDRQ fields.

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is implementation defined whether this bit is reset to the Cold reset value on exit from an implementation defined software-visible retention state. For more information about retention states, see 'Core power domain power states'.

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**Note**

Writes to this bit are not prohibited by the implementation defined authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

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On a Cold reset, if the powerup request is implemented and the powerup request has been asserted, this field is an implementation defined choice of 0 or 1. If the powerup request is not asserted, this field is set to 0.

Accessing this field has the following behavior:

- When OSLockStatus(), access to this field is **UNKNOWN/WI**.
- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **RW**.

## Otherwise:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | COREPURQ | RES0 | | CWRR | CORENPDRQ |

### Bits [31:4]

Reserved, res0.

### COREPURQ, bit [3]

Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain, and that the power controller emulates powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the implementation defined nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

| COREPURQ | Meaning |
|---|---|
| 0b0 | Do not request power up of the Core power domain. |
| 0b1 | Request power up of the Core power domain, and emulation of powerdown. |

In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.

This field is in the Debug power domain and can be read and written when the Core power domain is powered off.

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**Note**

Writes to this bit are not prohibited by the implementation defined authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

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The reset behavior of this field is:

- On an External debug reset, this field resets to 0.

Accessing this field has the following behavior:

- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **RW**.

**Bit [2]**

Reserved, res0.

**CWRR, bit [1]**
**When FEAT_RME is implemented:**

The PE ignores all writes to this bit.

**Otherwise:**

Warm reset request.

The extent of the reset is implementation defined, but must be one of:

- The request is ignored.
- Only this PE is Warm reset.
- This PE and other components of the system, possibly including other PEs, are Warm reset.

Arm deprecates use of this bit, and recommends that implementations ignore the request.

| CWRR | Meaning |
|---|---|
| 0b0 | No action. |
| 0b1 | Request Warm reset. |

This field is in the Core power domain

The PE ignores writes to this bit if any of the following are true:

- ExternalInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Non-secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE and EL3 is implemented.

In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.

The reset behavior of this field is:

- On a Warm reset, this field resets to `0`.

Accessing this field has the following behavior:

- Access is **RAZ/WI** if any of the following are true:
  - !IsCorePowered()
  - DoubleLockStatus()
  - OSLockStatus()
  - SoftwareLockStatus()
- Otherwise, access to this field is **WO/RAZ**.

**CORENPDRQ, bit [0]**

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the implementation defined nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

| CORENPDRQ | Meaning |
|---|---|
| `0b0` | If the system responds to a powerdown request, it powers down Core power domain. |
| `0b1` | If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain. |

When this bit reads as unknown, the PE ignores writes to this bit.

This field is in the Core power domain, and permitted accesses to this field map to the DBGPRCR.CORENPDRQ and DBGPRCR_EL1.CORENPDRQ fields.

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is implementation defined whether this bit is reset to the value of EDPRCR.COREPURQ on exit from an implementation defined software-visible retention state. For more information about retention states, see 'Core power domain power states'.

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**Note**

Writes to this bit are not prohibited by the implementation defined authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

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The reset behavior of this field is:

- On a Cold reset, this field resets to the value in EDPRCR.COREPURQ.

Accessing this field has the following behavior:

- Access is **UNKNOWN/WI** if any of the following are true:
  - !IsCorePowered()
  - DoubleLockStatus()
  - OSLockStatus()
- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **RW**.

## Accessing EDPRCR

On permitted accesses to the register, other access controls affect the behavior of some fields. See the field descriptions for more information.

**EDPRCR can be accessed through the external debug interface:**

| Component | Offset | Instance |
|---|---|---|
| Debug | 0x310 | EDPRCR |

This interface is accessible as follows:

- When (FEAT_DoPD is not implemented or IsCorePowered()) and SoftwareLockStatus(), accesses to this register are **RO**.
- When (FEAT_DoPD is not implemented or IsCorePowered()) and ! SoftwareLockStatus(), accesses to this register are **RW**.
- Otherwise, accesses to this register generate an error response.

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