GCSCR_EL3, Guarded Control Stack Control (EL3)

The GCSCR_EL3 characteristics are:

Purpose

Controls the Guarded control stack at EL3.

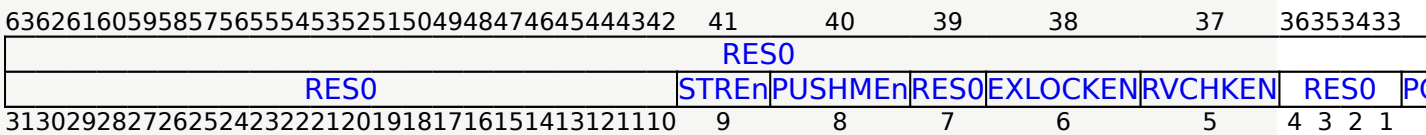
Configuration

This register is present only when FEAT_GCS is implemented. Otherwise, direct accesses to GCSCR_EL3 are undefined.

Attributes

GCSCR_EL3 is a 64-bit register.

Field descriptions



Bits [63:10]

Reserved, res0.

STREn, bit [9]

Execution of the following instructions are trapped:

- GCSSTR.
- GCSSTTR.

STREn	Meaning
0b0	Execution of any of the specified instructions at EL3 cause a GCS exception.
0b1	This control does not cause any instructions to be trapped.

The reset behavior of this field is:

- On a Warm reset, this field resets to `0`.

PUSHMEn, bit [8]

Trap GCSPUSHM instruction.

PUSHMEn	Meaning
`0b0`	Execution of a GCSPUSHM instruction at EL3 causes a Trap exception.
`0b1`	This control does not cause any instructions to be trapped.

The reset behavior of this field is:

- On a Warm reset, this field resets to `0`.

Bit [7]

Reserved, res0.

EXLOCKEN, bit [6]

Exception state lock.

Prevents `MSR` instructions from writing to ELR_EL3 or SPSR_EL3.

EXLOCKEN	Meaning
`0b0`	EL3 exception state locking disabled.
`0b1`	EL3 exception state locking enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to `0`.

RVCHKEN, bit [5]

Return value check enable.

RVCHKEN	Meaning
`0b0`	Return value checking disabled at EL3.
`0b1`	Return value checking enabled at EL3.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [4:1]

Reserved, res0.

PCRSEL, bit [0]

Guarded control stack procedure call return enable selection.

PCRSEL	Meaning
0b0	Guarded control stack at EL3 is not PCR Selected.
0b1	Guarded control stack at EL3 is PCR Selected.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

Accessing GCSCR_EL3

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, GCSCR_EL3

op0	op1	CRn	CRm	op2
0b11	0b110	0b0010	0b0101	0b000

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] = GCSCR_EL3;
```

MSR GCSCR_EL3, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b110	0b0010	0b0101	0b000

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    GCSCR_EL3 = X[t, 64];
```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