<u>Sh</u>
Pseud

Base	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
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MUL

Multiply

:
$$Rd = Rn * Rm$$
.

This is an alias of MADD. This means:

- The encodings in this description are named to match the encodings of MADD.
- The description of MADD gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31 30 29 28 27 26 25 24 23 22 21 2	20 19 18 17 16 15 14 13 12	2111098765	4 3 2 1 0
sf 0 0 1 1 0 1 1 0 0 0	Rm 0 1 1	1 1 Rn	Rd
	o0 Ra	 a	

32-bit (sf == 0)

```
MUL < Wd>, < Wn>, < Wm>
```

is equivalent to

and is always the preferred disassembly.

64-bit (sf == 1)

```
MUL < Xd > , < Xn > , < Xm >
```

is equivalent to

and is always the preferred disassembly.

Assembler Symbols

<wd></wd>	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.

<xd></xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.
<xn></xn>	Is the 64-bit name of the first general-purpose source register holding the multiplicand, encoded in the "Rn" field.
<xm></xm>	Is the 64-bit name of the second general-purpose source register holding the multiplier, encoded in the "Rm" field.

Operation

The description of $\underline{\mathsf{MADD}}$ gives the operational pseudocode for this instruction.

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 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no_diffs_2023_09_RC2,\ sve\ v2023-06_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$

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