

## FMOV (zero, unpredicated)

Move floating-point +0.0 to vector elements (unpredicated)

Unconditionally broadcast the floating-point constant +0.0 into each element of the destination vector. This instruction is unpredicated.

This is a pseudo-instruction of [DUP \(immediate\)](#). This means:

- The encodings in this description are named to match the encodings of [DUP \(immediate\)](#).
- The assembler syntax is used only for assembly, and is not used on disassembly.
- The description of [DUP \(immediate\)](#) gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1	size	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0					Zd
sh																imm8															

**FMOV** <Zd>.<T>, #0.0

is equivalent to

**DUP** <Zd>.<T>, #0

## Assembler Symbols

<Zd> Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T> Is the size specifier, encoded in "size":

size	<T>
00	RESERVED
01	H
10	S
11	D

## Operation

The description of [DUP \(immediate\)](#) gives the operational pseudocode for this instruction.

**Operational information**

If FEAT\_SVE2 is implemented or FEAT\_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
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