x by	Sh
ding	Pseud

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Encoding

STCLRB, STCLRLB

Atomic bit clear on byte in memory, without return, atomically loads an 8-bit byte from memory, performs a bitwise AND with the complement of the value held in a register on it, and stores the result back to memory.

- STCLRB does not have release semantics.
- STCLRLB stores to memory with release semantics, as described in *Load-Acquire*, *Store-Release*.

For information about memory accesses, see *Load/Store addressing modes*.

This is an alias of <u>LDCLRB</u>, <u>LDCLRAB</u>, <u>LDCLRALB</u>, <u>LDCLRLB</u>. This means:

- The encodings in this description are named to match the encodings of LDCLRB, LDCLRAB, LDCLRAB, LDCLRLB.
- The description of <u>LDCLRB</u>, <u>LDCLRAB</u>, <u>LDCLRALB</u>, <u>LDCLRLB</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

Integer (FEAT LSE)

31 30 29	28 27 26 25 24 23 22 2	1 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4 3 2	1 0
0 0 1	1 1 0 0 0 0 R 1	Rs 0 0 0 1 0 0 Rn	1 1 1	1 1
size	Α	орс	Rt	-

No memory ordering (R == 0)

```
STCLRB <Ws>, [<Xn | SP>]
is equivalent to

LDCLRB <Ws>, WZR, [<Xn | SP>]
and is always the preferred disassembly.
```

Release (R == 1)

```
STCLRLB <Ws>, [<Xn|SP>]
is equivalent to

LDCLRLB <Ws>, WZR, [<Xn|SP>]
and is always the preferred disassembly.
```

Assembler Symbols

<Ws> Is the 32-bit name of the general-purpose register holding

the data value to be operated on with the contents of the

memory location, encoded in the "Rs" field.

<Xn|SP> Is the 64-bit name of the general-purpose base register or

stack pointer, encoded in the "Rn" field.

Operation

The description of <u>LDCLRB</u>, <u>LDCLRAB</u>, <u>LDCLRALB</u>, <u>LDCLRLB</u> gives the operational pseudocode for this instruction.

Operational information

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

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