AArch64 Instructions Index by Encoding

External Registers

# AMCIDR1, Activity Monitors Component Identification Register 1

The AMCIDR1 characteristics are:

## **Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Component identification scheme'.

## **Configuration**

It is implementation defined whether AMCIDR1 is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is optional.

This register is present only when FEAT\_AMUv1 is implemented.

## **Attributes**

AMCIDR1 is a 32-bit register.

# Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
RES0	CLASS	PRMBL_1

#### Bits [31:8]

Reserved, res0.

### **CLASS, bits [7:4]**

Component class.

CLASS	Meaning
0b1001	CoreSight component.

Other values are defined by the CoreSight Architecture.

This field reads as  $0 \times 9$ .

## **PRMBL\_1**, bits [3:0]

Preamble.

Reads as 0b0000.

Access to this field is **RO**.

# **Accessing AMCIDR1**

## AMCIDR1 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance	
AMU	0xFF4	AMCIDR1	

Accesses on this interface are **RO**.

AArch32	AArch64	AArch32	AArch64	Index by	<u>External</u>
<u>Registers</u>	<u>Registers</u>	<u>Instructions</u>	<u>Instructions</u>	<b>Encoding</b>	<u>Registers</u>

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