dex by	Sh
coding	Pseu

<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding

LSL (register)

Logical Shift Left (register) shifts a register value left by a variable number of bits, shifting in zeros, and writes the result to the destination register. The remainder obtained by dividing the second source register by the data size defines the number of bits by which the first source register is left-shifted.

This is an alias of LSLV. This means:

- The encodings in this description are named to match the encodings of <u>LSLV</u>.
- The description of <u>LSLV</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9	8 7 6 5	4 3 2 1 0
sf 0 0 1 1 0 1	. 0 1 1 0 Rm	0 0 1 0 0 0	Rn	Rd
	•	on2		

32-bit (sf == 0)

```
LSL <Wd>, <Wn>, <Wm> is equivalent to
```

and is always the preferred disassembly.

64-bit (sf == 1)

```
LSL \langle Xd \rangle, \langle Xn \rangle, \langle Xm \rangle
```

is equivalent to

and is always the preferred disassembly.

Assembler Symbols

<wd></wd>	Is the 32-bit name of the general-purpose destination
	register, encoded in the "Rd" field.

<wm></wm>	Is the 32-bit name of the second general-purpose source register holding a shift amount from 0 to 31 in its bottom 5 bits, encoded in the "Rm" field.
<xd></xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.
<xn></xn>	Is the 64-bit name of the first general-purpose source register, encoded in the "Rn" field.
<xm></xm>	Is the 64-bit name of the second general-purpose source register holding a shift amount from 0 to 63 in its bottom 6 bits, encoded in the "Rm" field.

Operation

The description of <u>LSLV</u> gives the operational pseudocode for this instruction.

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no diffs 2023 09 RC2, sve v2023-06 rel ; Build timestamp: 2023-09-18T17:56

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