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UMMLA (vector)

Unsigned 8-bit integer matrix multiply-accumulate. This instruction multiplies the 2x8 matrix of unsigned 8-bit integer values in the first source vector by the 8x2 matrix of unsigned 8-bit integer values in the second source vector. The resulting 2x2 32-bit integer matrix product is destructively added to the 32-bit integer matrix accumulator in the destination vector. This is equivalent to performing an 8-way dot product per destination element.

From Armv8.2 to Armv8.5, this is an optional instruction. From Armv8.6 it is mandatory for implementations that include Advanced SIMD to support it. *ID AA64ISAR1 EL1*.I8MM indicates whether this instruction is supported.

Vector (FEAT_I8MM)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 1 1 1 0 1 1 0 1 0 0 Rm 1 0 1 0 0 1 Rn Rd B
```

```
UMMLA <Vd>.4S, <Vn>.16B, <Vm>.16B
```

```
if !IsFeatureImplemented(FEAT_I8MM) then UNDEFINED;
integer n = UInt(Rn);
integer m = UInt(Rm);
integer d = UInt(Rd);
```

Assembler Symbols

<Vd> Is the name of the SIMD&FP third source and destination register, encoded in the "Rd" field.

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Is the name of the first SIMD&FP source register, encoded

in the "Rn" field.

<Vm> Is the name of the second SIMD&FP source register,

encoded in the "Rm" field.

Operation

<Vn>

```
CheckFPAdvSIMDEnabled64();

bits(128) operand1 = \underline{V}[n, 128];

bits(128) operand2 = \underline{V}[m, 128];

bits(128) addend = \underline{V}[d, 128];

\underline{V}[d, 128] = \underline{MatMulAdd}(addend, operand1, operand2, TRUE, TRUE);
```

Operational information

Arm expects that the UMMLA (vector) instruction will deliver a peak integer multiply throughput that is at least as high as can be achieved using two UDOT (vector) instructions, with a goal that it should have significantly higher throughput.

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