## SPMEVFILTR<n>\_EL0, System Performance Monitors Event Filter Control Register, n = 0 -63

The SPMEVFILTR<n> EL0 characteristics are:

### **Purpose**

With <u>SPMEVTYPER<n>\_EL0</u> and <u>SPMEVFILT2R<n>\_EL0</u>, configures when event counter <u>SPMEVCNTR<n>\_EL0</u> in System PMU <s> increments.

The contents of this register are implementation defined. For more information, see <u>SPMEVTYPER<n> EL0</u>.

### **Configuration**

This register is present only when FEAT\_SPMU is implemented. Otherwise, direct accesses to SPMEVFILTR<n> EL0 are undefined.

#### **Attributes**

SPMEVFILTR<n>\_EL0 is a 64-bit register.

### Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

IMPLEMENTATION DEFINED

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31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

#### **IMPLEMENTATION DEFINED, bits [63:0]**

implementation defined.

### Accessing SPMEVFILTR<n>\_EL0

To access SPMEVFILTR<n>\_EL0 for System PMU <s>, set <a href="SPMSELR EL0">SPMSELR EL0</a>. SYSPMUSEL to s and <a href="SPMSELR EL0">SPMSELR EL0</a>. BANK to n[5:4].

SPMEVFILTR<n>\_EL0 reads-as-zero and ignores writes if event counter <n> is not implemented by System PMU <s>.

Accesses to this register use the following encodings in the System register encoding space:

## MRS <Xt>, SPMEVFILTR<m>\_EL0 ; Where m = 0-15

op0	op1	CRn	CRm	op2
0b10	0b011	0b1110	0b010:m[3]	m[2:0]

```
integer m = UInt(CRm<0>:op2<2:0>);
if PSTATE.EL == ELO then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<E2H, TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR EL2. <E2H, TGE> != '11'
&& IsFeatureImplemented(FEAT FGT2) &&
HDFGRTR2_EL2.nSPMEVTYPERn_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMEVFILTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR\_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nSPMEVTYPERn_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMEVFILTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
```

# MSR SPMEVFILTR<m>\_EL0, <Xt>; Where m = 0-15

op0	op1	CRn	CRm	op2
0b10	0b011	0b1110	0b010:m[3]	m[2:0]

```
integer m = UInt(CRm<0>:op2<2:0>);
if PSTATE.EL == ELO then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nSPMEVTYPERn_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVFILTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m] = X[t, 64];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
```

```
SCR EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT FGT2) &&
HDFGWTR2 EL2.nSPMEVTYPERn EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVFILTR ELO[UInt(SPMSELR ELO.SYSPMUSEL),
(UInt(SPMSELR ELO.BANK) * 16) + m] = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVFILTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m] = X[t, 64];
elsif PSTATE.EL == EL3 then
    SPMEVFILTR ELO[UInt(SPMSELR ELO.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m] = X[t, 64];
```

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