SPMCFGR_EL1, System Performance Monitors Configuration Register

The SPMCFGR_EL1 characteristics are:

Purpose

Describes the capabilities of System PMU <s>.

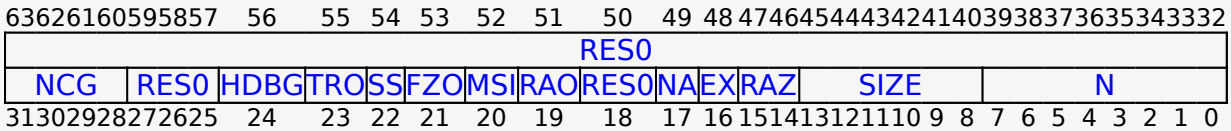
Configuration

This register is present only when FEAT_SPMU is implemented. Otherwise, direct accesses to SPMCFGR_EL1 are undefined.

Attributes

SPMCFGR_EL1 is a 64-bit register.

Field descriptions



Bits [63:32]

Reserved, res0.

NCG, bits [31:28]

Counter Groups.

Defines the number of counter groups implemented by System PMU <s>, minus one.

If this field is zero, then one counter group is implemented and SPMCGCR<n>_EL1 read-as-zero.

Otherwise, for each counter group <m>, SPMCGCR<m DIV 8>_EL1.N<m MOD 8> defines the number of counters in the group.

Locating the first counter in each group depends on the number of implemented groups. Each counter group starts with counter:

- SPMEVTYPER<mÃ—32>_EL0, meaning there are at most 32 counters per group, if there are 2 counter groups.
- SPMEVTYPER<mÃ—16>_EL0, meaning there are at most 16 counters per group, if there are 3 or 4 counter groups.
- SPMEVTYPER<mÃ—8>_EL0, meaning there are at most 8 counters per group, if there are between 5 and 8 counter groups.
- SPMEVTYPER<mÃ—4>_EL0, meaning there are at most 4 counters per group, if there are more than 8 counter groups.

This field has an implementation defined value.

Access to this field is **RO**.

Bits [27:25]

Reserved, res0.

HDBG, bit [24]

Halt-on-debug supported. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

TRO, bit [23]

Trace output supported. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

SS, bit [22]

Snapshot supported. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

FZO, bit [21]

Freeze-on-overflow supported. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

MSI, bit [20]

Message-signaled interrupts supported. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

Bit [19]

Reserved, RAO.

Bit [18]

Reserved, res0.

NA, bit [17]

No write access when running. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

EX, bit [16]

Export supported. For more information on this field, see 'CoreSight PMU Architecture'.

This field has an implementation defined value.

Access to this field is **RO**.

Bits [15:14]

Reserved, RAZ.

SIZE, bits [13:8]

Counter size. The size of the largest counter implemented by System PMU <s>. Defined values are:

SIZE	Meaning
0b000111	8-bit counters.
0b001001	10-bit counters.
0b001011	12-bit counters.
0b001111	16-bit counters.

0b010011	20-bit counters.
0b010111	24-bit counters.
0b011111	32-bit counters.
0b100011	36-bit counters.
0b100111	40-bit counters.
0b101011	44-bit counters.
0b101111	48-bit counters.
0b110011	52-bit counters.
0b110111	56-bit counters.
0b111111	64-bit counters.

All other values are reserved.

Not all counters must be this size. For example, a System PMU might include a mix of 32-bit and 64-bit counters.

N, bits [7:0]

Number of event counters implemented by System PMU <s>, minus 1. Defined values are:

N	Meaning
0x00..0x3F	Number of event counters implemented by System PMU <s>, minus 1.

All other values are reserved.

Accessing SPMCFGR_EL1

To access SPMCFGR_EL1 for System PMU <s>, set SPMSELR_EL0.SYSPMUSEL to s.

SPMCFGR_EL1 reads-as-zero if the System PMU selected by SPMSELR_EL0.SYSPMUSEL is not implemented.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, SPMCFGR_EL1

op0	op1	CRn	CRm	op2
0b10	0b000	0b1001	0b1101	0b111

```
if PSTATE.EL == EL0 then
```

```
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nSPMID == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMCFGR_EL1[UInt(SPMSELR_EL0.SYSPMUSEL)];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMCFGR_EL1[UInt(SPMSELR_EL0.SYSPMUSEL)];
elsif PSTATE.EL == EL3 then
    X[t, 64] =
SPMCFGR_EL1[UInt(SPMSELR_EL0.SYSPMUSEL)];
```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