AArch64
Instructions

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GICR_INVALLR, Redistributor Invalidate All Register

The GICR INVALLR characteristics are:

Purpose

Invalidates any cached configuration data of all LPIs, causing the GIC to reload the interrupt configuration from the appropriate LPI Configuration table.

Configuration

A copy of this register is provided for each Redistributor.

Attributes

GICR INVALLR is a 64-bit register.

Field descriptions

63	63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32							
V	RESO VPEID							
RES0								
31	30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	5 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						

V, bit [63]

When FEAT GICv4p1 is implemented:

Indicates whether the INTID is virtual or physical.

V	Meaning
0b0	Invalidate is for a physical INTID.
0b1	Invalidate is for a virtual INTID.

Otherwise:

Reserved, res0.

Bits [62:48]

Reserved, res0.

vPEID, bits [47:32] When FEAT GICv4p1 is implemented:

When GICR INVLPIR.V == 0, this field is res0

When GICR_INVLPIR.V == 1, this field is the target vPEID of the invalidate.

Note

The size of this field is implementation defined, and is specified by the <u>GICD_TYPER2</u>.VIL and <u>GICD_TYPER2</u>.VID fields. Unimplemented bits are res0.

Otherwise:

Reserved, res0.

Bits [31:0]

Reserved, res0.

Note

If any LPI has been forwarded to the PE and a valid write to GICR_INVALLR is received, the Redistributor must ensure it reloads its properties from memory. This has no effect on the forwarded LPI if it has already been activated.

Accessing GICR_INVALLR

This register is mandatory when any of the following are true:

- GICR TYPER.Direct is 1.
- GICR CTLR.IR is 1.
- GICv4.1 is implemented.

Otherwise, the functionality is implementation defined.

Writes to this register have no effect if no physical LPIs are currently stored in the local Redistributor cache.

GICR INVALLR can be accessed through the memory-mapped interfaces:

Component Frame	Offset	Instance
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GIC	RD_base	0x00B0	GICR_INVALLR
Redistributor			

Accesses on this interface are WO.

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