GICR_IPRIORITYR<n>, Interrupt Priority Registers, n = 0 - 7

The GICR_IPRIORITYR<n> characteristics are:

Purpose

Holds the priority of the corresponding interrupt for each SGI and PPI supported by the GIC.

Configuration

A copy of these registers is provided for each Redistributor.

These registers are configured as follows:

- GICR_IPRIORITYR0-GICR_IPRIORITYR3 store the priority of SGIs.
- GICR_IPRIORITYR4-GICR_IPRIORITYR7 store the priority of PPIs.

Attributes

GICR_IPRIORITYR<n> is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Priority_offset_3B	Priority_offset_2B	Priority_offset_1B	Priority_offset_0B

Priority_offset_3B, bits [31:24]

Interrupt priority value from an implementation defined range, at byte offset 3. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

Priority_offset_2B, bits [23:16]

Interrupt priority value from an implementation defined range, at byte offset 2. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

Priority_offset_1B, bits [15:8]

Interrupt priority value from an implementation defined range, at byte offset 1. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

Priority_offset_0B, bits [7:0]

Interrupt priority value from an implementation defined range, at byte offset 0. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

Accessing GICR_IPRIORITYR<n>

These registers are used when affinity routing is enabled for the Security state of the interrupt. When affinity routing is not enabled the bits corresponding to the interrupt are RAZ/WI and GICD_IPRIORITYR<n> provides equivalent functionality.

These registers are used for SGIs and PPIs only. Equivalent functionality for SPIs is provided by GICD_IPRIORITYR<n>.

These registers are byte-accessible.

When GICD_CTLR.DS == 0:

- A field that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.
- A Non-secure access to a field that corresponds to a Non-secure Group 1 interrupt behaves as described in 'Software accesses of interrupt priority' in ARMÂ® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Note

Implementations must ensure that an interrupt that is pending at the time of the

write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

GICR_IPRIORITYR<n> can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Redistributor	SGI_base	0x0400 + (4 * n)	GICR_IPRIORITYR<n>

Accesses on this interface are **RW**.

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