

TRCDEVAFF, Device Affinity Register

The TRCDEVAFF characteristics are:

Purpose

For additional information, see the CoreSight Architecture Specification.

Reads the same value as the [MPIDR_EL1](#) register for the PE that this trace unit has affinity with.

Configuration

This register is present only when FEAT_ETE is implemented and FEAT_TRC_EXT is implemented. Otherwise, direct accesses to TRCDEVAFF are res0.

Attributes

TRCDEVAFF is a 64-bit register.

Field descriptions

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| MPIDR_EL1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| MPIDR_EL1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

MPIDR_EL1, bits [63:0]

Read-only copy of [MPIDR_EL1](#), as seen from the highest implemented Exception level.

Accessing TRCDEVAFF

External debugger accesses to this register are unaffected by the OS Lock.

TRCDEVAFF can be accessed through the external debug interface:

| Component | Offset | Instance |
|-----------|--------|-----------|
| ETE | 0xFA8 | TRCDEVAFF |

This interface is accessible as follows:

- When !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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