AArch32 Instructions AArch64
Instructions

Index by Encoding

External Registers

# MPAMCFG\_MBW\_MIN, MPAM Memory Bandwidth Minimum Partition Configuration Register

The MPAMCFG MBW MIN characteristics are:

### **Purpose**

MPAMCFG\_MBW\_MIN is a 32-bit read/write register that controls the minimum fraction of memory bandwidth that the PARTID selected by MPAMCFG\_PART\_SEL is permitted to use.

MPAMCFG\_MBW\_MIN\_s controls the minimum bandwidth for the Secure PARTID selected by the Secure instance of MPAMCFG\_PART\_SEL. MPAMCFG\_MBW\_MIN\_ns controls the minimum bandwidth for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG\_PART\_SEL. MPAMCFG\_MBW\_MIN\_rt controls the minimum bandwidth for the Root PARTID selected by the Root instance of MPAMCFG\_PART\_SEL. MPAMCFG\_MBW\_MIN\_rl controls the minimum bandwidth for the Realm PARTID selected by the Realm instance of MPAMCFG\_PART\_SEL.

A PARTID that has used less than MIN is given preferential access to bandwidth.

If <u>MPAMF\_IDR</u>.HAS\_RIS is 1, the control settings accessed are those of the resource instance currently selected by <u>MPAMCFG\_PART\_SEL</u>.RIS and the PARTID selected by <u>MPAMCFG\_PART\_SEL</u>.PARTID\_SEL.

### **Configuration**

This register is present only when FEAT\_MPAM is implemented, MPAMF\_IDR.HAS\_MBW\_PART == 1 and MPAMF\_MBW\_IDR.HAS\_MIN == 1. Otherwise, direct accesses to MPAMCFG MBW MIN are res0.

The power and reset domain of each MSC component is specific to that component.

### **Attributes**

MPAMCFG\_MBW\_MIN is a 32-bit register.

#### Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

RESO

MIN

#### Bits [31:16]

Reserved, res0.

#### MIN, bits [15:0]

Memory minimum bandwidth allocated to the partition selected by <u>MPAMCFG\_PART\_SEL</u>. MIN is in fixed-point fraction format. The fraction represents the portion of the total memory bandwidth capacity through the controlled component that the PARTID is permitted to allocate.

The implemented width of the fixed-point fraction is given in <a href="MPAMF\_MBW\_IDR">MPAMF\_MBW\_IDR</a>. BWA\_WD. Unimplemented bits are RAZ/WI. The implemented bits of the MIN field are always to the left of the field. For example, if BWA\_WD = 4, the implemented bits are MPAMCFG\_MBW\_MIN[15:12] and MPAMCFG\_MBW\_MIN[11:0] are unimplemented.

The fixed-point fraction MIN is less than 1. The implied binary point is between bits 15 and 16. This representation has as the largest fraction of the bandwidth that can be represented in an implementation with w implemented bits is 1.0 minus one half to the power w.

## Accessing MPAMCFG\_MBW\_MIN

This register is within the MPAM feature page memory frames.

In a system that supports Secure, Non-secure, Root, and Realm memory maps, there must be MPAM feature pages in all four address maps:

- MPAMCFG\_MBW\_MIN\_s must only be accessible from the Secure MPAM feature page.
- MPAMCFG\_MBW\_MIN\_ns must only be accessible from the Nonsecure MPAM feature page.
- MPAMCFG\_MBW\_MIN\_rt must only be accessible from the Root MPAM feature page.
- MPAMCFG\_MBW\_MIN\_rl must only be accessible from the Realm MPAM feature page.

MPAMCFG\_MBW\_MIN\_s, MPAMCFG\_MBW\_MIN\_ns, MPAMCFG\_MBW\_MIN\_rt, and MPAMCFG\_MBW\_MIN\_rl must be separate registers:

• The Secure instance (MPAMCFG\_MBW\_MIN\_s) accesses the memory minimum bandwidth partitioning used for Secure PARTIDs.

- The Non-secure instance (MPAMCFG\_MBW\_MIN\_ns) accesses the memory minimum bandwidth partitioning used for Non-secure PARTIDs.
- The Root instance (MPAMCFG\_MBW\_MIN\_rt) accesses the memory minimum bandwidth partitioning used for Root PARTIDs.
- The Realm instance (MPAMCFG\_MBW\_MIN\_rl) accesses the memory minimum bandwidth partitioning used for Realm PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG\_MBW\_MIN access the memory minimum bandwidth partitioning configuration settings for the bandwidth resource instance selected by <a href="MPAMCFG\_PART\_SEL">MPAMCFG\_PART\_SEL</a>.RIS and the PARTID selected by <a href="MPAMCFG\_PART\_SEL">MPAMCFG\_PART\_SEL</a>.PARTID SEL.

When RIS is not implemented, loads and stores to MPAMCFG\_MBW\_MIN access the memory minimum bandwidth partitioning configuration settings for the PARTID selected by MPAMCFG\_PART\_SEL.PARTID\_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG\_MBW\_MIN access the memory minimum bandwidth partitioning configuration settings for the internal PARTID selected by MPAMCFG\_PART\_SEL.PARTID\_SEL, and MPAMCFG\_PART\_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG\_MBW\_MIN access the memory minimum bandwidth partitioning configuration settings for the request PARTID selected by MPAMCFG\_PART\_SEL.PARTID\_SEL, and MPAMCFG\_PART\_SEL.INTERNAL must be 0.

# MPAMCFG\_MBW\_MIN can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
MPAM	MPAMF_BASE_s	0x0200	MPAMCFG_MBW_MIN_s

Accesses on this interface are RW.

Component	Frame	Offset	Instance
MPAM	MPAMF_BASE_ns	0x0200	MPAMCFG_MBW_MIN_ns

Accesses on this interface are **RW**.

Component	Frame	Offset	Instance
MPAM	MPAMF_BASE_rt	0x0200	MPAMCFG_MBW_MIN_rt

When FEAT\_RME is implemented, accesses on this interface are **RW**.

Component	Frame	Offset	Instance

MPAM	MPAMF_BASE_rl	0x0200	MPAMCFG_MBW_MIN_rl

When FEAT RME is implemented, accesses on this interface are RW.

AArch32 Registers AArch64 Registers

AArch32 Instructions AArch64
Instructions

Index by Encoding

External Registers

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.