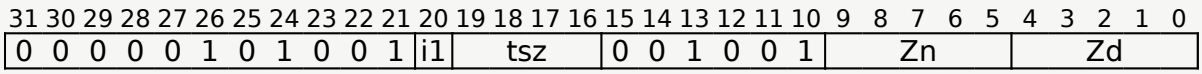
DUPQ

Broadcast indexed element within each quadword vector segment (unpredicated)

Unconditionally broadcast the indexed element within each 128-bit source vector segment to all elements of the corresponding destination vector segment. This instruction is unpredicated.
The immediate element index is in the range of 0 to 15 (bytes), 7 (halfwords), 3 (words) or 1 (doublewords).

SVE2
(FEAT_SVE2p1)




```
DUPQ <Zd>.<T>, <Zn>.<T>[<imm>]
```

```
if !HaveSVE2p1() && !HaveSME2p1() then UNDEFINED;
if tsz == '0000' then UNDEFINED;
constant integer lsb = LowestSetBit(tsz);
constant integer esize = 8 << lsb;
constant bits(5) imm = i1:tsz;
constant integer index = UInt(imm<4:(lsb+1)>);
integer n = UInt(Zn);
integer d = UInt(Zd);
```

Assembler Symbols

<Zd> Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T> Is the size specifier, encoded in “tsz”:

tsz	<T>
0000	RESERVED
xxx1	B
xx10	H
x100	S
1000	D

<Zn> Is the name of the source scalable vector register, encoded in the "Zn" field.

<imm> Is the immediate index, in the range 0 to one less than the number of elements in 128 bits, encoded in "i1:tsz".

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer segments = VL DIV 128;
constant integer elements = 128 DIV esize;
bits(VL) operand = Z[n, VL];
bits(VL) result;
bits(esize) element;

for s = 0 to segments-1
    element = Elem[operand, s * elements + index, esize];
    Elem[result, s, 128] = Replicate(element, 128 DIV esize);

Z[d, VL] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
    - The values of the data supplied in any of its registers.
    - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
    - The values of the data supplied in any of its registers.
    - The values of the NZCV flags.

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56