AMCR, Activity Monitors Control Register

The AMCR characteristics are:

Purpose

Global control register for the activity monitors implementation. AMCR is applicable to both the architected and the auxiliary counter groups.

Configuration

External register AMCR bits [31:0] are architecturally mapped to AArch64 System register AMCR_EL0[31:0].

External register AMCR bits [31:0] are architecturally mapped to AArch32 System register AMCR[31:0].

It is implementation defined whether AMCR is implemented in the Core power domain or in the Debug power domain.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCR are res0.

Attributes

AMCR is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																					HDBG	RES0									

Bits [31:11]

Reserved, res0.

HDBG, bit [10]

This bit controls whether activity monitor counting is halted when the PE is halted in Debug state.

HDBG	Meaning
0b0	Activity monitors do not halt counting when the PE is halted in Debug state.

0b1	Activity monitors halt counting when the PE is halted in Debug state.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [9:0]

Reserved, res0.

Accessing AMCR

AMCR can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
AMU	0xE04	AMCR

Accesses on this interface are **RO**.

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