AArch64 Instructions

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External Registers

PMICNTR ELO, Performance Monitors Instruction Counter Register

The PMICNTR EL0 characteristics are:

Purpose

If event counting is not prohibited and the instruction counter is enabled, the counter increments for each architecturally-executed instruction, according to the configuration specified by PMU.PMICFILTR ELO.

Configuration

External register PMICNTR EL0 bits [63:0] are architecturally mapped to AArch64 System register PMICNTR EL0[63:0].

This register is present only when FEAT PMUv3 ICNTR is implemented. Otherwise, direct accesses to PMICNTR EL0 are res0.

PMICNTR EL0 is in the Core power domain.

Attributes

PMICNTR EL0 is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

03 02 01 00 33 30 37 30 33 31 33 32 31 30 13 10 17 10 13 11 13 12 11 10 33 30 37 30 33 31 33 32						
ICNT						
ICNI						
ICN I						
TOTAL						
21 20 20 20 27 26 25 24 22 22 21 20 10 10 10 17 16 15 14 12 12 11 10 0 0 7 6 5 4 2 2 1 0						

ICNT, bits [63:0]

Instruction Counter.

The reset behavior of this field is:

• On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMICNTR_EL0

Accesses to this register use the following encodings:

Accessible at offset 0x100 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

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