

GCSPR_EL2, Guarded Control Stack Pointer (EL2)

The GCSPR_EL2 characteristics are:

Purpose

Contains the Guarded control stack pointer at EL2.

Configuration

This register is present only when FEAT_GCS is implemented. Otherwise, direct accesses to GCSPR_EL2 are undefined.

Attributes

GCSPR_EL2 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
PTR[63:3]																															
PTR[63:3]																															RES0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

PTR[63:3], bits [63:3]

EL2 Guarded control stack pointer bits [63:3].

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [2:0]

Reserved, res0.

Accessing GCSPR_EL2

When FEAT_VHE is implemented, and [HCR_EL2.E2H](#) is 1, without explicit synchronization, accesses from EL2 using the register name GCSPR_EL2 or GCSPR_EL1 are not guaranteed to be ordered with respect to accesses using the other register name.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, GCSPR_EL2

op0	op1	CRn	CRm	op2
0b11	0b100	0b0010	0b0101	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = GCSPR_EL2;
elsif PSTATE.EL == EL3 then
    X[t, 64] = GCSPR_EL2;
```

MSR GCSPR_EL2, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b100	0b0010	0b0101	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
```

```

        elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            else
                GCSPR_EL2 = X[t, 64];
        elsif PSTATE.EL == EL3 then
            GCSPR_EL2 = X[t, 64];

```

MRS <Xt>, GCSPR_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0010	0b0101	0b001

```

if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elseif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGTR_EL2.nGCS_EL1 == '0'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        X[t, 64] = NVMem[0x8C0];
    else
        X[t, 64] = GCSPR_EL1;
elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elseif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elseif HCR_EL2.E2H == '1' then
        X[t, 64] = GCSPR_EL2;
    else
        X[t, 64] = GCSPR_EL1;
elseif PSTATE.EL == EL3 then
    X[t, 64] = GCSPR_EL1;

```

MSR GCSPR_EL1, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b0010	0b0101	0b001

```

if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elseif EL2Enabled() &&

```

```

IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGWTR_EL2.nGCS_EL1 == '0'
then
    AArch64.SystemAccessTrap(EL2, 0x18);
elseif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        NVMem[0x8C0] = X[t, 64];
    else
        GCSPR_EL1 = X[t, 64];
elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elseif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elseif HCR_EL2.E2H == '1' then
        GCSPR_EL2 = X[t, 64];
    else
        GCSPR_EL1 = X[t, 64];
elseif PSTATE.EL == EL3 then
    GCSPR_EL1 = X[t, 64];

```

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

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