AArch64
Instructions

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External Registers

GMID_EL1, Multiple tag transfer ID Register

The GMID EL1 characteristics are:

Purpose

Indicates the block size that is accessed by the LDGM and STGM System instructions.

Configuration

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to GMID EL1 are undefined.

Attributes

GMID EL1 is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

RES0	
RES0	BS
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0

Bits [63:4]

Reserved, res0.

BS, bits [3:0]

 Log_2 of the block size in words. The minimum supported size is 16B (value == 2) and the maximum is 256B (value == 6).

Accessing GMID_EL1

Accesses to this register use the following encodings in the System register encoding space:

op0 op1 CRn CRm op2	2
---------------------	---

0b11 | 0b001 | 0b0000 | 0b0000 | 0b100

```
if PSTATE.EL == ELO then
    if IsFeatureImplemented(FEAT IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR EL2.TID5 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = GMID\_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = GMID\_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = GMID\_EL1;
```

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