

## AMEVCNTR1<n>, Activity Monitors Event Counter Registers 1, n = 0 - 15

The AMEVCNTR1<n> characteristics are:

### Purpose

Provides access to the auxiliary activity monitor event counters.

### Configuration

External register AMEVCNTR1<n> bits [63:0] are architecturally mapped to AArch64 System register [AMEVCNTR1<n>\\_EL0\[63:0\]](#).

External register AMEVCNTR1<n> bits [63:0] are architecturally mapped to AArch32 System register [AMEVCNTR1<n>\[63:0\]](#).

It is implementation defined whether AMEVCNTR1<n> is implemented in the Core power domain or in the Debug power domain.

This register is present only when FEAT\_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR1<n> are res0.

### Attributes

AMEVCNTR1<n> is a 64-bit register.

### Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ACNT																															
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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

#### ACNT, bits [63:0]

Auxiliary activity monitor event counter n.

Value of auxiliary activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

The reset behavior of this field is:

- On an AMU reset, this field resets to 0.

## Accessing AMEVCNTR1<n>

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads of AMEVCNTR1<n> are RAZ. Software must treat reserved accesses as res0. See 'Access requirements for reserved and unallocated registers'.

**Note**

[AMCGCR](#).CG1NC identifies the number of auxiliary activity monitor event counters.

**AMEVCNTR1<n> can be accessed through the memory-mapped interfaces:**

Component	Offset	Instance	Range
AMU	0x100 + (8 * n)	AMEVCNTR1<n>	31:0

Accesses on this interface are **RO**.

Component	Offset	Instance	Range
AMU	0x104 + (8 * n)	AMEVCNTR1<n>	63:32

Accesses on this interface are **RO**.

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