ERRCRICR2, Critical Error Interrupt Configuration Register 2

The ERRCRICR2 characteristics are:

Purpose

Critical Error Interrupt control and configuration register.

Configuration

This register is present only when (the Critical Error Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRCRICR2 are res0.

ERRCRICR2 is implemented only as part of a memory-mapped group of error records.

Attributes

ERRCRICR2 is a:

- 64-bit register when the Critical Error Interrupt is implemented, the implementation uses the recommended layout for the ERRIRQCR registers and the implementation uses simple interrupts
- 32-bit register when the implementation uses message-signaled interrupts, the Critical Error Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR registers
- 32-bit register when the implementation does not use the recommended layout for the ERRIRQCR registers

Field descriptions

When the Critical Error Interrupt is implemented, the implementation uses the recommended layout for the ERRIRQCR registers and the implementation uses simple interrupts:

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
RES0																								IRQEN	RES0						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:8]

Reserved, res0.

IRQEN, bit [7]

Interrupts enable. Enables generation of interrupts.

IRQEN	Meaning
0b0	Disabled.
0b1	Enabled.

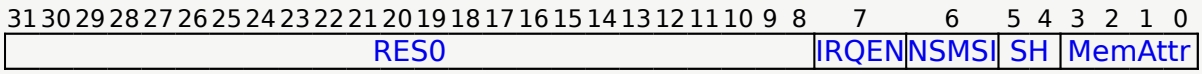
The reset behavior of this field is:

- On an Error recovery reset, this field resets to 0.

Bits [6:0]

Reserved, res0.

When the implementation uses message-signaled interrupts, the Critical Error Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR registers:



Bits [31:8]

Reserved, res0.

IRQEN, bit [7]
When the component supports disabling message signaled interrupts:

Message signaled interrupt enable. Enables generation of message signaled interrupts.

IRQEN	Meaning
0b0	Disabled.
0b1	Enabled.

The reset behavior of this field is:

- On an Error recovery reset, this field resets to 0.

Otherwise:

Reserved, res0.

Message signaled interrupt enable.

Message signaled interrupts are always enabled.

NSMSI, bit [6]
When the component supports configuring the physical address space for message signaled interrupts:

Non-secure message signaled interrupt. Defines the physical address space for message signaled interrupts.

NSMSI	Meaning
0b0	Secure physical address space.
0b1	Non-secure physical address space.

The reset behavior of this field is:

- On a Error recovery reset, this field resets to an implementation defined value.

Accessing this field has the following behavior:

- Access is **RO** if any of the following are true:
  - an access is Non-secure
  - an access is Realm
- Otherwise, access to this field is **RW**.

Otherwise:

Reserved, res0.

Non-secure message signaled interrupt.

The physical address space for message signaled interrupts is implementation defined.

SH, bits [5:4]
When the component supports configuring the Shareability domain for message signaled interrupts:

Shareability. Defines the Shareability domain for message signaled interrupts.

SH	Meaning
0b00	Not shared.
0b10	Outer Shareable.
0b11	Inner Shareable.

All other values are reserved.

This field is ignored when ERRCRICR2.MemAttr specifies any of the following memory types:

- Any Device memory type.
- Normal memory, Inner Non-cacheable, Outer Non-cacheable.

All Device and Normal Inner Non-cacheable Outer Non-cacheable memory regions are always treated as Outer Shareable.

The reset behavior of this field is:

- On an Error recovery reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Shareability.

The Shareability domain for message signaled interrupts is implementation defined.

MemAttr, bits [3:0]
When the component supports configuring the memory type for message signaled interrupts:

Memory type. Defines the memory type and attributes for message signaled interrupts.

MemAttr	Meaning
0b0000	Device-nGnRnE memory.
0b0001	Device-nGnRE memory.
0b0010	Device-nGRE memory.
0b0011	Device-GRE memory.
0b0101	Normal memory, Inner Non-cacheable, Outer Non-cacheable.
0b0110	Normal memory, Inner Write-Through, Outer Non-cacheable.
0b0111	Normal memory, Inner Write-Back, Outer Non-cacheable.
0b1001	Normal memory, Inner Non-cacheable, Outer Write-Through.
0b1010	Normal memory, Inner Write-Through, Outer Write-Through.

0b1011	Normal memory, Inner Write-Back, Outer Write-Through.
0b1101	Normal memory, Inner Non-cacheable, Outer Write-Back.
0b1110	Normal memory, Inner Write-Through, Outer Write-Back.
0b1111	Normal memory, Inner Write-Back, Outer Write-Back.

All other values are reserved.

Note

This is the same format as the VMSAv8-64 stage 2 memory region attributes.

The reset behavior of this field is:

- On an Error recovery reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Memory type.

The memory type used for message signaled interrupts is implementation defined.

When the implementation does not use the recommended layout for the ERRIRQCR registers:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMPLEMENTATION DEFINED																															

IMPLEMENTATION DEFINED, bits [31:0]

implementation defined.

Accessing ERRCRICR2

If the implementation does not use the recommended layout for the ERRIRQCR registers then accesses to ERRCRICR2 are implementation defined.

ERRCRICR2 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance

RAS	0xEAC	ERRCRICR2

This interface is accessible as follows:

- When the implementation uses message-signaled interrupts, (an access is Non-secure or an access is Realm), the implementation uses the recommended layout for the ERRIRQCR registers and ERRCRICR2.NSMSI configures the physical address space for message-signaled interrupts as Secure, accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

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