

## CNTP\_TVAL, Counter-timer Physical Timer TimerValue

The CNTP\_TVAL characteristics are:

### Purpose

Holds the timer value for the EL1 physical timer.

### Configuration

It is implementation defined whether CNTP\_TVAL is implemented in the Core power domain or in the Debug power domain.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

### Attributes

CNTP\_TVAL is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TimerValue																															

### TimerValue, bits [31:0]

The TimerValue view of the EL1 physical timer.

On a read of this register:

- If [CNTP\\_CTL.ENABLE](#) is 0, the value returned is unknown.
- If [CNTP\\_CTL.ENABLE](#) is 1, the value returned is (CompareValue - [CNTPCT](#)).

On a write of this register, CompareValue is set to ([CNTPCT](#) + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When [CNTP\\_CTL.ENABLE](#) is 1, the timer condition is met when ([CNTPCT](#) - CompareValue) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- [CNTP\\_CTL.ISTATUS](#) is set to 1.
- If [CNTP\\_CTL.IMASK](#) is 0, an interrupt is generated.

When [CNTP\\_CTL](#).ENABLE is 0, the timer condition is not met, but [CNTPCT](#) continues to count, so the TimerValue view appears to continue to count down.

The reset behavior of this field is:

- On a Timer reset, this field resets to an architecturally unknown value.

## Accessing CNTP\_TVAL

CNTP\_TVAL can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- CNTP\_TVAL is accessible in that frame if the value of [CNTACR<n>](#).RWPT is 1.
- Otherwise, the CNTP\_TVAL address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTP\_TVAL is accessible in that frame if both:
  - CNTP\_TVAL is accessible in the corresponding CNTBaseN frame:
  - The value of [CNTEL0ACR](#).ELOPTEN is 1.
- Otherwise, the CNTP\_TVAL address in that frame is RAZ/WI.

**CNTP\_TVAL can be accessed through the memory-mapped interfaces:**

Component	Frame	Offset	Instance
Timer	CNTBaseN	0x028	CNTP_TVAL

Accesses on this interface are **RW**.

Component	Frame	Offset	Instance
Timer	CNTEL0BaseN	0x028	CNTP_TVAL

Accesses on this interface are **RW**.

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