# ID\_AFR0\_EL1, AArch32 Auxiliary Feature Register 0

The ID AFR0 EL1 characteristics are:

## **Purpose**

Provides information about the implementation defined features of the PE in AArch32 state.

Must be interpreted with the Main ID Register, MIDR\_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

## **Configuration**

AArch64 System register ID\_AFR0\_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID\_AFR0[31:0].

#### **Attributes**

ID\_AFR0\_EL1 is a 64-bit register.

## Field descriptions

## When AArch32 is supported:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

RESO

RESO

IMPLEMEN IMPLEMEN IMPLEMEN IMPLEMEN IMPLEMEN IMPLEMENTATION
DEFINED DEFINED DEFINED DEFINED

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

#### Bits [63:16]

Reserved, res0.

#### **IMPLEMENTATION DEFINED, bits [15:12]**

implementation defined.

#### **IMPLEMENTATION DEFINED, bits [11:8]**

implementation defined.

#### **IMPLEMENTATION DEFINED, bits [7:4]**

implementation defined.

#### **IMPLEMENTATION DEFINED, bits [3:0]**

implementation defined.

#### Otherwise:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

05 02 01 00 55 50 57 50 55 54 55 52 51 50 45 40 47 40 45 44 45 42 41 40 55 50 57 50 55 54 55 52					
LINIZNIONANI					
UNKNOWN					
LINICHOLINI					
UNKNOWN					

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

#### Bits [63:0]

Reserved, unknown.

## **Accessing ID AFR0 EL1**

Accesses to this register use the following encodings in the System register encoding space:

## MRS <Xt>, ID AFR0 EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0001	0b011

```
if PSTATE.EL == ELO then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID\_AFR0\_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = ID\_AFR0\_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ID\_AFR0\_EL1;
```

AArch32AArch64AArch32AArch64Index byExternalRegistersRegistersInstructionsInstructionsEncodingRegisters

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright  $\hat{A}$  © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.