# PMCID2SR, CONTEXTIDR_EL2 Sample Register

The PMCID2SR characteristics are:

## Purpose

Contains the sampled value of CONTEXTIDR_EL2, captured on reading PMU.PMPCSR[31:0].

## Configuration

This register is present only when FEAT_PMUv3_EXT32 is implemented. Otherwise, direct accesses to PMCID2SR are res0.

If FEAT_PMUv3_EXT64 is implemented, the same content is present in the same location, and can be accessed using PMCCIDSR[63:32].

PMCIDR2SR is in the Core power domain.

**Note**

If FEAT_PCSRv8p2 is not implemented, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

## Attributes

PMCID2SR is a 32-bit register.

This register is part of the PMU block.

## Field descriptions

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CONTEXTIDR_EL2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**CONTEXTIDR_EL2, bits [31:0]**

Context ID. The value of CONTEXTIDR_EL2 that is associated with the most recent PMU.PMPCSR sample. When the most recent PMU.PMPCSR sample is generated:

- If the PE is not executing at EL3, EL2 is using AArch64, and EL2 is enabled in the current Security state, then this field is set to the Context ID sampled from CONTEXTIDR_EL2.
- Otherwise, this field is set to an unknown value.

Because the value written to this field is an indirect read of CONTEXTIDR_EL2, it is constrained unpredictable whether this field is set to the original or new value if PMU.PMPCSR samples:

- An instruction that writes to CONTEXTIDR_EL2.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

## Accessing PMCID2SR

implementation defined extensions to external debug might make the value of this register unknown, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.

Accesses to this register use the following encodings:

```
Accessible at offset 0x22C from PMU
```

- When DoubleLockStatus(), or !IsCorePowered() or OSLockStatus(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.



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