

AMEVTYPER1<n>, Activity Monitors Event Type Registers 1, n = 0 - 15

The AMEVTYPER1<n> characteristics are:

Purpose

Provides information on the events that an auxiliary activity monitor event counter [AMEVCNTR1<n>](#) counts.

Configuration

External register AMEVTYPER1<n> bits [31:0] are architecturally mapped to AArch64 System register [AMEVTYPER1<n>_EL0\[31:0\]](#).

External register AMEVTYPER1<n> bits [31:0] are architecturally mapped to AArch32 System register [AMEVTYPER1<n>\[31:0\]](#).

It is implementation defined whether AMEVTYPER1<n> is implemented in the Core power domain or in the Debug power domain.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPER1<n> are res0.

Attributes

AMEVTYPER1<n> is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																evtCount															

Bits [31:16]

Reserved, res0.

evtCount, bits [15:0]

Event to count. The event number of the event that is counted by the auxiliary activity monitor event counter [AMEVCNTR1<n>](#).

It is implementation defined what values are supported by each counter.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing AMEVTYPER1<n>

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads of AMEVTYPER1<n> are RAZ. Software must treat reserved accesses as res0. See 'Access requirements for reserved and unallocated registers'.

Note

[AMCGCR](#).CG1NC identifies the number of auxiliary activity monitor event counters.

AMEVTYPER1<n> can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
AMU	0x480 + (4 * n)	AMEVTYPER1<n>

Accesses on this interface are **RO**.

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