# GICD_TYPER2, Interrupt Controller Type Register 2

The GICD_TYPER2 characteristics are:

## Purpose

Provides information about which features the GIC implementation supports.

## Configuration

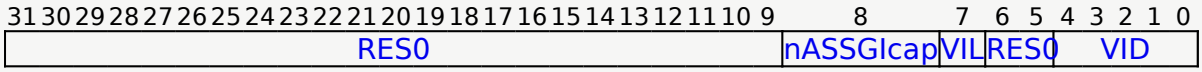
This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICD_TYPER2 are res0.

When GICD_CTLR.DS == 0, this register is Common.

## Attributes

GICD_TYPER2 is a 32-bit register.

## Field descriptions




### Bits [31:9]

Reserved, res0.

### nASSGIcap, bit [8]

Indicates whether SGIs can be configured to not have an active state.

| nASSGIcap | Meaning |
|---|---|
| 0b0 | SGIs have an active state. |
| 0b1 | SGIs can be globally configured not to have an active state. |

This bit is res0 on implementations that support two Security states.

**VIL, bit [7]**

Indicates whether 16 bits of vPEID are implemented.

| VIL | Meaning |
|---|---|
| 0b0 | GIC supports 16-bit vPEID. |
| 0b1 | GIC supports GICD_TYPER2.VID + 1 bits of vPEID. |

**Bits [6:5]**

Reserved, res0.

**VID, bits [4:0]**

When GICD_TYPER2.VIL == 1, the number of bits is equal to the bits of vPEID minus one.

When GICD_TYPER2.VIL == 0, this field is res0.

## Accessing GICD_TYPER2

**GICD_TYPER2 can be accessed through the memory-mapped interfaces:**

| Component | Frame | Offset | Instance |
|---|---|---|---|
| GIC Distributor | Dist_base | 0x000C | GICD_TYPER2 |

Accesses on this interface are **RO**.



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