PMCCIDSR, CONTEXTIDR_ELx Sample Register

The PMCCIDSR characteristics are:

Purpose

Contains the sampled value of CONTEXTIDR_EL1 and CONTEXTIDR_EL2, captured on reading PMU.PMPCSR.

Configuration

This register is present only when FEAT_PMUv3_EXT is implemented. Otherwise, direct accesses to PMCCIDSR are res0.

If FEAT_PMUv3_EXT32 is implemented, the same content is present in the same location, and can be accessed using PMCID2SR[31:0] and PMCID1SR[31:0].

Note

If FEAT_PCSRv8p2 is not implemented, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

Attributes

PMCCIDSR is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
CONTEXTIDR_EL2
CONTEXTIDR_EL1
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

CONTEXTIDR_EL2, bits [63:32]

Context ID. The value of CONTEXTIDR_EL2 that is associated with the most recent PMU.PMPCSR sample. When the most recent PMU.PMPCSR sample is generated:

- If the PE is not executing at EL3, EL2 is using AArch64, and EL2 is enabled in the current Security state, then this field is set to the Context ID sampled from CONTEXTIDR_EL2.
- Otherwise, this field is set to an unknown value.

Because the value written to this field is an indirect read of CONTEXTIDR_EL2, it is constrained unpredictable whether this field is set to the original or new value if PMU.PMPCSR samples:

- An instruction that writes to CONTEXTIDR_EL2.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CONTEXTIDR_EL1, bits [31:0]

Context ID. The value of CONTEXTIDR that is associated with the most recent PMU.PMPCSR sample. When the most recent PMU.PMPCSR sample is generated:

- If EL1 is using AArch64, then the Context ID is sampled from CONTEXTIDR_EL1.
- If EL1 is using AArch32, then the Context ID is sampled from CONTEXTIDR.
- If EL3 is implemented and is using AArch32, then CONTEXTIDR is a banked register and this register samples the current banked copy of CONTEXTIDR for the Security state that is associated with the most recent PMU.PMPCSR sample.

Because the value written to this registser is an indirect read of CONTEXTIDR, it is constrained unpredictable whether this register is set to the original or new value if PMU.PMPCSR samples:

- An instruction that writes to CONTEXTIDR.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

Accessing PMCCIDSR

implementation defined extensions to external debug might make the value of this register unknown, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT64 is implemented

Accessible at offset 0x228 from PMU

- When DoubleLockStatus(), or !IsCorePowered() or OSLockStatus(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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