PMINTEN, Performance Monitors Interrupt Enable register

The PMINTEN characteristics are:

Purpose

Enables the generation of interrupt requests on overflows from the Cycle Count Register, PMU.PMCCNTR_EL0, and the event counters PMU.PMEVCNTR<n>_EL0.

Configuration

External register PMINTEN bits [63:0] are architecturally mapped to AArch64 System register PMINTENSET_EL1[63:0] when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMINTEN bits [63:0] are architecturally mapped to AArch64 System register PMINTENCLR_EL1[63:0] when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMINTEN bits [31:0] are architecturally mapped to AArch32 System register PMINTENCLR[31:0].

External register PMINTEN bits [31:0] are architecturally mapped to AArch32 System register PMINTENSET[31:0].

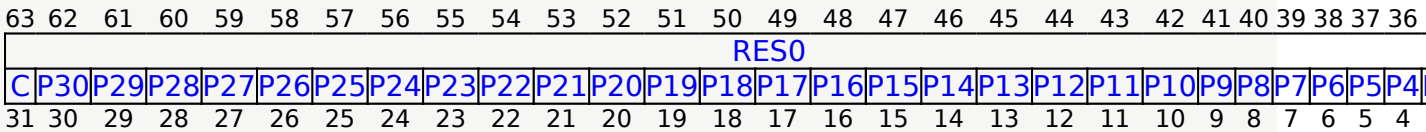
This register is present only when FEAT_PMUv3_EXT64 is implemented. Otherwise, direct accesses to PMINTEN are res0.

Attributes

PMINTEN is a 64-bit register.

This register is part of the PMU block.

Field descriptions



Bits [63:33]

Reserved, res0.

F0, bit [32]
When FEAT_PMUv3_ICNTR is implemented:

Interrupt request on unsigned overflow of PMU.PMICNTR_EL0 enable.

F0	Meaning
0b0	Interrupt request on unsigned overflow of PMU.PMICNTR_EL0 disabled.
0b1	Interrupt request on unsigned overflow of PMU.PMICNTR_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

C, bit [31]

PMU.PMCCNTR_EL0 unsigned overflow interrupt request enable bit. Possible values are:

C	Meaning
0b0	The cycle counter overflow interrupt request is disabled.
0b1	The cycle counter overflow interrupt request is enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

P<n>, bit [n], for n = 30 to 0

Event counter unsigned overflow interrupt request enable bit for PMU.PMEVCNTR<n>_EL0.

If PMU.PMCFGR.N is less than 31, bits [30:PMU.PMCFGR.N] are RAZ/WI.

P<n>	Meaning
0b0	The PMU.PMEVCNTR<n>_EL0 event counter interrupt request is disabled.
0b1	The PMU.PMEVCNTR<n>_EL0 event counter interrupt request is enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMINTEN

Accesses to this register use the following encodings:

Accessible at offset 0xC50 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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