# PMSSCR\_EL1, Performance Monitors Snapshot Status and Capture Register

The PMSSCR EL1 characteristics are:

## **Purpose**

Holds status information about the captured counters and provides a mechanism for software to initiate a sample.

## **Configuration**

AArch64 System register PMSSCR\_EL1 bits [63:0] are architecturally mapped to External register PMU.PMSSCR\_EL1[63:0].

This register is present only when FEAT\_PMUv3\_SS is implemented. Otherwise, direct accesses to PMSSCR EL1 are undefined.

#### **Attributes**

PMSSCR EL1 is a 64-bit register.

## Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

RES0		NC
RES0		SS
 21 20 20 20 27 26 25 24 22 22 21 20 10 10 17 16 15 14 12 12 11 10 0 0 7 6 5 4 2	 1	$\overline{}$

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

#### Bits [63:33]

Reserved, res0.

#### NC, bit [32]

No Capture. Indicates whether the PMU counters have been captured.

NC	Meaning	
0b0	PMU counters captured.	
0b1	PMU counters not captured.	

The reset behavior of this field is:

On a Warm reset, this field resets to 1.

#### Bits [31:1]

Reserved, res0.

#### SS, bit [0]

Snapshot Capture and Status.

SS	Meaning
0b0	On a read, the Capture event has
	completed.
0b1	On a read, the Capture event has
	not completed.
	On a write, request a Capture
	event.

A write of 0 to this field is ignored.

It is constrained unpredictable whether a Capture event has completed if this field is modified when the Capture event is ongoing.

The reset behavior of this field is:

• On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

- When Capture events are disabled, access to this field is **RO**.
- Otherwise, access to this field is **RW**.

## Accessing PMSSCR\_EL1

Accesses to this register use the following encodings in the System register encoding space:

# MRS <Xt>, PMSSCR EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b1001	0b1101	0b011

```
IsFeatureImplemented(FEAT FGT2) && HaveEL(EL3) &&
SCR EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2 EL2.nPMSSCR EL1 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPMSS == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = PMSSCR EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPMSS == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR EL3.EnPMSS == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = PMSSCR\_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = PMSSCR EL1;
```

# MSR PMSSCR\_EL1, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b1001	0b1101	0b011

```
if PSTATE.EL == ELO then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPMSS == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR\_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2 EL2.nPMSSCR EL1 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPMSS == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
```

```
AArch64.SystemAccessTrap(EL3, 0x18);
    else
        PMSSCR\_EL1 = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPMSS == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.EnPMSS == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        PMSSCR_EL1 = X[t, 64];
elsif PSTATE.EL == EL3 then
    PMSSCR_EL1 = X[t, 64];
```

AArch32 Registers AArch64 Registers AArch32 Instructions AArch64 Instructions Index by Encoding External Registers

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