AArch64
Instructions

Index by Encoding

External Registers

EDPIDRO, External Debug Peripheral Identification Register 0

The EDPIDRO characteristics are:

Purpose

Provides information to identify an external debug component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

When FEAT_DoPD is implemented, EDPIDR0 is in the Core power domain. Otherwise, EDPIDR0 is in the Debug power domain.

Implementation of this register is optional.

This register is required for CoreSight compliance.

Attributes

EDPIDR0 is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6 5	4	3	2	1	0
RES0			PART 0				

Bits [31:8]

Reserved, res0.

PART_0, bits [7:0]

Part number, least significant byte.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing EDPIDR0

EDPIDRO can be accessed through the external debug interface:

Component	Offset	Instance		
Debug	0xFE0	EDPIDR0		

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered(), accesses to this register are **RO**.
- Otherwise, accesses to this register generate an error response.

AArch32	AArch64	AArch32	AArch64	Index by	<u>External</u>
<u>Registers</u>	<u>Registers</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding	<u>Registers</u>

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright © 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.