HDFGWTR2_EL2, Hypervisor Debug Fine-Grained Write Trap Register 2

The HDFGWTR2_EL2 characteristics are:

Purpose

Provides controls for traps of MSR and MCR writes of debug, trace, PMU, and Statistical Profiling System registers.

Configuration

This register is present only when FEAT_FGT2 is implemented. Otherwise, direct accesses to HDFGWTR2_EL2 are undefined.

Attributes

HDFGWTR2_EL2 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RES0									nTRBMPAM_EL1	nPMZR_EL0	nTRCITECR_EL1	nPMSDSFR_EL1	RES0		nSPMSCR_EL1	nS
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Bits [63:23]

Reserved, res0.

nTRBMPAM_EL1, bit [22]
When FEAT_TRBE_MPAM is implemented:

Trap MSR writes of TRBMPAM_EL1 at EL1 and EL0 using AArch64 to EL2.

nTRBMPAM_EL1	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2. {E2H, TGE} != {1, 1}, then MSR writes of TRBMPAM_EL1 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of TRBMPAM_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMZR_EL0, bit [21]
When FEAT_PMUv3p9 is implemented:

Trap MSR writes of PMZR_EL0 at EL1 and EL0 using AArch64 to EL2.

nPMZR_EL0	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2.{E2H, TGE} != {1, 1}, then MSR writes of PMZR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of PMZR_EL0 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nTRCITECR_EL1, bit [20]
When FEAT_ITE is implemented:

Trap MSR writes of TRCITECR_EL1 at EL1 using AArch64 to EL2.

nTRCITECR_EL1	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of TRCITECR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of TRCITECR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMSDSFR_EL1, bit [19]
When FEAT_SPE_FDS is implemented:

Trap MSR writes of PMSDSFR_EL1 at EL1 using AArch64 to EL2.

nPMSDSFR_EL1	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of PMSDSFR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of PMSDSFR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [18:17]

Reserved, res0.

nSPMSCR_EL1, bit [16]
When FEAT_SPMU is implemented:

Trap MSR writes of SPMSCR_EL1 at EL1 using AArch64 to EL2.

nSPMSCR_EL1	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of SPMSCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of SPMSCR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMACCESSR_EL1, bit [15]
When FEAT_SPMU is implemented:

Trap MSR writes of SPMACCESSR_EL1 at EL1 using AArch64 to EL2.

nSPMACCESSR_EL1	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of SPMACCESSR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of SPMACCESSR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMCR_EL0, bit [14]
When FEAT_SPMU is implemented:

Trap MSR writes of SPMCR_EL0 at EL1 and EL0 using AArch64 to EL2.

nSPMCR_EL0	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2.{E2H, TGE} != {1, 1}, then MSR writes of SPMCR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of SPMCR_EL0 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMOVS, bit [13]
When FEAT_SPMU is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 and EL0 using AArch64 of any of the following AArch64 System registers to EL2:

- SPMOVSCLR_EL0.
- SPMOVSSET_EL0.

nSPMOVS	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2.{E2H, TGE} != {1, 1}, then MSR writes at EL1 and EL0 using AArch64 of any of the specified System registers are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of the specified System registers are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMINTEN, bit [12]
When FEAT_SPMU is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- SPMINTENCLR_EL1.
- SPMINTENSET_EL1.

nSPMINTEN	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes at EL1 using AArch64 of any of the specified System registers are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of the specified System registers are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMCNTEN, bit [11]
When FEAT_SPMU is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 and EL0 using AArch64 of any of the following AArch64 System registers to EL2:

- SPMCNTENCLR_EL0.
- SPMCNTENSET_EL0.

nSPMCNTEN	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2.{E2H, TGE} != {1, 1}, then MSR writes at EL1 and EL0 using AArch64 of any of the specified System registers are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of the specified System registers are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMSELR_EL0, bit [10]
When FEAT_SPMU is implemented:

Trap MSR writes of SPMSELR_EL0 at EL1 and EL0 using AArch64 to EL2.

nSPMSELR_EL0	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2. {E2H, TGE} != {1, 1}, then MSR writes of SPMSELR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of SPMSELR_EL0 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMEVTYPERn_EL0, bit [9]
When FEAT_SPMU is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 and EL0 using AArch64 of any of the following AArch64 System registers to EL2:

- SPMEVTYPER<n>_EL0.
- SPMEVFILTR<n>_EL0.
- SPMEVFILT2R<n>_EL0.

nSPMEVTYPERn_EL0	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2. {E2H, TGE} != {1, 1}, then MSR writes at EL1 and EL0 using AArch64 of any of the specified System registers are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of the specified System registers are not trapped by this mechanism.

Regardless of the value of this field, if event counter n is not implemented, a write of SPMEVTYPER<n>_EL0, SPMEVFILTR<n>_EL0, or SPMEVFILT2R<n>_EL0 is undefined.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nSPMEVCNTRn_EL0, bit [8]
When FEAT_SPMU is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 and EL0 using AArch64 of any of the following AArch64 System registers to EL2: SPMEVCNTR<n>_EL0.

nSPMEVCNTRn_EL0	Meaning
0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2. {E2H, TGE} != {1, 1}, then MSR writes at EL1 and EL0 using AArch64 of any of the specified System registers are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of the specified System registers are not trapped by this mechanism.

Regardless of the value of this field, if event counter n is not implemented, a write of SPMEVCNTR<n>_EL0 is undefined.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMSSCR_EL1, bit [7]
When FEAT_PMUv3_SS is implemented:

Trap `MSR` writes of PMSSCR_EL1 at EL1 using AArch64 to EL2.

nPMSSCR_EL1	Meaning
`0b0`	If EL2 is implemented and enabled in the current Security state, then `MSR` writes of PMSSCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value `0x18`, unless the write generates a higher priority exception.
`0b1`	`MSR` writes of PMSSCR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [6]

Reserved, res0.

nMDSELR_EL1, bit [5]
When FEAT_Debugv8p9 is implemented:

Trap `MSR` writes of MDSELR_EL1 at EL1 using AArch64 to EL2.

nMDSELR_EL1	Meaning
`0b0`	If EL2 is implemented and enabled in the current Security state, then `MSR` writes of MDSELR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value `0x18`, unless the write generates a higher priority exception.
`0b1`	`MSR` writes of MDSELR_EL1 are not trapped by this mechanism.

It is implementation defined whether this field is implemented or is res0 when 16 or fewer breakpoints are implemented, 16 or fewer watchpoints are implemented, and MDSELR_EL1 is implemented as RAZ/WI.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMUACR_EL1, bit [4]
When FEAT_PMUv3p9 is implemented:

Trap MSR writes of PMUACR_EL1 at EL1 using AArch64 to EL2.

nPMUACR_EL1	Meaning
0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of PMUACR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of PMUACR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMICFILTR_EL0, bit [3]
When FEAT_PMUv3_ICNTR is implemented:

Trap MSR writes of PMICFILTR_EL0 at EL1 and EL0 using AArch64 to EL2.

nPMICFILTR_EL0	Meaning
0b0	If EL2 is implemented and enabled in the current Secu HCR_EL2.{E2H, TGE} != {1, 1}, then: • MSR writes of PMICFILTR_EL0 at EL1 and EL0 trapped to EL2 and reported with EC syndrom the write generates a higher priority exceptior • PMCNTENCLR_EL0.F0, PMCNTENSET_EL0.F PMOVSCLR_EL0.F0, and PMOVSSET_EL0.F0 and EL0. • PMINTENCLR_EL1.F0 and PMINTENSET_EL1 EL1.
0b1	MSR writes of PMICFILTR_EL0 are not trapped by this

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMICNTR_EL0, bit [2]
When FEAT_PMUv3_ICNTR is implemented:

Trap MSR writes of PMICNTR_EL0 at EL1 and EL0 using AArch64 to EL2.

nPMICNTR_EL0	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, and HCR_EL2. {E2H, TGE} != {1, 1}, then: • MSR writes of PMICNTR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception. • PMZR_EL0.F0 ignores writes at EL1 and EL0.
0b1	MSR writes of PMICNTR_EL0 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMIAR_EL1, bit [1]
When FEAT_SEBEP is implemented:

Trap MSR writes of PMIAR_EL1 at EL1 using AArch64 to EL2.

nPMIAR_EL1	Meaning
0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of PMIAR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of PMIAR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

nPMECR_EL1, bit [0]
When FEAT_EBEP is implemented or FEAT_PMUv3_SS is implemented:

Trap MSR writes of PMECR_EL1 at EL1 using AArch64 to EL2.

nPMECR_EL1	Meaning

0b0	If EL2 is implemented and enabled in the current Security state, then MSR writes of PMECR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.
0b1	MSR writes of PMECR_EL1 are not trapped by this mechanism.

This field is ignored by the PE and treated as zero when all of the following are true:

- EL3 is implemented.
- SCR_EL3.FGTEn2 == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Accessing HDFGWTR2_EL2

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, HDFGWTR2_EL2

op0	op1	CRn	CRm	op2
0b11	0b100	0b0011	0b0001	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
```

```
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        X[t, 64] = NVMem[0x1B0];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.FGTEn2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = HDFGWTR2_EL2;
elsif PSTATE.EL == EL3 then
    X[t, 64] = HDFGWTR2_EL2;
```

MSR HDFGWTR2_EL2, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b100	0b0011	0b0001	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x1B0] = X[t, 64];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.FGTEn2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        HDFGWTR2_EL2 = X[t, 64];
elsif PSTATE.EL == EL3 then
    HDFGWTR2_EL2 = X[t, 64];
```

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