PMPCSCTL, PC Sample-based Profiling Control Register

The PMPCSCTL characteristics are:

Purpose

Controls the PC Sample-based Profiling feature.

Configuration

This register is present only when FEAT_PCSRv8p9 is implemented. Otherwise, direct accesses to PMPCSCTL are res0.

PMPCSCTL is in the Core power domain.

Attributes

PMPCSCTL is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																											SS	RES0		IMP	EN

Bits [63:5]

Reserved, res0.

SS, bit [4]
When FEAT_PMUv3_SS is implemented:

Sample on Snapshot.

Controls whether the following registers are sampled on a PMU snapshot Capture event:

- If FEAT_PMUv3_EXT32 is implemented: PMU.PMCID1SR, PMU.PMCID2SR, PMU.PMPCSR, and PMU.PMVIDSR.
- If FEAT_PMUv3_EXT64 is implemented: PMU.PMCCIDSR, PMU.PMPCSR, and PMU.PMVCIDSR.

SS	Meaning
0b0	Sample on Read.
0b1	Sample on Snapshot.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

Otherwise:

Reserved, res0.

Bits [3:2]

Reserved, res0.

IMP, bit [1]

Profiling enable implemented.

IMP	Meaning
0b0	PMPCSCTL.EN reads-as-zero and ignores writes.
0b1	PMPCSCTL.EN is a read-write control bit.

This field has an implementation defined value.

Access to this field is **RO**.

EN, bit [0]
When PMU.PMPCSCTL.IMP == 1:

PC Sample-based Profiling Enable.

EN	Meaning
0b0	PC Sample-based Profiling is suspended.
0b1	PC Sample-based Profiling is active.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RAZ/WI.

Accessing PMPCSCTL

Accesses to this register use the following encodings:

```
Accessible at offset 0x230 from PMU
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- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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