<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding

Pseu

RORV

Rotate Right Variable provides the value of the contents of a register rotated by a variable number of bits. The bits that are rotated off the right end are inserted into the vacated bit positions on the left. The remainder obtained by dividing the second source register by the data size defines the number of bits by which the first source register is right-shifted.

This instruction is used by the alias **ROR** (register).

```
32-bit (sf == 0)

RORV <Wd>, <Wn>, <Wm>
64-bit (sf == 1)

RORV <Xd>, <Xn>, <Xm>

integer d = UInt (Rd);
integer n = UInt (Rn);
integer m = UInt (Rm);
```

constant integer datasize = 32 << UInt(sf);
ShiftType shift_type = DecodeShift(op2);</pre>

Assembler Symbols

<wd></wd>	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.
<wn></wn>	Is the 32-bit name of the first general-purpose source register, encoded in the "Rn" field.
<wm></wm>	Is the 32-bit name of the second general-purpose source register holding a shift amount from 0 to 31 in its bottom 5 bits, encoded in the "Rm" field.
<xd></xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.
<xn></xn>	Is the 64-bit name of the first general-purpose source register, encoded in the "Rn" field.
<xm></xm>	Is the 64-bit name of the second general-purpose source register holding a shift amount from 0 to 63 in its bottom 6 bits, encoded in the "Rm" field.

Operation

```
bits(datasize) result;
bits(datasize) operand2 = X[m, datasize];

result = ShiftReg(n, shift_type, UInt(operand2) MOD datasize, datasize)
X[d, datasize] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

<u>Base SIMD&FP SVE SME Index by Instructions Instructions Instructions Encoding</u>

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