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External Registers

GCSPR_EL0, Guarded Control Stack Pointer (EL0)

The GCSPR EL0 characteristics are:

Purpose

Contains the Guarded control stack pointer at ELO.

Configuration

This register is present only when FEAT_GCS is implemented. Otherwise, direct accesses to GCSPR EL0 are undefined.

Attributes

GCSPR EL0 is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

PTR[63:3]

PTR[63:3]

RESO
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PTR[63:3], bits [63:3]

ELO Guarded control stack pointer bits [63:3].

The reset behavior of this field is:

• On a Warm reset, this field resets to an architecturally unknown value.

Bits [2:0]

Reserved, res0.

Accessing GCSPR_EL0

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, GCSPR EL0

op0	op1	CRn	CRm	op2
0b11	0b011	0b0010	0b0101	0b001

```
if PSTATE.EL == ELO then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif (!EL2Enabled() | HCR_EL2.TGE != '1') &&
GCSCREO EL1.nTR == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.TGE == '1' &&
GCSCRE0 EL1.nTR == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3)
| SCR_EL3.FGTEn == '1') && HFGRTR_EL2.nGCS_EL0 ==
'0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = GCSPR\_EL0;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) |
SCR_EL3.FGTEn == '1') && HFGRTR_EL2.nGCS_EL0 == '0'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        X[t, 64] = GCSPR\_EL0;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
```

```
X[t, 64] = GCSPR_EL0;
elsif PSTATE.EL == EL3 then
X[t, 64] = GCSPR_EL0;
```

MSR GCSPR EL0, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b011	0b0010	0b0101	0b001

```
if PSTATE.EL == ELO then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) |
SCR_EL3.FGTEn == '1') && HFGWTR_EL2.nGCS EL0 == '0'
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        GCSPR\_EL0 = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        GCSPR\_EL0 = X[t, 64];
elsif PSTATE.EL == EL3 then
    GCSPR\_EL0 = X[t, 64];
```

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