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Pseu

PEXT (predicate)

Set predicate from predicate-as-counter

Expands the source predicate-as-counter into a four-predicate wide mask and copies one quarter of it into the destination predicate register.

SVE2 (FEAT_SVE2p1)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 0 1 0 0 1 0 1 size 1 0 0 0 0 0 0 1 1 1 0 0 mm2 PNn 1 Pd
```

```
PEXT <Pd>. <T>, <PNn>[<imm>]
```

```
if !HaveSME2() && !HaveSVE2p1() then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer n = UInt('1':PNn);
integer d = UInt(Pd);
integer part = UInt(imm2);</pre>
```

Assembler Symbols

<Pd>

Is the name of the destination scalable predicate register, encoded in the "Pd" field.

<T>

Is the size specifier, encoded in "size":

size	<t></t>
0.0	В
01	Н
10	S
11	D

<PNn>

Is the name of the first source scalable predicate register PN8-PN15, with predicate-as-counter encoding, encoded in the "PNn" field.

<imm>

Is the element index, in the range 0 to 3, encoded in the "imm2" field.

Operation

```
if HaveSVE2p1() then CheckSVEEnabled(); else CheckStreamingSVEEnabled()
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV esize;
bits(PL) pred = P[n, PL];
bits(PL*4) mask = CounterToPredicate(pred<15:0>, PL*4);
```

```
bits(PL) result;
constant integer psize = esize DIV 8;

for e = 0 to elements-1
   bit pbit = PredicateElement(mask, part * elements + e, esize);
   Elem[result, e, psize] = ZeroExtend(pbit, psize);

P[d, PL] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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