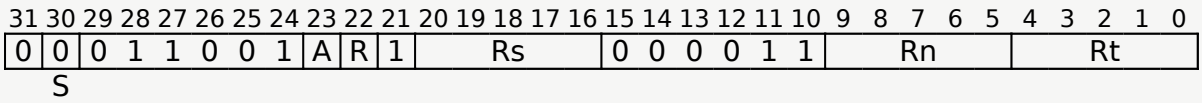
RCWCASP, RCWCASPA, RCWCASPL, RCWCASPAL

Read Check Write Compare and Swap quadword in memory reads a 128-bit quadword from memory, and compares it against the value held in a pair of registers. If the comparison is equal, the value in a second pair of registers is conditionally written to memory. Storing back to memory is conditional on RCW Checks. If the write is performed, the read and the write occur atomically such that no other modification of the memory location can take place between the read and the write. This instruction updates the condition flags based on the result of the update of memory.

- `RCWCASPA` and `RCWCASPAL` load from memory with acquire semantics.
- `RCWCASPL` and `RCWCASPAL` store to memory with release semantics.
- `RCWCASP` has neither acquire nor release semantics.

Integer
(FEAT_D128 && FEAT_THE)



RCWCASP (A == 0 && R == 0)

```
RCWCASP <Xs>, <X(s+1)>, <Xt>, <X(t+1)>, [<Xn|SP>]
```

RCWCASPA (A == 1 && R == 0)

```
RCWCASPA <Xs>, <X(s+1)>, <Xt>, <X(t+1)>, [<Xn|SP>]
```

RCWCASPAL (A == 1 && R == 1)

```
RCWCASPAL <Xs>, <X(s+1)>, <Xt>, <X(t+1)>, [<Xn|SP>]
```

RCWCASPL (A == 0 && R == 1)

```
RCWCASPL <Xs>, <X(s+1)>, <Xt>, <X(t+1)>, [<Xn|SP>]
```

```
if !IsFeatureImplemented(FEAT_D128) || !IsFeatureImplemented(FEAT_THE)
if Rs<0> == '1' then UNDEFINED;
if Rt<0> == '1' then UNDEFINED;
integer t = UInt(Rt);
integer n = UInt(Rn);
integer s = UInt(Rs);

boolean acquire = A == '1';
boolean release = R == '1';
boolean tagchecked = n != 31;
```

Assembler Symbols

<Xs>	Is the 64-bit name of the first general-purpose register to be compared and loaded, encoded in the "Rs" field. <Xs> must be an even-numbered register.
<X(s+1)>	Is the 64-bit name of the second general-purpose register to be compared and loaded.
<Xt>	Is the 64-bit name of the first general-purpose register to be conditionally stored, encoded in the "Rt" field. <Xt> must be an even-numbered register.
<X(t+1)>	Is the 64-bit name of the second general-purpose register to be conditionally stored.
<Xn|SP>	Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field.

Operation

```
if !IsD128Enabled(PSTATE.EL) then UNDEFINED;
bits(64) address;
bits(128) newdata;
bits(128) compdata;
bits(128) readdata;
bits(4) nzcv;

bits(64) s1 = X[s, 64];
bits(64) s2 = X[s+1, 64];
bits(64) t1 = X[t, 64];
bits(64) t2 = X[t+1, 64];

AccessDescriptor accdesc = CreateAccDescRCW(MemAtomicOp_CAS, FALSE, acq

compdata = if BigEndian(accdesc.acctype) then s1:s2 else s2:s1;
newdata = if BigEndian(accdesc.acctype) then t1:t2 else t2:t1;

if n == 31 then
    CheckSPAlignment();
    address = SP[];
else
    address = X[n, 64];

(nzcv, readdata) = MemAtomicRCW(address, compdata, newdata, accdesc);

PSTATE.<N,Z,C,V> = nzcv;
```

```
if BigEndian(accdesc.acctype) then
    X[s, 64] = readdata<127:64>;
    X[s+1, 64] = readdata<63:0>;
else
    X[s, 64] = readdata<63:0>;
    X[s+1, 64] = readdata<127:64>;
```

Operational information

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

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