ID_AA64MMFR3_EL1, AArch64 Memory Model Feature Register 3

The ID_AA64MMFR3_EL1 characteristics are:

Purpose

Provides information about the implemented memory model and memory management support in AArch64 state.

Configuration

Note

Prior to the introduction of the features described by this register, this register was unnamed and reserved, res0 from EL1, EL2, and EL3.

Attributes

ID_AA64MMFR3_EL1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Spec_FPACC				ADERR				SDERR				RES0				ANERR				SNERR				D128_2				D128			
MEC				AIE				S2POE				S1POE				S2PIE				S1PIE				SCTLRX				TCRX			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Spec_FPACC, bits [63:60]
When FEAT_FPACCOMBINE is implemented:

Speculative behavior in the event of a PAC authentication failure in an implementation that includes FEAT_FPACCOMBINE. Defined values are:

Spec_FPACC	Meaning

0b0000	The implementation does not disclose whether the speculative use of pointers processed by a PAC Authentication is materially different in terms of the impact on cached microarchitectural state between passing and failing of the PAC Authentication.
0b0001	The speculative use of pointers processed by a PAC Authentication is not materially different in terms of the impact on cached microarchitectural state between passing and failing of the PAC Authentication.

All other values are reserved.

For the purpose of this definition, cached microarchitecture state is the state of caching agents such as instruction caches, data caches and TLBs which can be altered as a result of speculation caused by a mispredicted execution, but is not restored to the state prior to the speculation when the misprediction is corrected.

Otherwise:

Reserved, res0.

ADERR, bits [59:56]

Asynchronous Device error exceptions. With ID_AA64MMFR3_EL1.SDERR, describes the PE behavior for error exceptions on Device memory loads. Defined values are:

ADERR	Meaning
0b0000	If FEAT_RASv2 is not implemented and ID_AA64MMFR3_EL1.SDERR is 0b0000, then the behavior is not described. Otherwise, the behavior is described by ID_AA64MMFR3_EL1.SDERR.

0b0001	Some error exceptions for Device memory loads are taken asynchronously.
0b0010	FEAT_ADERR is implemented. SCTLR2_ELx.EnADERR and HCRX_EL2.EnSDERR are implemented.

All other values are reserved.

When FEAT_RASv2 is implemented and ID_AA64MMFR3_EL1.SDERR is 0b0000, the value of this field is 0b0001.

When ID_AA64MMFR3_EL1.SDERR is 0b0001, the value of this field is 0b0000.

When ID_AA64MMFR3_EL1.SDERR is 0b0010, the value of this field is 0b0010.

FEAT_ADERR implements the functionality described by the value 0b0010.

SDERR, bits [55:52]

Synchronous Device error exceptions. With ID_AA64MMFR3_EL1.ADERR, describes the PE behavior for error exceptions on Device memory loads. Defined values are:

SDERR	Meaning
0b0000	If FEAT_RASv2 is not implemented and ID_AA64MMFR3_EL1.ADERR is 0b0000, then the behavior is not described. Otherwise, the behavior is described by ID_AA64MMFR3_EL1.ADERR.
0b0001	All error exceptions for Device memory loads are taken synchronously.
0b0010	FEAT_ADERR is implemented. SCTLR2_ELx.EnADERR and HCRX_EL2.EnSDERR are implemented.

All other values are reserved.

When FEAT_RASv2 is implemented and ID_AA64MMFR3_EL1.ADERR is 0b0000, the value of this field is 0b0001.

When ID_AA64MMFR3_EL1.ADERR is 0b0001, the value of this field is 0b0000.

When ID_AA64MMFR3_EL1.ADERR is 0b0010, the value of this field is 0b0010.

FEAT_ADERR implements the functionality described by the value 0b0010.

Bits [51:48]

Reserved, res0.

ANERR, bits [47:44]

Asynchronous Normal error exceptions. With ID_AA64MMFR3_EL1.SNERR, describes the PE behavior for error exceptions on Normal memory loads. Defined values are:

ANERR	Meaning
0b0000	If FEAT_RASv2 is not implemented and ID_AA64MMFR3_EL1.SNERR is 0b0000, then the behavior is not described. Otherwise, the behavior is described by ID_AA64MMFR3_EL1.SNERR.
0b0001	Some error exceptions for Normal memory loads are taken asynchronously.
0b0010	FEAT_ANERR is implemented. SCTLR2_ELx.EnANERR and HCRX_EL2.EnSNERR are implemented.

All other values are reserved.

When FEAT_RASv2 is implemented and ID_AA64MMFR3_EL1.SNERR is 0b0000, the value of this field is 0b0001.

When ID_AA64MMFR3_EL1.SNERR is 0b0001, the value of this field is 0b0000.

When ID_AA64MMFR3_EL1.SNERR is 0b0010, the value of this field is 0b0010.

FEAT_ANERR implements the functionality described by the value 0b0010.

SNERR, bits [43:40]

Synchronous Normal error exceptions. With ID_AA64MMFR3_EL1.ANERR, describes the PE behavior for error exceptions on Normal memory loads. Defined values are:

SNERR	Meaning
0b0000	If FEAT_RASv2 is not implemented and ID_AA64MMFR3_EL1.ANERR is 0b0000, then the behavior is not described. Otherwise, the behavior is described by ID_AA64MMFR3_EL1.ANERR.
0b0001	All error exceptions for Normal memory loads are taken synchronously.
0b0010	FEAT_ANERR is implemented. SCTLR2_ELx.EnANERR and HCRX_EL2.EnSNERR are implemented.

All other values are reserved.

When FEAT_RASv2 is implemented and ID_AA64MMFR3_EL1.ANERR is 0b0000, the value of this field is 0b0001.

When ID_AA64MMFR3_EL1.ANERR is 0b0001, the value of this field is 0b0000.

When ID_AA64MMFR3_EL1.ANERR is 0b0010, the value of this field is 0b0010.

FEAT_ANERR implements the functionality described by the value 0b0010.

D128_2, bits [39:36]

128-bit Page Table Descriptor at stage 2. Indicates support for 128-bit Page Table Descriptor at stage 2. Defined values are:

D128_2	Meaning
0b0000	128-bit Page Table Descriptor Extension at stage 2 is not supported.
0b0001	128-bit Page Table Descriptor Extension at stage 2 is supported.

All other values are reserved.

D128, bits [35:32]

128-bit Page Table Descriptor. Indicates support for 128-bit Page Table Descriptor. Defined values are:

D128	Meaning
0b0000	128-bit Page Table Descriptor Extension is not supported.
0b0001	128-bit Page Table Descriptor Extension is supported.

All other values are reserved.

MEC, bits [31:28]

Indicates support for Memory Encryption Contexts. Defined values are:

MEC	Meaning
0b0000	Memory Encryption Contexts is not supported.
0b0001	Memory Encryption Contexts is supported for Realm physical address space.

All other values are reserved.

FEAT_MEC implements the functionality identified by the value 0b0001.

AIE, bits [27:24]

Attribute Indexing. Indicates support for the Attribute Index Enhancement. Defined values are:

AIE	Meaning
0b0000	The Attribute Index Enhancement is not supported.
0b0001	The Attribute Index Enhancement at Stage 1 is supported.

All other values are reserved.

FEAT_AIE implements the functionality identified by the value 0b0001.

S2POE, bits [23:20]

Stage 2 Permission Overlay. Indicates support for Permission Overlay at Stage 2. Defined values are:

S2POE	Meaning
0b0000	Permission Overlay at Stage 2 is not supported.
0b0001	Permission Overlay at Stage 2 is supported.

All other values are reserved.

FEAT_S2POE implements the functionality identified by the value 0b0001.

S1POE, bits [19:16]

Stage 1 Permission Overlay. Indicates support for Permission Overlay at Stage 1. Defined values are:

S1POE	Meaning
0b0000	Permission Overlay at Stage 1 is not supported.
0b0001	Permission Overlay at Stage 1 is supported.

All other values are reserved.

FEAT_S1POE implements the functionality identified by the value 0b0001.

S2PIE, bits [15:12]

Stage 2 Permission Indirection. Indicates support for Permission Indirection at Stage 2. Defined values are:

S2PIE	Meaning
0b0000	Permission Indirection at Stage 2 is not supported.
0b0001	Permission Indirection at Stage 2 is supported.

All other values are reserved.

FEAT_S2PIE implements the functionality identified by the value 0b0001.

S1PIE, bits [11:8]

Stage 1 Permission Indirection. Indicates support for Permission Indirection at Stage 1. Defined values are:

S1PIE	Meaning
0b0000	Permission Indirection at Stage 1 is not supported.

0b0001	Permission Indirection at Stage 1 is supported.

All other values are reserved.

FEAT_S1PIE implements the functionality identified by the value 0b0001.

SCTLRX, bits [7:4]

SCTLRX Extension. Indicates support for Extension of SCTLR_EL1. Defined values are:

SCTLRX	Meaning
0b0000	SCTLR2_EL1, SCTLR2_EL2 and their associated trap controls are not implemented.
0b0001	SCTLR2_EL1, SCTLR2_EL2 and their associated trap controls are implemented.

All other values are reserved.

TCRX, bits [3:0]

TCR Extension. Indicates support for Extension of TCR_EL1. Defined values are:

TCRX	Meaning
0b0000	TCR2_EL1, TCR2_EL2 and their associated trap controls are not implemented.
0b0001	TCR2_EL1, TCR2_EL2 and their associated trap controls are implemented.

All other values are reserved.

Accessing ID_AA64MMFR3_EL1

Accesses to this register use the following encodings in the System register encoding space:

```
MRS <Xt>, ID_AA64MMFR3_EL1
```

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0111	0b011

```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() &&
(IsFeatureImplemented(FEAT_FGT) || !
IsZero(ID_AA64MMFR3_EL1) || boolean
IMPLEMENTATION_DEFINED "ID_AA64MMFR3_EL1 trapped by
HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AA64MMFR3_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64MMFR3_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64MMFR3_EL1;
```

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94