PMZR_EL0, Performance Monitors Zero with Mask

The PMZR_EL0 characteristics are:

Purpose

Zero the set of counters specified by the mask written to PMZR_EL0.

Configuration

External register PMZR_EL0 bits [63:0] are architecturally mapped to AArch64 System register PMZR_EL0[63:0].

This register is present only when FEAT_PMUv3_EXT64 is implemented and FEAT_PMUv3p9 is implemented. Otherwise, direct accesses to PMZR_EL0 are res0.

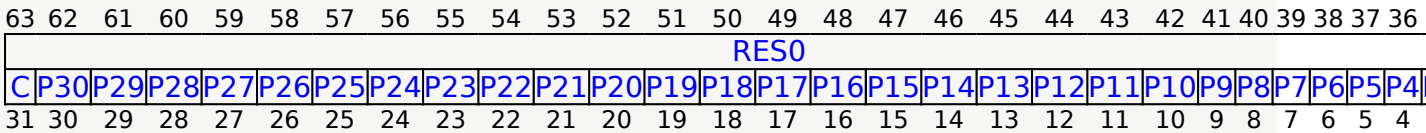
PMZR_EL0 is in the Core power domain.

Attributes

PMZR_EL0 is a 64-bit register.

This register is part of the PMU block.

Field descriptions



Bits [63:33]

Reserved, res0.

F<m>, bit [m+32], for m = 0
When FEAT_PMUv3_ICNTR is implemented:

Zero fixed-function counter <m>.

F<m>	Meaning
0b0	Write is ignored.

0b1	Set fixed-function counter <m> to zero.

Writing 1 to PMZR_EL0.F0 sets PMU.PMICNTR_EL0 to zero.

Otherwise:

Reserved, res0.

C, bit [31]

Zero PMU.PMCCNTR_EL0.

C	Meaning
0b0	Write is ignored.
0b1	Set PMU.PMCCNTR_EL0 to zero.

P<m>, bit [m], for m = 30 to 0

Zero PMEVCNTR<m>_EL0.

P<m>	Meaning
0b0	Write is ignored.
0b1	Set PMEVCNTR<m>_EL0 to zero.

Accessing PMZR_EL0

Accesses to this register use the following encodings:

Accessible at offset 0xCA0 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **WI**.
- Otherwise, accesses to this register are **WO**.