

PUNPKHI, PUNPKLO

Unpack and widen half of predicate

Unpack elements from the lowest or highest half of the source predicate and place in elements of twice their size within the destination predicate. This instruction is unpredicated.

It has encodings from 2 classes: [High half](#) and [Low half](#)

High half

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	Pn			0	Pd				
H																															

PUNPKHI [<Pd>](#).H, [<Pn>](#).B

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
constant integer esize = 16;
integer n = UInt(Pn);
integer d = UInt(Pd);
boolean hi = TRUE;
```

Low half

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	Pn			0	Pd			
H																															

PUNPKLO [<Pd>](#).H, [<Pn>](#).B

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
constant integer esize = 16;
integer n = UInt(Pn);
integer d = UInt(Pd);
boolean hi = FALSE;
```

Assembler Symbols

- [<Pd>](#) Is the name of the destination scalable predicate register, encoded in the "Pd" field.
- [<Pn>](#) Is the name of the source scalable predicate register, encoded in the "Pn" field.

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
```

```

constant integer elements = VL DIV esize;
bits(PL) operand = P[n, PL];
bits(PL) result;
constant integer psize = esize DIV 8;

for e = 0 to elements-1
    bit pbit = PredicateElement(operand, if hi then e + elements else e
    Elem[result, e, psize] = ZeroExtend(pbit, psize);

P[d, PL] = result;

```

Operational information

If FEAT_SVE2 is implemented or FEAT_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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Instructions](#)

[SIMD&FP
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[SVE
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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode
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