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## MOV (vector, unpredicated)

Move vector register (unpredicated)

Move vector register. This instruction is unpredicated.

This is an alias of ORR (vectors, unpredicated). This means:

- The encodings in this description are named to match the encodings of <u>ORR</u> (vectors, unpredicated).
- The description of <u>ORR (vectors, unpredicated)</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31 30 29 28 27 26 25 2	4 23 22 21 20 19	18 17 16 15 14 13 12	11 10 9 8 7 6 5	4 3 2 1 0
0 0 0 0 0 1 0	0 0 1 1 2	Zm 0011	0 0 Zn	Zd

## is equivalent to

ORR 
$$\langle Zd \rangle$$
.D,  $\langle Zn \rangle$ .D,  $\langle Zn \rangle$ .D

and is the preferred disassembly when Zn == Zm.

# **Assembler Symbols**

<Zd> Is the name of the destination scalable vector register,

encoded in the "Zd" field.

<Zn> Is the name of the first source scalable vector register,

encoded in the "Zn" field.

## **Operation**

The description of <u>ORR (vectors, unpredicated)</u> gives the operational pseudocode for this instruction.

#### **Operational information**

If FEAT\_SVE2 is implemented or FEAT\_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56

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