

TRBPIDR2, Peripheral Identification Register 2

The TRBPIDR2 characteristics are:

Purpose

Provides discovery information about the component.

For additional information, see the CoreSight Architecture Specification.

Configuration

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBPIDR2 are res0.

TRBPIDR2 is in the Core power domain.

Attributes

TRBPIDR2 is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																REVISION		JEDEC		DES 1											

Bits [31:8]

Reserved, res0.

REVISION, bits [7:4]

Component major revision. TRBPIDR2.REVISION and [TRBPIDR3](#).REVAND together form the revision number of the component, with TRBPIDR2.REVISION being the most significant part and [TRBPIDR3](#).REVAND the least significant part. When a component is changed, TRBPIDR2.REVISION or [TRBPIDR3](#).REVAND are increased to ensure that software can differentiate the different revisions of the component. [TRBPIDR3](#).REVAND should be set to 0b0000 when TRBPIDR2.REVISION is increased.

This field has an implementation defined value.

Access to this field is **RO**.

JEDEC, bit [3]

JEDEC-assigned JEP106 implementer code is used.

Reads as 0b1.

Access to this field is **RO**.

DES_1, bits [2:0]

Designer, JEP106 identification code, bits [6:4]. [TRBPIDR1](#).DES_0 and TRBPIDR2.DES_1 together form the JEDEC-assigned JEP106 identification code for the designer of the component. The parity bit in the JEP106 identification code is not included. The code identifies the designer of the component, which might not be the same as the implementer of the device containing the component. To obtain a number, or to see the assignment of these codes, contact JEDEC <http://www.jedec.org>.

Note

For a component designed by Arm Limited, the JEP106 identification code is 0x3B.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing TRBPIDR2

TRBPIDR2 can be accessed through the external debug interface:

Component	Offset	Instance
TRBE	0xFE8	TRBPIDR2

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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