# GCSCRE0_EL1, Guarded Control Stack Control (EL0)

The GCSCRE0_EL1 characteristics are:

## Purpose

Controls the Guarded control stack at EL0.

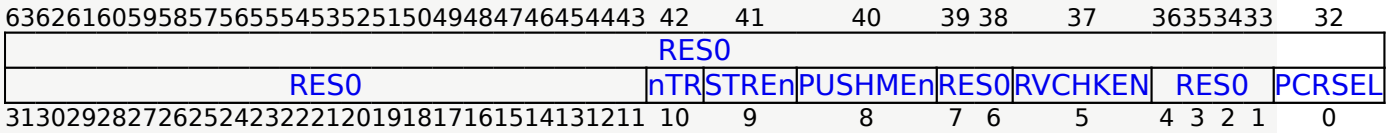
## Configuration

This register is present only when FEAT_GCS is implemented. Otherwise, direct accesses to GCSCRE0_EL1 are undefined.

## Attributes

GCSCRE0_EL1 is a 64-bit register.

## Field descriptions




### Bits [63:11]

Reserved, res0.

### nTR, bit [10]

Trap GCS register accesses from EL0.

| nTR | Meaning |
|---|---|
| 0b0 | Read accesses to GCSPR_EL0 at EL0 cause a Trap exception. |
| 0b1 | This control does not cause any instructions to be trapped. |

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

**STREn, bit [9]**

Execution of the following instructions are trapped:

- GCSSTR.
- GCSSTTR.

| STREn | Meaning |
|---|---|
| 0b0 | Execution of any of the specified instructions at EL0 cause a GCS exception. |
| 0b1 | This control does not cause any instructions to be trapped. |

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

**PUSHMEn, bit [8]**

Trap GCSPUSHM instruction.

| PUSHMEn | Meaning |
|---|---|
| 0b0 | Execution of a GCSPUSHM instruction at EL0 causes a Trap exception. |
| 0b1 | This control does not cause any instructions to be trapped. |

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

**Bits [7:6]**

Reserved, res0.

**RVCHKEN, bit [5]**

Return value check enable.

| RVCHKEN | Meaning |
|---|---|
| 0b0 | Return value checking disabled at EL0. |
| 0b1 | Return value checking enabled at EL0. |

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

#### Bits [4:1]

Reserved, res0.

#### PCRSEL, bit [0]

Guarded control stack procedure call return enable selection.

| PCRSEL | Meaning |
|---|---|
| 0b0 | Guarded control stack at EL0 is not PCR Selected. |
| 0b1 | Guarded control stack at EL0 is PCR Selected. |

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

## Accessing GCSCRE0_EL1

Accesses to this register use the following encodings in the System register encoding space:

### MRS <Xt>, GCSCRE0_EL1

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b000 | 0b0010 | 0b0101 | 0b010 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGRTR_EL2.nGCS_EL0 == '0'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
```

```
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = GCSCRE0_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = GCSCRE0_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = GCSCRE0_EL1;
```

# MSR GCSCRE0_EL1, <Xt>

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b000 | 0b0010 | 0b0101 | 0b010 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGWTR_EL2.nGCS_EL0 == '0'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        GCSCRE0_EL1 = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.GCSEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.GCSEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
```

```
            GCSCRE0_EL1 = X[t, 64];
    elsif PSTATE.EL == EL3 then
        GCSCRE0_EL1 = X[t, 64];
```

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