

## LUT14 (four registers)

Lookup table read with 4-bit indexes

Copy 16-bit or 32-bit elements from ZT0 to four destination vectors using packed 4-bit indices from a segment of the source vector register. A segment corresponds to a portion of the source vector that is consumed in order to fill the destination vector. The segment is selected by the vector segment index modulo the total number of segments.

This instruction is unpredicated.

It has encodings from 2 classes: [Consecutive](#) and [Strided](#)

### Consecutive (FEAT\_SME2)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	1	0	0	0	1	0	1	i1	1	0	size	0	0				Zn			Zd	0	0		

**LUT14** { [<Zd1>](#).[<T>](#) - [<Zd4>](#).[<T>](#) }, ZT0, [<Zn>](#)[[<index>](#)]

```
if !HaveSME2() then UNDEFINED;
if size == '00' || size == '11' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer isize = 4;
integer n = UInt(Zn);
integer dstride = 1;
integer d = UInt(Zd:'00');
integer imm = UInt(i1);
constant integer nreg = 4;
```

### Strided (FEAT\_SME2p1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	1	0	0	1	1	0	1	i1	1	0	size	0	0				Zn			D	0	0	Zd	

**LUT14** { [<Zd1>](#).H, [<Zd2>](#).H, [<Zd3>](#).H, [<Zd4>](#).H }, ZT0, [<Zn>](#)[[<index>](#)]

```
if !HaveSME2p1() then UNDEFINED;
if size != '01' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer isize = 4;
integer n = UInt(Zn);
integer dstride = 4;
integer d = UInt(D:'00':Zd);
integer imm = UInt(i1);
constant integer nreg = 4;
```

## Assembler Symbols

- <Zd1>** For the consecutive variant: is the name of the first destination scalable vector register of a multi-vector sequence, encoded as "Zd" times 4.
- For the strided variant: is the name of the first destination scalable vector register Z0-Z3 or Z16-Z19 of a multi-vector sequence, encoded as "D:'00':Zd".
- <Zd2>** Is the name of the second destination scalable vector register Z4-Z7 or Z20-Z23 of a multi-vector sequence, encoded as "D:'01':Zd".
- <Zd3>** Is the name of the third destination scalable vector register Z8-Z11 or Z24-Z27 of a multi-vector sequence, encoded as "D:'10':Zd".
- <T>** Is the size specifier, encoded in "size":

size	<T>
00	RESERVED
01	H
10	S
11	RESERVED

- <Zd4>** For the consecutive variant: is the name of the fourth destination scalable vector register of a multi-vector sequence, encoded as "Zd" times 4 plus 3.
- For the strided variant: is the name of the fourth destination scalable vector register Z12-Z15 or Z28-Z31 of a multi-vector sequence, encoded as "D:'11':Zd".
- <Zn>** Is the name of the source scalable vector register, encoded in the "Zn" field.
- <index>** Is the vector segment index, in the range 0 to 1, encoded in the "i1" field.

## Operation

```
CheckStreamingSVEEnabled\(\) ;  
CheckSMEZT0Enabled\(\) ;  
constant integer VL = CurrentVL ;  
constant integer elements = VL DIV esize ;  
integer segments = esize DIV (isize * nreg) ;  
integer segment = imm MOD segments ;  
bits(VL) indexes = Z[n, VL] ;  
bits(512) table = ZT0[512] ;  
  
for r = 0 to nreg-1  
    integer base = (segment * nreg + r) * elements ;  
    bits(VL) result ;
```

```

for e = 0 to elements-1
    integer index = UInt(Elem[indexes, base+e, isize]);
    Elem[result, e, esize] = Elem[table, index, 32]<esize-1:0>;
    Z[d, VL] = result;
    d = d + dstride;

```

## Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

[Base  
Instructions](#)

[SIMD&FP  
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[SVE  
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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56

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