EDECR, External Debug Execution Control Register

The EDECR characteristics are:

Purpose

Controls Halting debug events.

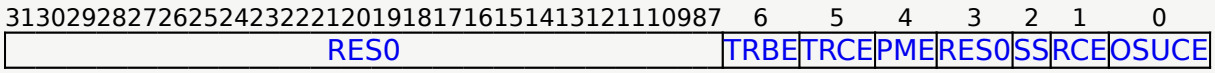
Configuration

When FEAT_DoPD is implemented, EDECR is in the Core power domain. Otherwise, EDECR is in the Debug power domain.

Attributes

EDECR is a 32-bit register.

Field descriptions



Bits [31:7]

Reserved, res0.

TRBE, bit [6]
When FEAT_Debugv8p9 is implemented and FEAT_TRBE_EXT is implemented:

Trace Buffer External Debug Request Enable.

TRBE	Meaning
0b0	Trace Buffer External Debug Request disabled.
0b1	Trace Buffer External Debug Request enabled.

This field is in the Core power domain.

The reset behavior of this field is:

- On a Cold reset, this field resets to 0.

Otherwise:

Reserved, res0.

TRCE, bit [5]
When FEAT_ETEv1p3 is implemented and FEAT_Debugv8p9 is implemented:

ETE External Debug Request Enable.

TRCE	Meaning
0b0	ETE External Debug Request disabled.
0b1	ETE External Debug Request enabled.

This field is in the Core power domain.

The reset behavior of this field is:

- On a Cold reset, this field resets to 0.

Otherwise:

Reserved, res0.

PME, bit [4]
When FEAT_Debugv8p9 is implemented and FEAT_PMUv3p9 is implemented:

PMU Overflow External Debug Request Enable.

PME	Meaning
0b0	PMU Overflow External Debug Request disabled.
0b1	PMU Overflow External Debug Request enabled.

This field is in the Core power domain.

The reset behavior of this field is:

- On a Cold reset, this field resets to 0.

Otherwise:

Reserved, res0.

Bit [3]

Reserved, res0.

SS, bit [2]

Halting step enable. Possible values of this field are:

SS	Meaning
0b0	Halting step debug event disabled.
0b1	Halting step debug event enabled.

If the value of EDECR.SS is changed when the PE is in Non-debug state, behavior is constrained unpredictable as described in 'Changing the value of EDECR.SS when not in Debug state'.

The reset behavior of this field is:

- On a Cold reset, when FEAT_DoPD is implemented, this field resets to 0.
- On an External debug reset, when FEAT_DoPD is not implemented, this field resets to 0.

RCE, bit [1]
When FEAT_DoPD is not implemented:

Reset Catch Enable.

RCE	Meaning
0b0	Reset Catch debug event disabled.
0b1	Reset Catch debug event enabled.

The reset behavior of this field is:

- On an External debug reset, this field resets to 0.

Otherwise:

Reserved, res0.

OSUCE, bit [0]
When FEAT_DoPD is not implemented:

OS Unlock Catch Enable.

OSUCE	Meaning
0b0	OS Unlock Catch debug event disabled.

0b1	OS Unlock Catch debug event enabled.

The reset behavior of this field is:

- On an External debug reset, this field resets to 0.

Otherwise:

Reserved, res0.

Accessing EDECR

EDECR can be accessed through the external debug interface:

Component	Offset	Instance
Debug	0x024	EDECR

This interface is accessible as follows:

- When (FEAT_DoPD is not implemented or IsCorePowered()) and SoftwareLockStatus(), accesses to this register are **RO**.
- When (FEAT_DoPD is not implemented or IsCorePowered()) and ! SoftwareLockStatus(), accesses to this register are **RW**.
- Otherwise, accesses to this register generate an error response.

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