

## SHA256H2

SHA256 hash update (part 2).

### Advanced SIMD (FEAT\_SHA256)

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |    |   |   |   |    |   |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|----|---|---|---|----|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5  | 4 | 3 | 2 | 1  | 0 |
| 0  | 1  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  |    |    |    |    | Rm |    | 0  | 1  | 0  | 1  | 0  | 0 |   |   |   | Rn |   |   |   | Rd |   |

P

**SHA256H2** **<Qd>**, **<Qn>**, **<Vm>**.4S

```
integer d = UInt(Rd);
integer n = UInt(Rn);
integer m = UInt(Rm);
if !IsFeatureImplemented(FEAT_SHA256) then UNDEFINED;
```

### Assembler Symbols

- <Qd>** Is the 128-bit name of the SIMD&FP source and destination, encoded in the "Rd" field.
- <Qn>** Is the 128-bit name of the second SIMD&FP source register, encoded in the "Rn" field.
- <Vm>** Is the name of the third SIMD&FP source register, encoded in the "Rm" field.

### Operation

```
AArch64.CheckFPAdvSIMDEnabled();
bits(128) result;
result = SHA256hash(V[n, 128], V[d, 128], V[m, 128], FALSE);
V[d, 128] = result;
```

### Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
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