

CTICONTROL, CTI Control register

The CTICONTROL characteristics are:

Purpose

Controls whether the CTI is enabled.

Configuration

CTICONTROL is in the Debug power domain.

Attributes

CTICONTROL is a 32-bit register.

Field descriptions

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | GLBEN |

Bits [31:1]

Reserved, res0.

GLBEN, bit [0]

Enables or disables the CTI mapping functions. Possible values of this field are:

| GLBEN | Meaning |
|-------|---|
| 0b0 | CTI mapping functions and application trigger disabled. |
| 0b1 | CTI mapping functions and application trigger enabled. |

When GLBEN is 0, the input channel to output trigger, input trigger to output channel, and application trigger functions are disabled and do not signal new events on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it is constrained unpredictable which of the following occurs:

- The output trigger remains asserted after the mapping functions are disabled.

- The output trigger is deasserted after the mapping functions are disabled.

All output triggers are disabled by CTI reset.

If the ECT supports multicycle channel events any existing output channel events will be terminated.

The reset behavior of this field is:

- On an External debug reset, this field resets to 0.

Accessing CTICONTROL

CTICONTROL can be accessed through the external debug interface:

| Component | Offset | Instance |
|-----------|--------|------------|
| CTI | 0x000 | CTICONTROL |

This interface is accessible as follows:

- When SoftwareLockStatus(), accesses to this register are **RO**.
- When !SoftwareLockStatus(), accesses to this register are **RW**.

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