# ICC_SRE_EL3, Interrupt Controller System Register Enable Register (EL3)

The ICC_SRE_EL3 characteristics are:

## Purpose

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL3.

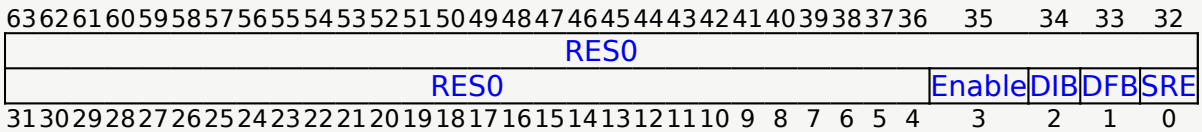
## Configuration

This register is present only when FEAT_GICv3 is implemented and EL3 is implemented. Otherwise, direct accesses to ICC_SRE_EL3 are undefined.

## Attributes

ICC_SRE_EL3 is a 64-bit register.

## Field descriptions




### Bits [63:4]

Reserved, res0.

### Enable, bit [3]

Enable. Enables lower Exception level access to ICC_SRE_EL1 and ICC_SRE_EL2.

| Enable | Meaning |
|---|---|
| 0b0 | EL1 accesses to ICC_SRE_EL1 trap to EL3, unless these accesses are trapped to EL2 as a result of ICC_SRE_EL2.Enable == 0. EL2 accesses to ICC_SRE_EL1 and ICC_SRE_EL2 trap to EL3. |

| | |
|---|---|
| 0b1 | EL1 accesses to ICC_SRE_EL1 do not trap to EL3.<br>EL2 accesses to ICC_SRE_EL1 and ICC_SRE_EL2 do not trap to EL3. |

If ICC_SRE_EL3.SRE is RAO/WI, an implementation is permitted to make the Enable bit RAO/WI.

If ICC_SRE_EL3.SRE is 0, the Enable bit behaves as 1 for all purposes other than reading the value of the bit.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

**DIB, bit [2]**

Disable IRQ bypass.

| DIB | Meaning |
|---|---|
| 0b0 | IRQ bypass enabled. |
| 0b1 | IRQ bypass disabled. |

In systems that do not support IRQ bypass, this bit is RAO/WI.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

**DFB, bit [1]**

Disable FIQ bypass.

| DFB | Meaning |
|---|---|
| 0b0 | FIQ bypass enabled. |
| 0b1 | FIQ bypass disabled. |

In systems that do not support FIQ bypass, this bit is RAO/WI.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

**SRE, bit [0]**

System Register Enable.

| SRE | Meaning |
|---|---|

| | |
|---|---|
| 0b0 | The memory-mapped interface must be used. Access at EL3 to any ICH_* or ICC_* register other than ICC_SRE_EL1, ICC_SRE_EL2, or ICC_SRE_EL3 is trapped to EL3 |
| 0b1 | The System register interface to the ICH_* registers and the EL1, EL2, and EL3 ICC_* registers is enabled for EL3. |

If software changes this bit from 1 to 0, the results are unpredictable.

If Realm Management Extension is implemented, this field is RAO/WI.

FEAT_GICv3 implementations that do not require GICv2 compatibility might choose to make this bit RAO/WI.

The reset behavior of this field is:

- On a Warm reset, this field resets to 0.

## Accessing ICC_SRE_EL3

This register is always System register accessible.

Accesses to this register use the following encodings in the System register encoding space:

### MRS <Xt>, ICC_SRE_EL3

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b110 | 0b1100 | 0b1100 | 0b101 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ICC_SRE_EL3;
```

# MSR ICC_SRE_EL3, <Xt>

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b110 | 0b1100 | 0b1100 | 0b101 |

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    ICC_SRE_EL3 = X[t, 64];
```

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