AArch32	AArch64	AArch32	AArch64	Index by	<u>External</u>
<u>Registers</u>	<u>Registers</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding	<u>Registers</u>

PMU

The PMU characteristics are:

Attributes

PMU is a block of size: 4096 bytes

Contents

Offset	Name A
0x000 + (8 * n) for n in 30:0	PMEVCNTR <n>_EL0</n>
0x000 + (8 * n) for n in 30:0	PMEVCNTR <n>_EL0 F</n>
0x000 + (8 * n) for n in 30:0	PMEVCNTR <n>_EL0 F</n>
0x0F8	PMCCNTR_EL0 F
0x0F8	PMCCNTR_EL0 F
0x0FC	PMCCNTR_EL0[63:32] F
0x100	PMICNTR_EL0 F

0x200	<u>PMPCSR</u>	FI
0x200	<u>PMPCSR</u>	FI
0x204	PMPCSR[63:32]	FI
0x208	<u>PMVCIDSR</u>	FI
0x208	PMCID1SR	FI
0x20C	<u>PMVIDSR</u>	FI
0x220	<u>PMPCSR</u>	FI
0x220	PMPCSR	FI
0x224	PMPCSR[63:32]	FI

0x228	<u>PMCCIDSR</u>	FI
0x228	PMCID1SR	FI
0x22C	PMCID2SR	FI
0x230	<u>PMPCSCTL</u>	F
0x400 + (8 * n) for n in 30:0	PMEVTYPER <n>_EL0[63:0]</n>	FI
0x400 + (4 * n) for n in 30:0	PMEVTYPER <n>_EL0[31:0]</n>	FI
0x47C	PMCCFILTR_EL0[31:0]	FI
0×480	PMICFILTR_EL0[31:0]	FI is FI
0x4F8	PMCCFILTR_EL0	FI
0x500	PMICFILTR_EL0	FI is FI
0x600 + (8 * n) for n in 30:0	PMEVCNTSVR <n>_EL1</n>	F
0×6F8	PMCCNTSVR_EL1	F
0x700	PMICNTSVR_EL1	F
		FI

$0 \times 800 \hat{A} + \hat{A}$ (4)	* n) forÂ	n in 63:0	PMEVFILT2R <n>[31:0]</n>	FE
022003 13 70	* n) forÂ	nñ inñ 62.0	PMEVFILT2R <n>[63:0]</n>	
UXOUUA TA (O.	A "A II) A IOIA	IIA IIIA 05.0	I MEVI IEIZK\II>[03.0]	FF
0xA00Â +Â (4	* n) forÂ	n in 30:0	PMEVTYPER <n>_EL0[63:32]</n>	
				FF
				(F
				ŀ
	0xA7C		PMCCFILTR_EL0[63:32]	
	01111		THOUTIER ENGINEER	FI
				15 (F
				l I
			DMIOCHED ELOICO 221	
	08Ax0		PMICFILTR_EL0[63:32]	FF
				is FE
			DA COMPENSORE EL O	
	0xC00		PMCNTENSET_EL0	FI
				i FE
				j
	0xC00		PMCNTENSET_EL0	FF
				FE
				is
				aı is
	0xC10		<u>PMCNTEN</u>	
				F
				-

0xC20	PMCNTENCLR_EL0	FI
		i
		FE
		J
0xC20	PMCNTENCLR_EL0	FI
		FE
		aı
		is
0xC40	PMINTENSET_EL1	F
		i
		FE
		I
	DMINITENIOPT PLA	
0xC40	PMINTENSET_EL1	F
		FE
		aı
0xC50	<u>PMINTEN</u>	is
UACSU	THINTLIN	FF
0xC60	PMINTENCLR_EL1	F
		i
		FE
0.000	DMINITENIOLD EL1	+
0xC60	PMINTENCLR_EL1	FI
		FI
		is
		aı
		is

	I	
0xC80	PMOVSCLR_EL0	FI
		i FI
] j
0xC80	PMOVSCLR_EL0	FI
		FI
		i
		aı i:
0xC90	<u>PMOVS</u>	FI
0xCA0	PMSWINC_EL0	FI
		is
0xCA0	PMZR_EL0	
		FI is
0xCC0	PMOVSSET_EL0	E1
		FI
		FI
0xCC0	PMOVSSET_EL0	FI
		FI i:
		i
0xCE0	PMCGCR0	
		FI

0xE00	<u>PMCFGR</u>	FI
0xE00	<u>PMCFGR</u>	FI
0xE04	PMCR_EL0	FI
0xE08	PMIIDR	FI
0xE10	PMCR_EL0	
	DIAGRADO	FI
0xE20	PMCEID0	FI
0xE24	PMCEID1	FI
0xE28	PMCEID2	FI
0xE2C	PMCEID3	FI
0xE30	PMSSCR_EL1	F
0xE40	PMMIR	FI i

0×E40	<u>PMMIR</u>	
		FI is I
0xF00	<u>PMITCTRL</u>	FI
0xFA8	<u>PMDEVAFF</u>	FI
0xFA8	PMDEVAFF0	FI
0×FAC	PMDEVAFF1	FI
0xFB0	PMLAR	FI
0xFB4	PMLSR	FI
0xFB8	<u>PMAUTHSTATUS</u>	
0xFBC	<u>PMDEVARCH</u>	
0xFC8	<u>PMDEVID</u>	FI
0xFCC	<u>PMDEVTYPE</u>	FI
0xFD0	PMPIDR4	

0xFE0	<u>PMPIDR0</u>
0xFE4	PMPIDR1
	<u> </u>
0xFE8	PMPIDR2
0xFEC	PMPIDR3
0xFF0	PMCIDR0
0xFF4	PMCIDR1
0xFF8	PMCIDR2
0xFFC	PMCIDR3

Direct accesses to other offsets in this block are res0.

AArch32AArch64AArch32AArch64Index byExternalRegistersRegistersInstructionsInstructionsEncodingRegisters

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

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