

## EDCIDR3, External Debug Component Identification Register 3

The EDCIDR3 characteristics are:

### Purpose

Provides information to identify an external debug component.

For more information, see 'About the Component Identification scheme'.

### Configuration

When FEAT\_DoPD is implemented, EDCIDR3 is in the Core power domain. Otherwise, EDCIDR3 is in the Debug power domain.

Implementation of this register is optional.

This register is required for CoreSight compliance.

### Attributes

EDCIDR3 is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																PRMBL 3															

#### Bits [31:8]

Reserved, res0.

#### PRMBL\_3, bits [7:0]

Preamble.

Reads as 0xB1.

Access to this field is **RO**.

# Accessing EDCIDR3

EDCIDR3 can be accessed through the external debug interface:

Component	Offset	Instance
Debug	0xFFC	EDCIDR3

This interface is accessible as follows:

- When FEAT\_DoPD is not implemented or IsCorePowered(), accesses to this register are **RO**.
- Otherwise, accesses to this register generate an error response.

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[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

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