PMCFGR, Performance Monitors Configuration Register

The PMCFGR characteristics are:

Purpose

Contains PMU-specific configuration data.

Configuration

This register is present only when FEAT_PMUv3_EXT is implemented. Otherwise, direct accesses to PMCFGR are res0.

PMCFGR is in the Core power domain.

Attributes

PMCFGR is a:

- 64-bit register when FEAT_PMUv3_EXT64 is implemented
- 32-bit register otherwise

This register is part of the PMU block.

Field descriptions

When FEAT_PMUv3_EXT64 is implemented:

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															
NCG				RES0							SS	FZO	RES0		UEN	WT	NA	EX	CCD	CC	SIZE								N			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:32]

Reserved, res0.

NCG, bits [31:28]
When FEAT_PMUv3_ICNTR is implemented:

Counter Groups. Defines the number of counter groups implemented, minus one.

Reads as `0b0001`.

Access to this field is **RO**.

Otherwise:

Defines the number of counter groups implemented, minus one.

This field reads-as-zero.

Reads as `0b0000`.

Access to this field is **RO**.

Bits [27:23]

Reserved, res0.

SS, bit [22]

Snapshot supported.

SS	Meaning
`0b0`	Snapshot mechanism not supported. The locations `0x600-0x7FC` and `0xE30-0xE3C` are implementation defined.
`0b1`	Snapshot mechanism supported. If FEAT_PMUv3_SS is implemented, then the following registers are implemented: • PMU.PMEVCNTSVR<n>_EL1. • PMU.PMCCNTSVR_EL1. • If FEAT_PMUv3_ICNTR is implemented, PMU.PMICNTSVR_EL1. • PMU.PMSSCR_EL1. Otherwise, locations `0x600-0x7FC` and `0xE30-0xE3C` contain implementation defined snapshot registers.

FEAT_PMUv3_SS implements the functionality identified by the value 1.

If FEAT_PMUv3_SS is not implemented, a PMU might include an implementation defined snapshot mechanism, including one using the implementation defined registers `0x600-0x7FC` and `0xE30-0xE3C`.

This field has an implementation defined value.

Access to this field is **RO**.

FZO, bit [21]

Freeze-on-overflow supported. Defined values are:

FZO	Meaning
`0b0`	Freeze-on-overflow mechanism is not supported. PMU.PMCR_EL0.FZO is res0.
`0b1`	Freeze-on-overflow mechanism is supported. PMU.PMCR_EL0.FZO is RW.

FEAT_PMUv3p7 implements the functionality added by the value `0b1`.

From Armv8.7, if FEAT_PMUv3 is implemented, the only permitted value is `0b1`.

Bit [20]

Reserved, res0.

UEN, bit [19]

User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RAZ.

Reads as `0b0`.

Access to this field is **RO**.

WT, bit [18]

This feature is not supported, so this bit is RAZ.

Reads as `0b0`.

Access to this field is **RO**.

NA, bit [17]

This feature is not supported, so this bit is RAZ.

Reads as `0b0`.

Access to this field is **RO**.

EX, bit [16]

Export supported. Value is implementation defined.

EX	Meaning
0b0	PMU.PMCR_EL0.X is res0.
0b1	PMU.PMCR_EL0.X is read/write.

This field has an implementation defined value.

Access to this field is **RO**.

CCD, bit [15]

Cycle counter has prescale.

This is res1 if AArch32 is supported, and RAZ otherwise.

CCD	Meaning
0b0	PMU.PMCR_EL0.D is res0.
0b1	PMU.PMCR_EL0.D is read/write.

CC, bit [14]

Dedicated cycle counter (counter 31) supported.

Reads as 0b1.

Access to this field is **RO**.

SIZE, bits [13:8]

Size of counters, minus one. This field defines the size of the largest counter implemented by the Performance Monitors Unit.

From Armv8, the largest counter is 64-bits, so the value of this field is 0b111111.

This field is used by software to determine the spacing of the counters in the memory-map. From Armv8, the counters are a doubleword-aligned addresses.

Reads as 0b111111.

Access to this field is **RO**.

N, bits [7:0]

Number of counters, minus one.

N	Meaning

0x00	Only PMU.PMCCNTR_EL0 implemented.
0x01..0x20	Number of counters implemented, 1 to 33.

All other values are reserved.

The count includes:

- The cycle counter, PMU.PMCCNTR_EL0.
- If FEAT_PMUv3_ICNTR is implemented, the Instruction Counter, PMU.PMICNTR_EL0.

For example, if PMCFGR.N == 0x07 then:

- There are eight counters in total.
- If FEAT_PMUv3_ICNTR is not implemented, this comprises 7 event counters and the cycle counter.
- If FEAT_PMUv3_ICNTR is implemented, this comprises 6 event counters, the cycle counter, and the instruction counter.

This field has an implementation defined value.

Access to this field is **RO**.

Otherwise:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCG				RES0					SS	FZO	RES0	UEN	WT	NA	EX	CCD	CC	SIZE				N									

NCG, bits [31:28]
When FEAT_PMUv3_ICNTR is implemented:

Counter Groups. Defines the number of counter groups implemented, minus one.

Reads as 0b0001.

Access to this field is **RO**.

Otherwise:

Defines the number of counter groups implemented, minus one.

This field reads-as-zero.

Reads as 0b0000.

Access to this field is **RO**.

Bits [27:23]

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0b0	Snapshot mechanism not supported. The locations 0x600-0x7FC and 0xE30-0xE3C are implementation defined.
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FEAT_PMUv3p7 implements the functionality added by the value 0b1.

From Armv8.7, if FEAT_PMUv3 is implemented, the only permitted value is 0b1.

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This feature is not supported, so this bit is RAZ.

Reads as 0b0.

Access to this field is **RO**.

NA, bit [17]

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Reads as 0b0.

Access to this field is **RO**.

EX, bit [16]

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Access to this field is **RO**.

CCD, bit [15]

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This field has an implementation defined value.

Access to this field is **RO**.

Accessing PMCFGR

Note

AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT64 is implemented

[63:0] Accessible at offset 0xE00 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

When FEAT_PMUv3_EXT32 is implemented

[31:0] Accessible at offset 0xE00 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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