AArch64
Instructions

Index by Encoding

External Registers

SPMEVCNTR<n>_EL0, System Performance Monitors Event Count Register, n = 0 - 63

The SPMEVCNTR<n> EL0 characteristics are:

Purpose

Event counter <n> in System PMU <s>, where n is 0 to 63.

Configuration

This register is present only when FEAT_SPMU is implemented. Otherwise, direct accesses to SPMEVCNTR<n> EL0 are undefined.

Attributes

SPMEVCNTR<n> EL0 is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

CNTR CNTR

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

CNTR, bits [63:0]

Event counter n.

The number of implemented bits for SPMEVCNTR<n>_EL0 is implementation defined. Unimplemented bits are res0.

The reset behavior of this field is:

• On a Warm reset, this field resets to an architecturally unknown value.

Accessing SPMEVCNTR<n>_EL0

To access SPMEVCNTR<n>_EL0 for System PMU <s>, set SPMSELR EL0.SYSPMUSEL to s and SPMSELR EL0.BANK to n[5:4].

SPMEVCNTR<n>_EL0 reads-as-zero and ignores writes if event counter <n> is not implemented by System PMU <s>.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, SPMEVCNTR<m>_EL0 ; Where m = 0-15

op0	op1	CRn	CRm	op2
0b10	0b011	0b1110	0b000:m[3]	m[2:0]

```
integer m = UInt(CRm<0>:op2<2:0>);
if PSTATE.EL == ELO then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR\_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nSPMEVCNTRn_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMEVCNTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR\_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nSPMEVCNTRn_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
```

```
SPMEVCNTR ELO[UInt(SPMSELR ELO.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] =
SPMEVCNTR_EL0 [UInt (SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m];
elsif PSTATE.EL == EL3 then
    X[t, 64] =
SPMEVCNTR ELO[UInt(SPMSELR ELO.SYSPMUSEL),
(UInt (SPMSELR ELO.BANK) * 16) + m];
```

MSR SPMEVCNTR<m>_EL0, <Xt>; Where m = 0-15

op0	op1	CRn	CRm	op2
0b10	0b011	0b1110	0b000:m[3]	m[2:0]

```
integer m = UInt(CRm<0>:op2<2:0>);
if PSTATE.EL == ELO then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<E2H, TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nSPMEVCNTRn_EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVCNTR_EL0 [UInt (SPMSELR_EL0.SYSPMUSEL),
(UInt (SPMSELR_ELO.BANK) * 16) + m] = X[t, 64];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
```

```
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2 EL2.nSPMEVCNTRn EL0 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED:
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVCNTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m] = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION DEFINED "EL3 trap priority
when SDD == '1'" && MDCR EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        SPMEVCNTR_EL0 [UInt (SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR_ELO.BANK) * 16) + m] = X[t, 64];
elsif PSTATE.EL == EL3 then
    SPMEVCNTR_EL0[UInt(SPMSELR_EL0.SYSPMUSEL),
(UInt(SPMSELR ELO.BANK) * 16) + m] = X[t, 64];
```

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