<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	Encoding

COSP

Clear Other Speculative Prediction Restriction by Context prevents predictions, other than Cache prefetch, Control flow, and Data Value predictions, that predict execution addresses based on information gathered from earlier execution within a particular execution context. Predictions, other than Cache prefetch, Control flow, and Data Value predictions, determined by the actions of code in the target execution context or contexts appearing in program order before the instruction cannot exploitatively control any speculative access occurring after the instruction is complete and synchronized.

This is an alias of **SYS**. This means:

- The encodings in this description are named to match the encodings of SYS.
- The description of <u>SYS</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

System (FEAT_SPECRES2)

COSP RCTX, <Xt>

is equivalent to

SYS #3, C7, C3, #6, <Xt>

and is always the preferred disassembly.

Assembler Symbols

< Xt >

Is the 64-bit name of the general-purpose source register, encoded in the "Rt" field.

Operation

The description of <u>SYS</u> gives the operational pseudocode for this instruction.

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 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no_diffs_2023_09_RC2,\ sve\ v2023-06_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$

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