

## AMPIDR2, Activity Monitors Peripheral Identification Register 2

The AMPIDR2 characteristics are:

### Purpose

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

### Configuration

It is implementation defined whether AMPIDR2 is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is optional.

This register is present only when FEAT\_AMUv1 is implemented.

### Attributes

AMPIDR2 is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																REVISION		JEDEC		DES 1											

#### Bits [31:8]

Reserved, res0.

#### REVISION, bits [7:4]

Part major revision. Parts can also use this field to extend Part number to 16-bits.

This field has an implementation defined value.

Access to this field is **RO**.

#### JEDEC, bit [3]

Indicates a JEP106 identity code is used.

Reads as 0b1.

Access to this field is **RO**.

### **DES\_1, bits [2:0]**

Designer, most significant bits of JEP106 ID code.

For Arm Limited, this field is 0b011.

This field has an implementation defined value.

Access to this field is **RO**.

## **Accessing AMPIDR2**

**AMPIDR2 can be accessed through the memory-mapped interfaces:**

<b>Component</b>	<b>Offset</b>	<b>Instance</b>
AMU	0xFE8	AMPIDR2

Accesses on this interface are **RO**.

---

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.