

## GICR\_SYNCR, Redistributor Synchronize Register

The GICR\_SYNCR characteristics are:

### Purpose

Indicates completion of register based invalidate operations.

### Configuration

A copy of this register is provided for each Redistributor.

### Attributes

GICR\_SYNCR is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																Busy															

#### Bits [31:1]

Reserved, res0.

#### Busy, bit [0]

Indicates completion of invalidation operations

Busy	Meaning
0b0	No operations are in progress.
0b1	A write is in progress to one or more of the following registers: <ul style="list-style-type: none"><li>• <a href="#">GICR_INVLPIR</a>.</li><li>• <a href="#">GICR_INVALLR</a>.</li><li>• GICv3, <a href="#">GICR_CLRLPIR</a>.</li></ul>

This field tracks operations initiated on the same Redistributor.

# Accessing GICR\_SYNCR

When this register is accessed, it is optional that an implementation might wait until all operations are complete before returning a value, in which case GICR\_SYNCR.Busy is always 0.

This register is mandatory when any of the following are true:

- [GICR\\_TYPER](#).Direct is 1.
- [GICR\\_CTLR](#).IR is 1.
- GICv4.1 is implemented.

Otherwise, the functionality is implementation defined.

**GICR\_SYNCR can be accessed through the memory-mapped interfaces:**

Component	Frame	Offset	Instance
GIC Redistributor	RD_base	0x00C0	GICR_SYNCR

Accesses on this interface are **RO**.

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.