# TRBCIDR0, Component Identification Register 0

The TRBCIDR0 characteristics are:

## Purpose

Provides discovery information about the component.

For additional information, see the CoreSight Architecture Specification.

## Configuration

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBCIDR0 are res0.

TRBCIDR0 is in the Core power domain.

## Attributes

TRBCIDR0 is a 32-bit register.

## Field descriptions

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | PRMBL_0 | | | | | | | |

**Bits [31:8]**

Reserved, res0.

**PRMBL_0, bits [7:0]**

Component identification preamble, segment 0.

Reads as `0x0D`.

Access to this field is **RO**.

## Accessing TRBCIDR0

**TRBCIDR0 can be accessed through the external debug interface:**

| Component | Offset | Instance |
|---|---|---|

| | | |
|---|---|---|
| TRBE | 0xFF0 | TRBCIDR0 |

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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