<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<b>Encoding</b>

Pseu

### **LDAXR**

Load-Acquire Exclusive Register derives an address from a base register value, loads a 32-bit word or 64-bit doubleword from memory, and writes it to a register. The memory access is atomic. The PE marks the physical address being accessed as an exclusive access. This exclusive access mark is checked by Store Exclusive instructions. See *Synchronization and semaphores*. The instruction also has memory ordering semantics as described in *Load-Acquire*, *Store-Release*. For information about memory accesses, see *Load/Store addressing modes*.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

1 x 0 0 1 0 0 0 0 1 0 (1)(1)(1)(1)(1)(1)(1)(1)(1)(1)(1)(1)

size

L

Rs

O

Rt

Rt
```

```
32-bit (size == 10)
```

```
LDAXR \langle Wt \rangle, [\langle Xn \mid SP \rangle \{, \#0\}]
```

## 64-bit (size == 11)

```
LDAXR <Xt>, [<Xn | SP>{, #0}]

integer n = UInt(Rn);
integer t = UInt(Rt);

constant integer elsize = 8 << UInt(size);
integer regsize = if elsize == 64 then 64 else 32;
boolean tagchecked = n != 31;</pre>
```

### **Assembler Symbols**

<Wt> Is the 32-bit name of the general-purpose register to be

transferred, encoded in the "Rt" field.

<Xt> Is the 64-bit name of the general-purpose register to be

transferred, encoded in the "Rt" field.

<Xn|SP> Is the 64-bit name of the general-purpose base register or

stack pointer, encoded in the "Rn" field.

#### Operation

```
bits(64) address;
bits(elsize) data;
constant integer dbytes = elsize DIV 8;

AccessDescriptor accdesc = CreateAccDescExLDST(MemOp LOAD, TRUE, tagche
if n == 31 then
```

```
CheckSPAlignment();
  address = SP[];
else
  address = X[n, 64];

// Tell the Exclusives monitors to record a sequence of one or more ato
  // memory reads from virtual address range [address, address+dbytes-1].
  // The Exclusives monitor will only be set if all the reads are from th
  // same dbytes-aligned physical address, to allow for the possibility of
  // an atomicity break if the translation is changed between reads.
  AArch64.SetExclusiveMonitors(address, dbytes);

data = Mem[address, dbytes, accdesc];
  X[t, regsize] = ZeroExtend(data, regsize);
```

# **Operational information**

If PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored.

BaseSIMD&FPSVESMEIndex byInstructionsInstructionsInstructionsInstructionsEncoding

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel; Build timestamp: 2023-09-18T17:56

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