External

Registers

# **CNTHVS CVAL EL2, Counter-timer Secure** Virtual Timer CompareValue register (EL2)

The CNTHVS CVAL EL2 characteristics are:

### **Purpose**

Holds the compare value for the Secure EL2 virtual timer.

### Configuration

AArch64 System register CNTHVS CVAL EL2 bits [63:0] are architecturally mapped to AArch32 System register CNTHVS CVAL[63:0].

This register is present only when FEAT SEL2 is implemented and FEAT VHE is implemented. Otherwise, direct accesses to CNTHVS CVAL EL2 are undefined.

#### **Attributes**

CNTHVS CVAL EL2 is a 64-bit register.

### Field descriptions

03 02 01 00 39 38 37 30 33 34 33 32 31 30 49 48 47 40 43 44 43 42 41 40 39 38 37 30 33 34 33 3
CompareValue
CompareValue

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

#### CompareValue, bits [63:0]

Holds the Secure EL2 virtual timer CompareValue.

When CNTHVS CTL EL2. ENABLE is 1, the timer condition is met when (CNTVCT ELO - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHVS CTL EL2.ISTATUS is set to 1.
- If <u>CNTHVS CTL EL2</u>.IMASK is 0, an interrupt is generated.

When <u>CNTHVS CTL EL2</u>.ENABLE is 0, the timer condition is not met, but CNTVCT ELO continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are res0.

The value of this field is treated as zero-extended in all counter calculations.

The reset behavior of this field is:

• On a Warm reset, this field resets to an architecturally unknown value.

### Accessing CNTHVS\_CVAL\_EL2

Accesses to this register use the following encodings in the System register encoding space:

# MRS <Xt>, CNTHVS\_CVAL\_EL2

op0	op1	CRn	CRm	op2
0b11	0b100	0b1110	0b0100	0b010

```
if PSTATE.EL == ELO then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
    if !IsCurrentSecurityState(SS Secure) then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if !IsCurrentSecurityState(SS_Secure) then
        UNDEFINED;
    else
        X[t, 64] = CNTHVS_CVAL_EL2;
elsif PSTATE.EL == EL3 then
    if SCR EL3.EEL2 == '0' then
        UNDEFINED;
    else
        X[t, 64] = CNTHVS_CVAL_EL2;
```

### MSR CNTHVS\_CVAL\_EL2, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b100	0b1110	0b0100	0b010

```
if PSTATE.EL == ELO then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if !IsCurrentSecurityState(SS_Secure) then
        UNDEFINED;
    elsif EL2Enabled() && HCR EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if !IsCurrentSecurityState(SS_Secure) then
        UNDEFINED;
        CNTHVS\_CVAL\_EL2 = X[t, 64];
elsif PSTATE.EL == EL3 then
    if SCR_EL3.EEL2 == '0' then
        UNDEFINED;
    else
        CNTHVS CVAL EL2 = X[t, 64];
```

## MRS <Xt>, CNTV\_CVAL\_EL0

op0	op1	CRn	CRm	op2
0b11	0b011	0b1110	0b0011	0b010

```
if PSTATE.EL == ELO then
    if !(EL2Enabled() && HCR_EL2.<E2H, TGE> == '11')
&& CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11'
&& CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11'
&& SCR EL3.NS == '0' &&
IsFeatureImplemented(FEAT_SEL2) then
        X[t, 64] = CNTHVS_CVAL_EL2;
    elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11'
&& SCR\_EL3.NS == '1' then
        X[t, 64] = CNTHV_CVAL_EL2;
    else
        X[t, 64] = CNTV_CVAL_ELO;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
```

```
X[t, 64] = NVMem[0x168];
else
          X[t, 64] = CNTV_CVAL_ELO;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
IsFeatureImplemented(FEAT_SEL2) then
          X[t, 64] = CNTHVS_CVAL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1'
then
          X[t, 64] = CNTHV_CVAL_EL2;
else
          X[t, 64] = CNTV_CVAL_EL0;
elsif PSTATE.EL == EL3 then
          X[t, 64] = CNTV_CVAL_EL0;
```

### MSR CNTV CVAL EL0, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b011	0b1110	0b0011	0b010

```
if PSTATE.EL == ELO then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11')
&& CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11'
&& CNTHCTL_EL2.ELOVTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11'
&& CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11'
&& SCR_EL3.NS == '0' &&
IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS\_CVAL\_EL2 = X[t, 64];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11'
&& SCR\_EL3.NS == '1' then
        CNTHV_CVAL_EL2 = X[t, 64];
        CNTV\_CVAL\_EL0 = X[t, 64];
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        NVMem[0x168] = X[t, 64];
    else
        CNTV_CVAL_ELO = X[t, 64];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
IsFeatureImplemented(FEAT_SEL2) then
```

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