ERR<n>MISC0, Error Record <n> Miscellaneous Register 0, n = 0 - 65534

The ERR<n>MISC0 characteristics are:

Purpose

implementation defined error syndrome register. The miscellaneous syndrome registers might contain:

- Information to locate where the error was detected.
- If the error was detected within a FRU, the identity of the FRU.
- A Corrected error counter or counters.
- Other state information not present in the corresponding status and address registers.

If the node that owns error record <n> implements a standard format Corrected error counter or counters (ERR<q>FR.CEC != `0b000`), then it is implementation defined whether error record <n> can record countable errors, and:

- If error record <n> records countable errors, then ERR<n>MISC0 implements the standard format Corrected error counter or counters for error record <n>.
- If error record <n> does not record countable errors, then it is recommended that the fields in ERR<n>MISC0 defined for the standard format counter or counters are res0. That is, the fields behave like counters that never count.

Configuration

This register is present only when error record <n> is implemented. Otherwise, direct accesses to ERR<n>MISC0 are res0.

ERR<q>FR describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record then q = n.

For implementation defined fields in ERR<n>MISC0, writing zero returns the error record to an initial quiescent state.

In particular, if any implementation defined syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, nonzero, and ignore writes are compliant with this requirement.

Note

Arm recommends that any implementation defined syndrome field that can generate a Fault Handling, Error Recovery, Critical, or implementation defined, interrupt request is disabled at Cold reset and is enabled by software writing an implementation defined nonzero value to an implementation defined field in ERR<q>CTLR.

Attributes

ERR<n>MISC0 is a 64-bit register.

Field descriptions

When ERR<q>FR.CEC == 0b000 or error record <n> does not record countable errors:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
IMPLEMENTATION DEFINED
IMPLEMENTATION DEFINED
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

IMPLEMENTATION DEFINED, bits [63:0]

implementation defined syndrome.

When ERR<q>FR.CEC == 0b100, ERR<q>FR.RP == 0 and error record <n> records countable errors:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48	47	46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
IMPLEMENTATION DEFINED	OF	CEC
IMPLEMENTATION DEFINED		
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

IMPLEMENTATION DEFINED, bits [63:48]

implementation defined syndrome.

OF, bit [47]

Sticky overflow bit. Set to 1 when ERR<n>MISC0.CEC is incremented and wraps through zero.

OF	Meaning
0b0	Counter has not overflowed.

0b1	Counter has overflowed.

A direct write that modifies this field might indirectly set ERR<n>STATUS.OF to an unknown value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this field to an unknown value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CEC, bits [46:32]

Corrected error count. Incremented for each Corrected error. It is implementation defined and might be unpredictable whether Deferred and Uncorrected errors are counted.

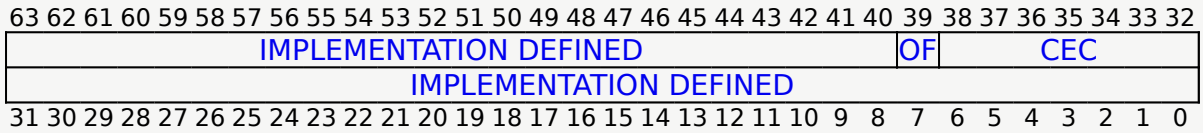
The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

IMPLEMENTATION DEFINED, bits [31:0]

implementation defined syndrome.

When ERR<q>FR.CEC == 0b010, ERR<q>FR.RP == 0 and error record <n> records countable errors:



IMPLEMENTATION DEFINED, bits [63:40]

implementation defined syndrome.

OF, bit [39]

Sticky overflow bit. Set to 1 when ERR<n>MISC0.CEC is incremented and wraps through zero.

OF	Meaning
0b0	Counter has not overflowed.
0b1	Counter has overflowed.

A direct write that modifies this field might indirectly set ERR<n>STATUS.OF to an unknown value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this field to an unknown value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CEC, bits [38:32]

Corrected error count. Incremented for each Corrected error. It is implementation defined and might be unpredictable whether Deferred and Uncorrected errors are counted.

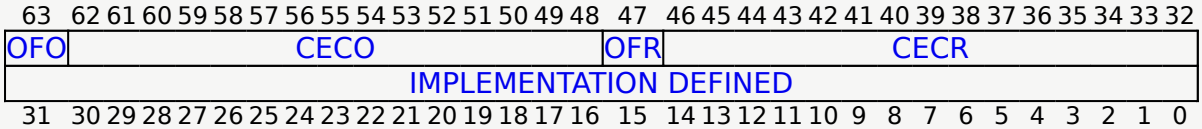
The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

IMPLEMENTATION DEFINED, bits [31:0]

implementation defined syndrome.

When ERR<q>FR.CEC == 0b100, ERR<q>FR.RP == 1 and error record <n> records countable errors:



OFO, bit [63]

Sticky overflow bit, other. Set to 1 when ERR<n>MISC0.CECO is incremented and wraps through zero.

OFO	Meaning
0b0	Other counter has not overflowed.
0b1	Other counter has overflowed.

A direct write that modifies this field might indirectly set ERR<n>STATUS.OF to an unknown value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this field to an unknown value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CECO, bits [62:48]

Corrected error count, other. Incremented for each countable error that is not accounted for by incrementing ERR<n>MISC0.CECR.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

OFR, bit [47]

Sticky overflow bit, repeat. Set to 1 when ERR<n>MISC0.CECR is incremented and wraps through zero.

OFR	Meaning
0b0	Repeat counter has not overflowed.
0b1	Repeat counter has overflowed.

A direct write that modifies this field might indirectly set ERR<n>STATUS.OF to an unknown value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this field to an unknown value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CECR, bits [46:32]

Corrected error count, repeat. Incremented for the first countable error, which also records other syndrome for the error, and subsequently for each countable error that matches the recorded other syndrome. Corrected errors are countable errors. It is implementation defined and might be unpredictable whether Deferred and Uncorrected errors are countable errors.

Note

For example, the other syndrome might include the set and way information for an error detected in a cache. This might be recorded in the implementation defined ERR<n>MISC<m> fields on a first Corrected error. ERR<n>MISC0.CECR is then incremented for each subsequent Corrected Error in the same set and way.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

IMPLEMENTATION DEFINED, bits [31:0]

implementation defined syndrome.

When ERR<q>FR.CEC == 0b010, ERR<q>FR.RP == 1 and error record <n> records countable errors:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48	47	46 45 44 43 42 41 40	39	38 37 36 35 34 33 32
IMPLEMENTATION DEFINED	OFO	CECO	OFR	CECR
IMPLEMENTATION DEFINED				
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9 8	7	6 5 4 3 2 1 0

IMPLEMENTATION DEFINED, bits [63:48]

implementation defined syndrome.

OFO, bit [47]

Sticky overflow bit, other. Set to 1 when ERR<n>MISC0.CECO is incremented and wraps through zero.

OFO	Meaning
0b0	Other counter has not overflowed.
0b1	Other counter has overflowed.

A direct write that modifies this field might indirectly set ERR<n>STATUS.OF to an unknown value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this field to an unknown value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CECO, bits [46:40]

Corrected error count, other. Incremented for each countable error that is not accounted for by incrementing ERR<n>MISC0.CECR.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

OFR, bit [39]

Sticky overflow bit, repeat. Set to 1 when ERR<n>MISC0.CECR is incremented and wraps through zero.

OFR	Meaning

0b0	Repeat counter has not overflowed.
0b1	Repeat counter has overflowed.

A direct write that modifies this field might indirectly set ERR<n>STATUS.OF to an unknown value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this field to an unknown value.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

CECR, bits [38:32]

Corrected error count, repeat. Incremented for the first countable error, which also records other syndrome for the error, and subsequently for each countable error that matches the recorded other syndrome. Corrected errors are countable errors. It is implementation defined and might be unpredictable whether Deferred and Uncorrected errors are countable errors.

Note

For example, the other syndrome might include the set and way information for an error detected in a cache. This might be recorded in the implementation defined ERR<n>MISC<m> fields on a first Corrected error. ERR<n>MISC0.CECR is then incremented for each subsequent Corrected Error in the same set and way.

The reset behavior of this field is:

- On a Cold reset, this field resets to an architecturally unknown value.

IMPLEMENTATION DEFINED, bits [31:0]

implementation defined syndrome.

Accessing ERR<n>MISC0

Reads from ERR<n>MISC0 return an implementation defined value and writes have implementation defined behavior.

If the Common Fault Injection Mechanism is implemented by the node that owns this error record, and ERR<q>PFGF.MV is 1, then some parts of this register are read/write when ERR<n>STATUS.MV is 0. See ERR<n>PFGF.MV for more information.

For other parts of this register, or if the Common Fault Injection Mechanism is not implemented, then Arm recommends that:

- Miscellaneous syndrome for multiple errors, such as a corrected error counter, is read/write.
- When ERR<n>STATUS.MV is 1, the miscellaneous syndrome specific to the most recently recorded error ignores writes.

Note

These recommendations allow a counter to be reset in the presence of a persistent error, while preventing specific information, such as that identifying a FRU, from being lost if an error is detected while the previous error is being logged.

ERR<n>MISC0 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
RAS	`0x020` + (64 * n)	ERR<n>MISC0

Accesses on this interface are **RW**.

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