MOV (scalar)

Move vector element to scalar. This instruction duplicates the specified vector element in the SIMD&FP source register into a scalar, and writes the result to the SIMD&FP destination register.

Depending on the settings in the *CPACR_EL1*, *CPTR_EL2*, and *CPTR_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

This is an alias of [DUP (element)](). This means:

- The encodings in this description are named to match the encodings of [DUP (element)]().
- The description of [DUP (element)]() gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

31 30	29	28 27 26 25 24 23 22 21	20 19 18 17 16	15	14 13 12 11	10	9 8 7 6 5	4 3 2 1 0
0 1	0	1 1 1 1 0 0 0 0	imm5	0	0 0 0 0	1	Rn	Rd

```
MOV <V><d>, <Vn>.<T>[<index>]
```

is equivalent to

```
DUP <V><d>, <Vn>.<T>[<index>]
```

and is always the preferred disassembly.

Assembler Symbols

\<V\>

Is the destination width specifier, encoded in "imm5":

imm5	\<V\>
x0000	RESERVED
xxxx1	B
xxx10	H
xx100	S
x1000	D

\<d\>

Is the number of the SIMD&FP destination register, encoded in the "Rd" field.

\<Vn\>

Is the name of the SIMD&FP source register, encoded in the "Rn" field.

<T>

Is the element width specifier, encoded in "imm5":

imm5	<T>
x0000	RESERVED
xxxx1	B
xxx10	H
xx100	S
x1000	D

<index>

Is the element index encoded in "imm5":

imm5	<index>
x0000	RESERVED
xxxx1	imm5<4:1>
xxx10	imm5<4:2>
xx100	imm5<4:3>
x1000	imm5<4>

Operation

The description of [DUP (element)](#) gives the operational pseudocode for this instruction.

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.