

SHA1SU0

SHA1 schedule update 0.

Advanced SIMD (FEAT_SHA1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0	0	0	0				Rm		0	0	1	1	0	0				Rn				Rd		

SHA1SU0 **<Vd>.4S, <Vn>.4S, <Vm>.4S**

```
integer d = UInt(Rd);
integer n = UInt(Rn);
integer m = UInt(Rm);
if !IsFeatureImplemented(FEAT_SHA1) then UNDEFINED;
```

Assembler Symbols

- <Vd>** Is the name of the SIMD&FP source and destination register, encoded in the "Rd" field.
- <Vn>** Is the name of the second SIMD&FP source register, encoded in the "Rn" field.
- <Vm>** Is the name of the third SIMD&FP source register, encoded in the "Rm" field.

Operation

```
AArch64.CheckFPAdvSIMDEnabled();

bits(128) operand1 = V[d, 128];
bits(128) operand2 = V[n, 128];
bits(128) operand3 = V[m, 128];
bits(128) result;

result = operand2<63:0>:operand1<127:64>;
result = result EOR operand1 EOR operand3;
V[d, 128] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.

- The values of the NZCV flags.

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