

## TRCVMIDCVR<n>, Virtual Context Identifier Comparator Value Register <n>, n = 0 - 7

The TRCVMIDCVR<n> characteristics are:

### Purpose

Contains the Virtual Context Identifier Comparator value.

### Configuration

External register TRCVMIDCVR<n> bits [63:0] are architecturally mapped to AArch64 System register [TRCVMIDCVR<n>\[63:0\]](#).

This register is present only when FEAT\_ETE is implemented, FEAT\_TRC\_EXT is implemented and  $\text{UInt}(\text{TRCIDR4.NUMVMIDC}) > n$ . Otherwise, direct accesses to TRCVMIDCVR<n> are res0.

### Attributes

TRCVMIDCVR<n> is a 64-bit register.

### Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32						
																VALUE																					
																VALUE																					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						

#### VALUE, bits [63:0]

Virtual context identifier value. The width of this field is indicated by [TRCIDR2.VMIDSIZE](#). Unimplemented bits are res0. After a PE Reset, the trace unit assumes that the Virtual context identifier is zero until the PE updates the Virtual context identifier .

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

## Accessing TRCVMIDCVR<n>

Must be programmed if any of the following are true:

- [TRCRSCTLR<a>](#).GROUP == 0b0111 and [TRCRSCTLR<a>](#).VMID[n] == 1.
- [TRCACATR<a>](#).CONTEXTTYPE == 0b10 or 0b11 and [TRCACATR<a>](#).CONTEXT == n.

**TRCVMIDCVR<n> can be accessed through the external debug interface:**

Component	Offset	Instance
ETE	0x640 + (8 * n)	TRCVMIDCVR<n>

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

---

[AArch32  
Registers](#)

[AArch64  
Registers](#)

[AArch32  
Instructions](#)

[AArch64  
Instructions](#)

[Index by  
Encoding](#)

[External  
Registers](#)

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94

Copyright Â© 2010-2023 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.