

SMADDL

Signed Multiply-Add Long multiplies two 32-bit register values, adds a 64-bit register value, and writes the result to the 64-bit destination register. This instruction is used by the alias [SMULL](#).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	1	1	0	0	1	Rm				0	Ra				Rn				Rd							
U								o0																							

SMADDL [<Xd>](#), [<Wn>](#), [<Wm>](#), [<Xa>](#)

```
integer d = UInt (Rd) ;
integer n = UInt (Rn) ;
integer m = UInt (Rm) ;
integer a = UInt (Ra) ;
```

Assembler Symbols

- [<Xd>](#) Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.
- [<Wn>](#) Is the 32-bit name of the first general-purpose source register holding the multiplicand, encoded in the "Rn" field.
- [<Wm>](#) Is the 32-bit name of the second general-purpose source register holding the multiplier, encoded in the "Rm" field.
- [<Xa>](#) Is the 64-bit name of the third general-purpose source register holding the addend, encoded in the "Ra" field.

Alias Conditions

Alias	Is preferred when
SMULL	Ra == '11111'

Operation

```
bits(32) operand1 = X[n, 32];
bits(32) operand2 = X[m, 32];
bits(64) operand3 = X[a, 64];

integer result;

result = Int(operand3, FALSE) + (Int(operand1, FALSE) * Int(operand2, F
X[d, 64] = result<63:0>;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

Base Instructions	SIMD&FP Instructions	SVE Instructions	SME Instructions	Index by Encoding
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[Sh](#)
[Pseu](#)

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56

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