External registers

AMCFGR: Activity Monitors Configuration Register

AMCGCR: Activity Monitors Counter Group Configuration Register

AMCIDR0: Activity Monitors Component Identification Register 0

AMCIDR1: Activity Monitors Component Identification Register 1

AMCIDR2: Activity Monitors Component Identification Register 2

AMCIDR3: Activity Monitors Component Identification Register 3

AMCNTENCLR0: Activity Monitors Count Enable Clear Register 0

AMCNTENCLR1: Activity Monitors Count Enable Clear Register 1

AMCNTENSET0: Activity Monitors Count Enable Set Register 0

AMCNTENSET1: Activity Monitors Count Enable Set Register 1

AMCR: Activity Monitors Control Register

AMDEVAFF0: Activity Monitors Device Affinity Register 0

AMDEVAFF1: Activity Monitors Device Affinity Register 1

AMDEVARCH: Activity Monitors Device Architecture Register

AMDEVTYPE: Activity Monitors Device Type Register

AMEVCNTR0<n>: Activity Monitors Event Counter Registers 0

AMEVCNTR1<n>: Activity Monitors Event Counter Registers 1

AMEVTYPER0<n>: Activity Monitors Event Type Registers 0

AMEVTYPER1<n>: Activity Monitors Event Type Registers 1

AMIIDR: Activity Monitors Implementation Identification Register

AMPIDR0: Activity Monitors Peripheral Identification Register 0

AMPIDR1: Activity Monitors Peripheral Identification Register 1

AMPIDR2: Activity Monitors Peripheral Identification Register 2

AMPIDR3: Activity Monitors Peripheral Identification Register 3

AMPIDR4: Activity Monitors Peripheral Identification Register 4

ASICCTL: CTI External Multiplexer Control register

CNTACR<n>: Counter-timer Access Control Registers

CNTCR: Counter Control Register

CNTCV: Counter Count Value register

CNTEL0ACR: Counter-timer EL0 Access Control Register

CNTFID0: Counter Frequency ID

CNTFID<n>: Counter Frequency IDs, n > 0

CNTFRQ: Counter-timer Frequency

CNTID: Counter Identification Register

CNTNSAR: Counter-timer Non-secure Access Register

CNTPCT: Counter-timer Physical Count

CNTP_CTL: Counter-timer Physical Timer Control

CNTP_CVAL: Counter-timer Physical Timer CompareValue

CNTP_TVAL: Counter-timer Physical Timer TimerValue

CNTSCR: Counter Scale Register

CNTSR: Counter Status Register

CNTTIDR: Counter-timer Timer ID Register

CNTVCT: Counter-timer Virtual Count

CNTVOFF: Counter-timer Virtual Offset

CNTVOFF<n>: Counter-timer Virtual Offsets

CNTV_CTL: Counter-timer Virtual Timer Control

CNTV_CVAL: Counter-timer Virtual Timer CompareValue

CNTV_TVAL: Counter-timer Virtual Timer TimerValue

CounterID<n>: Counter ID registers

CTIAPPCLEAR: CTI Application Trigger Clear register

CTIAPPPULSE: CTI Application Pulse register

CTIAPPSET: CTI Application Trigger Set register

CTIAUTHSTATUS: CTI Authentication Status register

CTICHINSTATUS: CTI Channel In Status register

CTICHOUTSTATUS: CTI Channel Out Status register

CTICIDR0: CTI Component Identification Register 0

CTICIDR1: CTI Component Identification Register 1

CTICIDR2: CTI Component Identification Register 2

CTICIDR3: CTI Component Identification Register 3

CTICLAIMCLR: CTI CLAIM Tag Clear register

CTICLAIMSET: CTI CLAIM Tag Set register

CTICONTROL: CTI Control register

CTIDEVAFF0: CTI Device Affinity register 0

CTIDEVAFF1: CTI Device Affinity register 1

CTIDEVARCH: CTI Device Architecture register

CTIDEVCTL: CTI Device Control register

CTIDEVID: CTI Device ID register 0

CTIDEVID1: CTI Device ID register 1

CTIDEVID2: CTI Device ID register 2

CTIDEVTYPE: CTI Device Type register

CTIGATE: CTI Channel Gate Enable register

CTIINEN<n>: CTI Input Trigger to Output Channel Enable registers

CTIINTACK: CTI Output Trigger Acknowledge register

CTIITCTRL: CTI Integration mode Control register

CTILAR: CTI Lock Access Register

CTILSR: CTI Lock Status Register

CTIOUTEN<n>: CTI Input Channel to Output Trigger Enable registers

CTIPIDR0: CTI Peripheral Identification Register 0

CTIPIDR1: CTI Peripheral Identification Register 1

CTIPIDR2: CTI Peripheral Identification Register 2

CTIPIDR3: CTI Peripheral Identification Register 3

CTIPIDR4: CTI Peripheral Identification Register 4

CTITRIGINSTATUS: CTI Trigger In Status register

CTITRIGOUTSTATUS: CTI Trigger Out Status register

DBGAUTHSTATUS_EL1: Debug Authentication Status Register

DBGBCR<n>_EL1: Debug Breakpoint Control Registers

DBGBVR<n>_EL1: Debug Breakpoint Value Registers

DBGCLAIMCLR_EL1: Debug CLAIM Tag Clear Register

DBGCLAIMSET_EL1: Debug CLAIM Tag Set Register

DBGDTRRX_EL0: Debug Data Transfer Register, Receive

DBGDTRTX_EL0: Debug Data Transfer Register, Transmit

DBGWCR<n>_EL1: Debug Watchpoint Control Registers

DBGWVR<n>_EL1: Debug Watchpoint Value Registers

EDAA32PFR: External Debug Auxiliary Processor Feature Register

EDACR: External Debug Auxiliary Control Register

EDCIDR0: External Debug Component Identification Register 0

EDCIDR1: External Debug Component Identification Register 1

EDCIDR2: External Debug Component Identification Register 2

EDCIDR3: External Debug Component Identification Register 3

EDCIDSR: External Debug Context ID Sample Register

EDDEVAFF0: External Debug Device Affinity register 0

EDDEVAFF1: External Debug Device Affinity register 1

EDDEVARCH: External Debug Device Architecture register

EDDEVID: External Debug Device ID register 0

EDDEVID1: External Debug Device ID register 1

EDDEVID2: External Debug Device ID register 2

EDDEVTYPE: External Debug Device Type register

EDDFR: External Debug Feature Register

EDDFR1: External Debug Feature Register 1

EDECCR: External Debug Exception Catch Control Register

EDECR: External Debug Execution Control Register

EDESR: External Debug Event Status Register

EDHSR: External Debug Halting Syndrome Register

EDITCTRL: External Debug Integration mode Control register

EDITR: External Debug Instruction Transfer Register

EDLAR: External Debug Lock Access Register

EDLSR: External Debug Lock Status Register

EDPCSR: External Debug Program Counter Sample Register

EDPFR: External Debug Processor Feature Register

EDPIDR0: External Debug Peripheral Identification Register 0

EDPIDR1: External Debug Peripheral Identification Register 1

EDPIDR2: External Debug Peripheral Identification Register 2

EDPIDR3: External Debug Peripheral Identification Register 3

EDPIDR4: External Debug Peripheral Identification Register 4

EDPRCR: External Debug Power/Reset Control Register

EDPRSR: External Debug Processor Status Register

EDRCR: External Debug Reserve Control Register

EDSCR: External Debug Status and Control Register

EDSCR2: External Debug Status and Control Register 2

EDVIDSR: External Debug Virtual Context Sample Register

EDWAR: External Debug Watchpoint Address Register

ERR<n>ADDR: Error Record <n> Address Register

ERR<n>CTLR: Error Record <n> Control Register

ERR<n>FR: Error Record <n> Feature Register

ERR<n>MISC0: Error Record <n> Miscellaneous Register 0

ERR<n>MISC1: Error Record <n> Miscellaneous Register 1

ERR<n>MISC2: Error Record <n> Miscellaneous Register 2

ERR<n>MISC3: Error Record <n> Miscellaneous Register 3

ERR<n>PFGCDN: Error Record <n> Pseudo-fault Generation Countdown Register

ERR<n>PFGCTL: Error Record <n> Pseudo-fault Generation Control Register

ERR<n>PFGF: Error Record <n> Pseudo-fault Generation Feature Register

ERR<n>STATUS: Error Record <n> Primary Status Register

ERRACR: Access Configuration Register

ERRCIDR0: Component Identification Register 0

ERRCIDR1: Component Identification Register 1

ERRCIDR2: Component Identification Register 2

ERRCIDR3: Component Identification Register 3

ERRCRICR0: Critical Error Interrupt Configuration Register 0

ERRCRICR1: Critical Error Interrupt Configuration Register 1

ERRCRICR2: Critical Error Interrupt Configuration Register 2

ERRDEVAFF: Device Affinity Register

ERRDEVARCH: Device Architecture Register

ERRDEVID: Device Configuration Register

ERRERICR0: Error Recovery Interrupt Configuration Register 0

ERRERICR1: Error Recovery Interrupt Configuration Register 1

ERRERICR2: Error Recovery Interrupt Configuration Register 2

ERRFHICR0: Fault Handling Interrupt Configuration Register 0

ERRFHICR1: Fault Handling Interrupt Configuration Register 1

ERRFHICR2: Fault Handling Interrupt Configuration Register 2

ERRGSR: Error Group Status Register

ERRIIDR: Implementation Identification Register

ERRIMPDEF<n>: IMPLEMENTATION DEFINED Register <n>

ERRIRQCR<n>: Generic Error Interrupt Configuration Register <n>

ERRIRQSR: Error Interrupt Status Register

ERRPIDR0: Peripheral Identification Register 0

ERRPIDR1: Peripheral Identification Register 1

ERRPIDR2: Peripheral Identification Register 2

ERRPIDR3: Peripheral Identification Register 3

ERRPIDR4: Peripheral Identification Register 4

GICC_ABPR: CPU Interface Aliased Binary Point Register

GICC_AEOIR: CPU Interface Aliased End Of Interrupt Register

GICC_AHPPIR: CPU Interface Aliased Highest Priority Pending Interrupt Register

GICC_AIAR: CPU Interface Aliased Interrupt Acknowledge Register

GICC_APR<n>: CPU Interface Active Priorities Registers

GICC_BPR: CPU Interface Binary Point Register

GICC_CTLR: CPU Interface Control Register

GICC_DIR: CPU Interface Deactivate Interrupt Register

GICC_EOIR: CPU Interface End Of Interrupt Register

GICC_HPPIR: CPU Interface Highest Priority Pending Interrupt Register

GICC_IAR: CPU Interface Interrupt Acknowledge Register

GICC_IIDR: CPU Interface Identification Register

GICC_NSAPR<n>: CPU Interface Non-secure Active Priorities Registers

GICC_PMR: CPU Interface Priority Mask Register

GICC_RPR: CPU Interface Running Priority Register

GICC_STATUSR: CPU Interface Status Register

GICD_CLRSPI_NSR: Clear Non-secure SPI Pending Register

GICD_CLRSPI_SR: Clear Secure SPI Pending Register

GICD_CPENDSGIR<n>: SGI Clear-Pending Registers

GICD_CTLR: Distributor Control Register

GICD_ICACTIVER<n>: Interrupt Clear-Active Registers

GICD_ICACTIVER<n>E: Interrupt Clear-Active Registers (extended SPI range)

GICD_ICENABLER<n>: Interrupt Clear-Enable Registers

GICD_ICENABLER<n>E: Interrupt Clear-Enable Registers

GICD_ICFGR<n>: Interrupt Configuration Registers

GICD_ICFGR<n>E: Interrupt Configuration Registers (Extended SPI Range)

GICD_ICPENDR<n>: Interrupt Clear-Pending Registers

GICD_ICPENDR<n>E: Interrupt Clear-Pending Registers (extended SPI range)

GICD_IGROUPR<n>: Interrupt Group Registers

GICD_IGROUPR<n>E: Interrupt Group Registers (extended SPI range)

GICD_IGRPMODR<n>: Interrupt Group Modifier Registers

GICD_IGRPMODR<n>E: Interrupt Group Modifier Registers (extended SPI range)

GICD_IIDR: Distributor Implementer Identification Register

GICD_INMIR<n>: Non-maskable Interrupt Registers, x = 0 to 31

GICD_INMIR<n>E: Non-maskable Interrupt Registers for Extended SPIs, x = 0 to 31

GICD_IPRIORITYR<n>: Interrupt Priority Registers

GICD_IPRIORITYR<n>E: Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC.

GICD_IROUTER<n>: Interrupt Routing Registers

GICD_IROUTER<n>E: Interrupt Routing Registers (Extended SPI Range)

GICD_ISACTIVER<n>: Interrupt Set-Active Registers

GICD_ISACTIVER<n>E: Interrupt Set-Active Registers (extended SPI range)

GICD_ISENABLER<n>: Interrupt Set-Enable Registers

GICD_ISENABLER<n>E: Interrupt Set-Enable Registers

GICD_ISPENDR<n>: Interrupt Set-Pending Registers

GICD_ISPENDR<n>E: Interrupt Set-Pending Registers (extended SPI range)

GICD_ITARGETSR<n>: Interrupt Processor Targets Registers

GICD_NSACR<n>: Non-secure Access Control Registers

GICD_NSACR<n>E: Non-secure Access Control Registers

GICD_SETSPI_NSR: Set Non-secure SPI Pending Register

GICD_SETSPI_SR: Set Secure SPI Pending Register

GICD_SGIR: Software Generated Interrupt Register

GICD_SPENDSGIR<n>: SGI Set-Pending Registers

GICD_STATUSR: Error Reporting Status Register

GICD_TYPER: Interrupt Controller Type Register

GICD_TYPER2: Interrupt Controller Type Register 2

GICH_APR<n>: Active Priorities Registers

GICH_EISR: End Interrupt Status Register

GICH_ELRSR: Empty List Register Status Register

GICH_HCR: Hypervisor Control Register

GICH_LR<n>: List Registers

GICH_MISR: Maintenance Interrupt Status Register

GICH_VMCR: Virtual Machine Control Register

GICH_VTR: Virtual Type Register

GICM_CLRSPI_NSR: Clear Non-secure SPI Pending Register

GICM_CLRSPI_SR: Clear Secure SPI Pending Register

GICM_IIDR: Distributor Implementer Identification Register

GICM_SETSPI_NSR: Set Non-secure SPI Pending Register

GICM_SETSPI_SR: Set Secure SPI Pending Register

GICM_TYPER: Distributor MSI Type Register

GICR_CLRLPIR: Clear LPI Pending Register

GICR_CTLR: Redistributor Control Register

GICR_ICACTIVER0: Interrupt Clear-Active Register 0

GICR_ICACTIVER<n>E: Interrupt Clear-Active Registers

GICR_ICENABLER0: Interrupt Clear-Enable Register 0

GICR_ICENABLER<n>E: Interrupt Clear-Enable Registers

GICR_ICFGR0: Interrupt Configuration Register 0

GICR_ICFGR1: Interrupt Configuration Register 1

GICR_ICFGR<n>E: Interrupt configuration registers

GICR_ICPENDR0: Interrupt Clear-Pending Register 0

GICR_ICPENDR<n>E: Interrupt Clear-Pending Registers

GICR_IGROUPR0: Interrupt Group Register 0

GICR_IGROUPR<n>E: Interrupt Group Registers

GICR_IGRPMODR0: Interrupt Group Modifier Register 0

GICR_IGRPMODR<n>E: Interrupt Group Modifier Registers

GICR_IIDR: Redistributor Implementer Identification Register

GICR_INMIR0: Non-maskable Interrupt Register for PPIs.

GICR_INMIR<n>E: Non-maskable Interrupt Registers for Extended PPIs, x = 1 to 2.

GICR_INVALLR: Redistributor Invalidate All Register

GICR_INVLPIR: Redistributor Invalidate LPI Register

GICR_IPRIORITYR<n>: Interrupt Priority Registers

GICR_IPRIORITYR<n>E: Interrupt Priority Registers (extended PPI range)

GICR_ISACTIVER0: Interrupt Set-Active Register 0

GICR_ISACTIVER<n>E: Interrupt Set-Active Registers

GICR_ISENABLER0: Interrupt Set-Enable Register 0

GICR_ISENABLER<n>E: Interrupt Set-Enable Registers

GICR_ISPENDR0: Interrupt Set-Pending Register 0

GICR_ISPENDR<n>E: Interrupt Set-Pending Registers

GICR_MPAMIDR: Report maximum PARTID and PMG Register

GICR_NSACR: Non-secure Access Control Register

GICR_PARTIDR: Set PARTID and PMG Register

GICR_PENDBASER: Redistributor LPI Pending Table Base Address Register

GICR_PROPBASER: Redistributor Properties Base Address Register

GICR_SETLPIR: Set LPI Pending Register

GICR_STATUSR: Error Reporting Status Register

GICR_SYNCR: Redistributor Synchronize Register

GICR_TYPER: Redistributor Type Register

GICR_VPENDBASER: Virtual Redistributor LPI Pending Table Base Address Register

GICR_VPROPBASER: Virtual Redistributor Properties Base Address Register

GICR_VSGIPENDR: Redistributor virtual SGI pending state register

GICR_VSGIR: Redistributor virtual SGI pending state request register

GICR_WAKER: Redistributor Wake Register

GICV_ABPR: Virtual Machine Aliased Binary Point Register

GICV_AEOIR: Virtual Machine Aliased End Of Interrupt Register

GICV_AHPPIR: Virtual Machine Aliased Highest Priority Pending Interrupt Register

GICV_AIAR: Virtual Machine Aliased Interrupt Acknowledge Register

GICV_APR<n>: Virtual Machine Active Priorities Registers

GICV_BPR: Virtual Machine Binary Point Register

GICV_CTLR: Virtual Machine Control Register

GICV_DIR: Virtual Machine Deactivate Interrupt Register

GICV_EOIR: Virtual Machine End Of Interrupt Register

GICV_HPPIR: Virtual Machine Highest Priority Pending Interrupt Register

GICV_IAR: Virtual Machine Interrupt Acknowledge Register

GICV_IIDR: Virtual Machine CPU Interface Identification Register

GICV_PMR: Virtual Machine Priority Mask Register

GICV_RPR: Virtual Machine Running Priority Register

GICV_STATUSR: Virtual Machine Error Reporting Status Register

GITS_BASER<n>: ITS Translation Table Descriptors

GITS_CBASER: ITS Command Queue Descriptor

GITS_CREADR: ITS Read Register

GITS_CTLR: ITS Control Register

GITS_CWRITER: ITS Write Register

GITS_IIDR: ITS Identification Register

GITS_MPAMIDR: Report maximum PARTID and PMG Register

GITS_MPIDR: Report ITS's affinity.

GITS_PARTIDR: Set PARTID and PMG Register

GITS_SGIR: ITS SGI Register

GITS_STATUSR: ITS Error Reporting Status Register

GITS_TRANSLATER: ITS Translation Register

GITS_TYPER: ITS Type Register

GITS_UMSIR: ITS Unmapped MSI register

MIDR_EL1: Main ID Register

MPAMCFG_CASSOC: MPAM Cache Maximum Associativity Partition Configuration Register

MPAMCFG_CMAX: MPAM Cache Maximum Capacity Partition Configuration Register

MPAMCFG_CMIN: MPAM Cache Minimum Capacity Partition Configuration Register

MPAMCFG_CPBM<n>: MPAM Cache Portion Bitmap Partition Configuration Register

MPAMCFG_DIS: MPAM Partition Configuration Disable Register

MPAMCFG_EN: MPAM Partition Configuration Enable Register

MPAMCFG_EN_FLAGS: MPAM Partition Configuration Enable Flags Register

MPAMCFG_INTPARTID: MPAM Internal PARTID Narrowing Configuration Register

MPAMCFG_MBW_MAX: MPAM Memory Bandwidth Maximum Partition Configuration Register

MPAMCFG_MBW_MIN: MPAM Memory Bandwidth Minimum Partition Configuration Register

MPAMCFG_MBW_PBM<n>: MPAM Bandwidth Portion Bitmap Partition Configuration Register

MPAMCFG_MBW_PROP: MPAM Memory Bandwidth Proportional Stride Partition Configuration Register

MPAMCFG_MBW_WINWD: MPAM Memory Bandwidth Partitioning Window Width Configuration Register

MPAMCFG_PART_SEL: MPAM Partition Configuration Selection Register

MPAMCFG_PRI: MPAM Priority Partition Configuration Register

MPAMF_AIDR: MPAM Architecture Identification Register

MPAMF_CCAP_IDR: MPAM Features Cache Capacity Partitioning ID register

MPAMF_CPOR_IDR: MPAM Features Cache Portion Partitioning ID register

MPAMF_CSUMON_IDR: MPAM Features Cache Storage Usage Monitoring ID register

MPAMF_ECR: MPAM Error Control Register

MPAMF_ERR_MSI_ADDR_H: MPAM Error MSI High-part Address Register

MPAMF_ERR_MSI_ADDR_L: MPAM Error MSI Low-part Address Register

MPAMF_ERR_MSI_ATTR: MPAM Error MSI Write Attributes Register

MPAMF_ERR_MSI_DATA: MPAM Error MSI Data Register

MPAMF_ERR_MSI_MPAM: MPAM Error MSI Write MPAM Information Register

MPAMF_ESR: MPAM Error Status Register

MPAMF_IDR: MPAM Features Identification Register

MPAMF_IIDR: MPAM Implementation Identification Register

MPAMF_IMPL_IDR: MPAM Implementation-Specific Partitioning Feature Identification Register

MPAMF_MBWUMON_IDR: MPAM Features Memory Bandwidth Usage Monitoring ID register

MPAMF_MBW_IDR: MPAM Memory Bandwidth Partitioning Identification Register

MPAMF_MSMON_IDR: MPAM Resource Monitoring Identification Register

MPAMF_PARTID_NRW_IDR: MPAM PARTID Narrowing ID register

MPAMF_PRI_IDR: MPAM Priority Partitioning Identification Register

MPAMF_SIDR: MPAM Features Secure Identification Register

MSMON_CAPT_EVNT: MPAM Capture Event Generation Register

MSMON_CFG_CSU_CTL: MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register

MSMON_CFG_CSU_FLT: MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register

MSMON_CFG_MBWU_CTL: MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register

MSMON_CFG_MBWU_FLT: MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register

MSMON_CFG_MON_SEL: MPAM Monitor Instance Selection Register

MSMON_CSU: MPAM Cache Storage Usage Monitor Register

MSMON_CSU_CAPTURE: MPAM Cache Storage Usage Monitor Capture Register

MSMON_CSU_OFSR: MPAM CSU Monitor Overflow Status Register

MSMON_MBWU: MPAM Memory Bandwidth Usage Monitor Register

MSMON_MBWU_CAPTURE: MPAM Memory Bandwidth Usage Monitor Capture Register

MSMON_MBWU_L: MPAM Long Memory Bandwidth Usage Monitor Register

MSMON_MBWU_L_CAPTURE: MPAM Long Memory Bandwidth Usage Monitor Capture Register

MSMON_MBWU_OFSR: MPAM MBWU Monitor Overflow Status Register

MSMON_OFLOW_MSI_ADDR_H: MPAM Monitor Overflow MSI Write High-part Address Register

MSMON_OFLOW_MSI_ADDR_L: MPAM Monitor Overflow MSI Low-part Address Register

MSMON_OFLOW_MSI_ATTR: MPAM Monitor Overflow MSI Write Attributes Register

MSMON_OFLOW_MSI_DATA: MPAM Monitor Overflow MSI Write Data Register

MSMON_OFLOW_MSI_MPAM: MPAM Monitor Overflow MSI Write MPAM Information Register

MSMON_OFLOW_SR: MPAM Monitor Overflow Status Register

OSLAR_EL1: OS Lock Access Register

PMAUTHSTATUS: Performance Monitors Authentication Status register

PMCCFILTR_EL0: Performance Monitors Cycle Counter Filter Register

PMCCIDSR: CONTEXTIDR_ELx Sample Register

PMCCNTR_EL0: Performance Monitors Cycle Counter

PMCCNTSVR_EL1: Performance Monitors Cycle Count Saved Value Register

PMCEID0: Performance Monitors Common Event Identification register 0

PMCEID1: Performance Monitors Common Event Identification register 1

PMCEID2: Performance Monitors Common Event Identification register 2

PMCEID3: Performance Monitors Common Event Identification register 3

PMCFGR: Performance Monitors Configuration Register

PMCGCR0: Counter Group Configuration Register 0

PMCID1SR: CONTEXTIDR_EL1 Sample Register

PMCID2SR: CONTEXTIDR_EL2 Sample Register

PMCIDR0: Performance Monitors Component Identification Register 0

PMCIDR1: Performance Monitors Component Identification Register 1

PMCIDR2: Performance Monitors Component Identification Register 2

PMCIDR3: Performance Monitors Component Identification Register 3

PMCNTEN: Performance Monitors Count Enable register

PMCNTENCLR_EL0: Performance Monitors Count Enable Clear Register

PMCNTENSET_EL0: Performance Monitors Count Enable Set Register

PMCR_EL0: Performance Monitors Control Register

PMDEVAFF: Performance Monitors Device Affinity register

PMDEVAFF0: Performance Monitors Device Affinity register 0

PMDEVAFF1: Performance Monitors Device Affinity register 1

PMDEVARCH: Performance Monitors Device Architecture register

PMDEVID: Performance Monitors Device ID register

PMDEVTYPE: Performance Monitors Device Type register

PMEVCNTR<n>_EL0: Performance Monitors Event Count Registers

PMEVCNTSVR<n>_EL1: Performance Monitors Event Count Saved Value Register <n>

PMEVFILT2R<n>: Performance Monitors Event Filter Registers

PMEVTYPER<n>_EL0: Performance Monitors Event Type Registers

PMICFILTR_EL0: Performance Monitors Instruction Counter Filter Register

PMICNTR_EL0: Performance Monitors Instruction Counter Register

PMICNTSVR_EL1: Performance Monitors Instruction Count Saved Value Register

PMIIDR: Performance Monitors Implementation Identification Register

PMINTEN: Performance Monitors Interrupt Enable register

PMINTENCLR_EL1: Performance Monitors Interrupt Enable Clear Register

PMINTENSET_EL1: Performance Monitors Interrupt Enable Set Register

PMITCTRL: Performance Monitors Integration mode Control register

PMLAR: Performance Monitors Lock Access Register

PMLSR: Performance Monitors Lock Status Register

PMMIR: Performance Monitors Machine Identification Register

PMOVS: Performance Monitors Overflow Flag Status register

PMOVSCLR_EL0: Performance Monitors Overflow Flag Status Clear register

PMOVSSET_EL0: Performance Monitors Overflow Flag Status Set Register

PMPCSCTL: PC Sample-based Profiling Control Register

PMPCSR: Program Counter Sample Register

PMPIDR0: Performance Monitors Peripheral Identification Register 0

PMPIDR1: Performance Monitors Peripheral Identification Register 1

PMPIDR2: Performance Monitors Peripheral Identification Register 2

PMPIDR3: Performance Monitors Peripheral Identification Register 3

PMPIDR4: Performance Monitors Peripheral Identification Register 4

PMSSCR_EL1: Performance Monitors Snapshot Status and Capture Register

PMSWINC_EL0: Performance Monitors Software Increment Register

PMVCIDSR: CONTEXTIDR_EL1 and VMID Sample Register

PMVIDSR: VMID Sample Register

PMZR_EL0: Performance Monitors Zero with Mask

TRBAUTHSTATUS: Authentication Status Register

TRBBASER_EL1: Trace Buffer Base Address Register

TRBCIDR0: Component Identification Register 0

TRBCIDR1: Component Identification Register 1

TRBCIDR2: Component Identification Register 2

TRBCIDR3: Component Identification Register 3

TRBCR: Trace Buffer Control Register

TRBDEVAFF: Device Affinity Register

TRBDEVARCH: Trace Buffer Device Architecture Register

TRBDEVID: Device Configuration Register

TRBDEVID1: Device Configuration Register 1

TRBDEVID2: Device Configuration Register 2

TRBDEVTYPE: Device Type Register

TRBIDR_EL1: Trace Buffer ID Register

TRBITCTRL: Integration Mode Control Register

TRBLAR: Lock Access Register

TRBLIMITR_EL1: Trace Buffer Limit Address Register

TRBLSR: Lock Status Register

TRBMAR_EL1: Trace Buffer Memory Attribute Register

TRBMPAM_EL1: Trace Buffer MPAM Configuration Register

TRBPIDR0: Peripheral Identification Register 0

TRBPIDR1: Peripheral Identification Register 1

TRBPIDR2: Peripheral Identification Register 2

TRBPIDR3: Peripheral Identification Register 3

TRBPIDR4: Peripheral Identification Register 4

TRBPIDR5: Peripheral Identification Register 5

TRBPIDR6: Peripheral Identification Register 6

TRBPIDR7: Peripheral Identification Register 7

TRBPTR_EL1: Trace Buffer Write Pointer Register

TRBSR_EL1: Trace Buffer Status/syndrome Register

TRBTRG_EL1: Trace Buffer Trigger Counter Register

TRCACATR<n>: Address Comparator Access Type Register <n>

TRCACVR<n>: Address Comparator Value Register <n>

TRCAUTHSTATUS: Authentication Status Register

TRCAUXCTLR: Auxiliary Control Register

TRCBBCTLR: Branch Broadcast Control Register

TRCCCCTLR: Cycle Count Control Register

TRCCIDCCTLR0: Context Identifier Comparator Control Register 0

TRCCIDCCTLR1: Context Identifier Comparator Control Register 1

TRCCIDCVR<n>: Context Identifier Comparator Value Registers <n>

TRCCIDR0: Component Identification Register 0

TRCCIDR1: Component Identification Register 1

TRCCIDR2: Component Identification Register 2

TRCCIDR3: Component Identification Register 3

TRCCLAIMCLR: Claim Tag Clear Register

TRCCLAIMSET: Claim Tag Set Register

TRCCNTCTLR<n>: Counter Control Register <n>

TRCCNTRLDVR<n>: Counter Reload Value Register <n>

TRCCNTVR<n>: Counter Value Register <n>

TRCCONFIGR: Trace Configuration Register

TRCDEVAFF: Device Affinity Register

TRCDEVARCH: Device Architecture Register

TRCDEVID: Device Configuration Register

TRCDEVID1: Device Configuration Register 1

TRCDEVID2: Device Configuration Register 2

TRCDEVTYPE: Device Type Register

TRCEVENTCTL0R: Event Control 0 Register

TRCEVENTCTL1R: Event Control 1 Register

TRCEXTINSELR<n>: External Input Select Register <n>

TRCIDR0: ID Register 0

TRCIDR1: ID Register 1

TRCIDR10: ID Register 10

TRCIDR11: ID Register 11

TRCIDR12: ID Register 12

TRCIDR13: ID Register 13

TRCIDR2: ID Register 2

TRCIDR3: ID Register 3

TRCIDR4: ID Register 4

TRCIDR5: ID Register 5

TRCIDR6: ID Register 6

TRCIDR7: ID Register 7

TRCIDR8: ID Register 8

TRCIDR9: ID Register 9

TRCIMSPEC0: IMP DEF Register 0

TRCIMSPEC<n>: IMP DEF Register <n>

TRCITCTRL: Integration Mode Control Register

TRCITEEDCR: Instrumentation Trace Extension External Debug Control Register

TRCLAR: Lock Access Register

TRCLSR: Lock Status Register

TRCOSLSR: Trace OS Lock Status Register

TRCPDCR: PowerDown Control Register

TRCPDSR: PowerDown Status Register

TRCPIDR0: Peripheral Identification Register 0

TRCPIDR1: Peripheral Identification Register 1

TRCPIDR2: Peripheral Identification Register 2

TRCPIDR3: Peripheral Identification Register 3

TRCPIDR4: Peripheral Identification Register 4

TRCPIDR5: Peripheral Identification Register 5

TRCPIDR6: Peripheral Identification Register 6

TRCPIDR7: Peripheral Identification Register 7

TRCPRGCTLR: Programming Control Register

TRCQCTLR: Q Element Control Register

TRCRSCTLR<n>: Resource Selection Control Register <n>

TRCRSR: Resources Status Register

TRCSEQEVR<n>: Sequencer State Transition Control Register <n>

TRCSEQRSTEVR: Sequencer Reset Control Register

TRCSEQSTR: Sequencer State Register

TRCSSCCR<n>: Single-shot Comparator Control Register <n>

TRCSSCSR<n>: Single-shot Comparator Control Status Register <n>

TRCSSPCICR<n>: Single-shot Processing Element Comparator Input Control Register <n>

TRCSTALLCTLR: Stall Control Register

TRCSTATR: Trace Status Register

TRCSYNCPR: Synchronization Period Register

TRCTRACEIDR: Trace ID Register

TRCTSCTLR: Timestamp Control Register

TRCVICTLR: ViewInst Main Control Register

TRCVIIECTLR: ViewInst Include/Exclude Control Register

TRCVIPCSSCTLR: ViewInst Start/Stop PE Comparator Control Register

TRCVISSCTLR: ViewInst Start/Stop Control Register

TRCVMIDCCTLR0: Virtual Context Identifier Comparator Control Register 0

TRCVMIDCCTLR1: Virtual Context Identifier Comparator Control Register 1

TRCVMIDCVR<n>: Virtual Context Identifier Comparator Value Register <n>

28/03/2023 16:10