

TRBCIDR1, Component Identification Register 1

The TRBCIDR1 characteristics are:

Purpose

Provides discovery information about the component.

For additional information, see the CoreSight Architecture Specification.

Configuration

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBCIDR1 are res0.

TRBCIDR1 is in the Core power domain.

Attributes

TRBCIDR1 is a 32-bit register.

Field descriptions

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|---------|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES0 | | | | | | | | | | | | | | | | CLASS | | | | PRMBL 1 | | | | | | | | | | | |

Bits [31:8]

Reserved, res0.

CLASS, bits [7:4]

Component class.

| CLASS | Meaning |
|--------|-----------------------|
| 0b1001 | CoreSight peripheral. |

Other values are defined by the CoreSight Architecture.

Access to this field is **RO**.

PRMBL_1, bits [3:0]

Component identification preamble, segment 1.

Reads as 0b0000.

Access to this field is **RO**.

Accessing TRBCIDR1

TRBCIDR1 can be accessed through the external debug interface:

| Component | Offset | Instance |
|-----------|--------|----------|
| TRBE | 0xFF4 | TRBCIDR1 |

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

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