External register index by offset

Below are indexes for external registers in the following blocks:

- AMU
- CTI
- Debug
- ETE
- GIC CPU interface
- GIC Distributor
- GIC ITS control
- GIC ITS translation
- GIC Redistributor
- GIC Virtual CPU interface
- GIC Virtual interface control
- MPAM
- PMU
- RAS
- TRBE
- Timer

In the AMU block:

Offset	Name	Description	Access	
0x000 + (8 * n)	AMEVCNTR0<n>[31:0]	Activity Monitors Event Counter Registers 0	RO	-
0x004 + (8 * n)	AMEVCNTR0<n>[63:32]	Activity Monitors Event Counter Registers 0	RO	-
0x100 + (8 * n)	AMEVCNTR1<n>[31:0]	Activity Monitors Event Counter Registers 1	RO	-
0x104 + (8 * n)	AMEVCNTR1<n>[63:32]	Activity Monitors Event Counter Registers 1	RO	-
0x400 + (4 * n)	AMEVTYPER0<n>	Activity Monitors Event Type Registers 0	RO	-

Offset	Name	Description	Access	
0x480 + (4 * n)	AMEVTYPER1<n>	Activity Monitors Event Type Registers 1	RO	-
0xC00	AMCNTENSET0	Activity Monitors Count Enable Set Register 0	RO	-
0xC04	AMCNTENSET1	Activity Monitors Count Enable Set Register 1	RO	-
0xC20	AMCNTENCLR0	Activity Monitors Count Enable Clear Register 0	RO	-
0xC24	AMCNTENCLR1	Activity Monitors Count Enable Clear Register 1	RO	-
0xCE0	AMCGCR	Activity Monitors Counter Group Configuration Register	RO	-
0xE00	AMCFGR	Activity Monitors Configuration Register	RO	-
0xE04	AMCR	Activity Monitors Control Register	RO	-
0xE08	AMIIDR	Activity Monitors Implementation Identification Register	RO	-
0xFA8	AMDEVAFF0	Activity Monitors Device Affinity Register 0	RO	-
0xFAC	AMDEVAFF1	Activity Monitors Device Affinity Register 1	RO	-

Offset	Name	Description	Access	
0xFBC	AMDEVARCH	Activity Monitors Device Architecture Register	RO	-
0xFCC	AMDEVTYPE	Activity Monitors Device Type Register	RO	-
0xFD0	AMPIDR4	Activity Monitors Peripheral Identification Register 4	RO	-
0xFE0	AMPIDR0	Activity Monitors Peripheral Identification Register 0	RO	-
0xFE4	AMPIDR1	Activity Monitors Peripheral Identification Register 1	RO	-
0xFE8	AMPIDR2	Activity Monitors Peripheral Identification Register 2	RO	-
0xFEC	AMPIDR3	Activity Monitors Peripheral Identification Register 3	RO	-
0xFF0	AMCIDR0	Activity Monitors Component Identification Register 0	RO	-
0xFF4	AMCIDR1	Activity Monitors Component Identification Register 1	RO	-
0xFF8	AMCIDR2	Activity Monitors Component Identification Register 2	RO	-

Offset	Name	Description	Access	
0xFFC	AMCIDR3	Activity Monitors Component Identification Register 3	RO	-

In the CTI block:

Offset	Name	Description	Access	
0x000	CTICONTROL	CTI Control register	RW	-
0x010	CTIINTACK	CTI Output Trigger Acknowledge register	WO	-
0x014	CTIAPPSET	CTI Application Trigger Set register	RW	-
0x018	CTIAPPCLEAR	CTI Application Trigger Clear register	WO	-
0x01C	CTIAPPPULSE	CTI Application Pulse register	WO	-
0x020 + (4 * n)	CTIINEN<n>	CTI Input Trigger to Output Channel Enable registers	RW	-
0x0A0 + (4 * n)	CTIOUTEN<n>	CTI Input Channel to Output Trigger Enable registers	RW	-
0x130	CTITRIGINSTATUS	CTI Trigger In Status register	RO	-
0x134	CTITRIGOUTSTATUS	CTI Trigger Out Status register	RO	-
0x138	CTICHINSTATUS	CTI Channel In Status register	RO	-

Offset	Name	Description	Access	
0x13C	CTICHOUTSTATUS	CTI Channel Out Status register	RO	-
0x140	CTIGATE	CTI Channel Gate Enable register	RW	-
0x144	ASICCTL	CTI External Multiplexer Control register	RO	-
0x150	CTIDEVCTL	CTI Device Control register	RW	-
0xF00	CTIITCTRL	CTI Integration mode Control register	RW	-
0xFA0	CTICLAIMSET	CTI CLAIM Tag Set register	RW	-
0xFA4	CTICLAIMCLR	CTI CLAIM Tag Clear register	RW	-
0xFA8	CTIDEVAFF0	CTI Device Affinity register 0	RO	-
0xFAC	CTIDEVAFF1	CTI Device Affinity register 1	RO	-
0xFB0	CTILAR	CTI Lock Access Register	WO	-
0xFB4	CTILSR	CTI Lock Status Register	RO	-
0xFB8	CTIAUTHSTATUS	CTI Authentication Status register	RO	-
0xFBC	CTIDEVARCH	CTI Device Architecture register	RO	-
0xFC0	CTIDEVID2	CTI Device ID register 2	RO	-
0xFC4	CTIDEVID1	CTI Device ID register 1	RO	-
0xFC8	CTIDEVID	CTI Device ID register 0	RO	-

Offset	Name	Description	Access	
0xFCC	CTIDEVTYPE	CTI Device Type register	RO	-
0xFD0	CTIPIDR4	CTI Peripheral Identification Register 4	RO	-
0xFE0	CTIPIDR0	CTI Peripheral Identification Register 0	RO	-
0xFE4	CTIPIDR1	CTI Peripheral Identification Register 1	RO	-
0xFE8	CTIPIDR2	CTI Peripheral Identification Register 2	RO	-
0xFEC	CTIPIDR3	CTI Peripheral Identification Register 3	RO	-
0xFF0	CTICIDR0	CTI Component Identification Register 0	RO	-
0xFF4	CTICIDR1	CTI Component Identification Register 1	RO	-
0xFF8	CTICIDR2	CTI Component Identification Register 2	RO	-
0xFFC	CTICIDR3	CTI Component Identification Register 3	RO	-

In the Debug block:

Offset	Name	Description	Access	
0x020	EDESR	External Debug Event Status Register	RW	-
0x024	EDECR	External Debug Execution Control Register	RW	-

Offset	Name	Description	Access	
0x028	EDSCR2	External Debug Status and Control Register 2	RW	-
0x030	EDWAR[31:0]	External Debug Watchpoint Address Register	RO	-
0x034	EDWAR[63:32]	External Debug Watchpoint Address Register	RO	-
0x038	EDHSR	External Debug Halting Syndrome Register	RO	-
0x080	DBGDTRRX_EL0	Debug Data Transfer Register, Receive	RW	-
0x084	EDITR	External Debug Instruction Transfer Register	WO	-
0x088	EDSCR	External Debug Status and Control Register	RW	-
0x08C	DBGDTRTX_EL0	Debug Data Transfer Register, Transmit	RW	-
0x090	EDRCR	External Debug Reserve Control Register	WO	-
0x094	EDACR	External Debug Auxiliary Control Register	RW	-

Offset	Name	Description	Access	
0x098	EDECCR	External Debug Exception Catch Control Register	RW	-
0x0A0	EDPCSR[31:0]	External Debug Program Counter Sample Register	RO	-
0x0A4	EDCIDSR	External Debug Context ID Sample Register	RO	-
0x0A8	EDVIDSR	External Debug Virtual Context Sample Register	RO	-
0x0AC	EDPCSR[63:32]	External Debug Program Counter Sample Register	RO	-
0x300	OSLAR_EL1	OS Lock Access Register	WO	-
0x310	EDPRCR	External Debug Power/ Reset Control Register	RW	-
0x314	EDPRSR	External Debug Processor Status Register	RO	-
0x400 + (16 * n)	DBGBVR<n>_EL1[63:0]	Debug Breakpoint Value Registers	RW	-
0x408 + (16 * n)	DBGBCR<n>_EL1	Debug Breakpoint Control Registers	RW	-

Offset	Name	Description	Access	
0x800 + (16 * n)	DBGWVR<n>_EL1[63:0]	Debug Watchpoint Value Registers	RW	-
0x808 + (16 * n)	DBGWCR<n>_EL1	Debug Watchpoint Control Registers	RW	-
0xD00	MIDR_EL1	Main ID Register	RO	-
0xD20	EDPFR[31:0]	External Debug Processor Feature Register	RO	-
0xD24	EDPFR[63:32]	External Debug Processor Feature Register	RO	-
0xD28	EDDFR[31:0]	External Debug Feature Register	RO	-
0xD2C	EDDFR[63:32]	External Debug Feature Register	RO	-
0xD48	EDDFR1[31:0]	External Debug Feature Register 1	RO	-
0xD4C	EDDFR1[63:32]	External Debug Feature Register 1	RO	-
0xD60	EDAA32PFR	External Debug Auxiliary Processor Feature Register	RO	-
0xF00	EDITCTRL	External Debug Integration mode Control register	RW	-

Offset	Name	Description	Access	
0xFA0	DBGCLAIMSET_EL1	Debug CLAIM Tag Set Register	RW	-
0xFA4	DBGCLAIMCLR_EL1	Debug CLAIM Tag Clear Register	RW	-
0xFA8	EDDEVAFF0	External Debug Device Affinity register 0	RO	-
0xFAC	EDDEVAFF1	External Debug Device Affinity register 1	RO	-
0xFB0	EDLAR	External Debug Lock Access Register	WO	-
0xFB4	EDLSR	External Debug Lock Status Register	RO	-
0xFB8	DBGAUTHSTATUS_EL1	Debug Authentication Status Register	RO	-
0xFBC	EDDEVARCH	External Debug Device Architecture register	RO	-
0xFC0	EDDEVID2	External Debug Device ID register 2	RO	-
0xFC4	EDDEVID1	External Debug Device ID register 1	RO	-
0xFC8	EDDEVID	External Debug Device ID register 0	RO	-
0xFCC	EDDEVTYPE	External Debug Device Type register	RO	-
0xFD0	EDPIDR4	External Debug Peripheral Identification Register 4	RO	-

Offset	Name	Description	Access	
0xFE0	EDPIDR0	External Debug Peripheral Identification Register 0	RO	-
0xFE4	EDPIDR1	External Debug Peripheral Identification Register 1	RO	-
0xFE8	EDPIDR2	External Debug Peripheral Identification Register 2	RO	-
0xFEC	EDPIDR3	External Debug Peripheral Identification Register 3	RO	-
0xFF0	EDCIDR0	External Debug Component Identification Register 0	RO	-
0xFF4	EDCIDR1	External Debug Component Identification Register 1	RO	-
0xFF8	EDCIDR2	External Debug Component Identification Register 2	RO	-
0xFFC	EDCIDR3	External Debug Component Identification Register 3	RO	-

In the ETE block:

Offset	Name	Description	Access	
0x004	TRCPRGCTLR	Programming Control Register	RW	-
0x00C	TRCSTATR	Trace Status Register	RO	-

Offset	Name	Description	Access	
0x010	TRCCONFIGR	Trace Configuration Register	RW	-
0x018	TRCAUXCTLR	Auxiliary Control Register	RW	-
0x020	TRCEVENTCTL0R	Event Control 0 Register	RW	-
0x024	TRCEVENTCTL1R	Event Control 1 Register	RW	-
0x028	TRCRSR	Resources Status Register	RW	-
0x02C	TRCSTALLCTLR	Stall Control Register	RW	-
0x030	TRCTSCTLR	Timestamp Control Register	RW	-
0x034	TRCSYNCPR	Synchronization Period Register	RW	-
0x038	TRCCCCTLR	Cycle Count Control Register	RW	-
0x03C	TRCBBCTLR	Branch Broadcast Control Register	RW	-
0x040	TRCTRACEIDR	Trace ID Register	RW	-
0x044	TRCQCTLR	Q Element Control Register	RW	-
0x048	TRCITEEDCR	Instrumentation Trace Extension External Debug Control Register	RW	-
0x080	TRCVICTLR	ViewInst Main Control Register	RW	-
0x084	TRCVIIECTLR	ViewInst Include/Exclude Control Register	RW	-
0x088	TRCVISSCTLR	ViewInst Start/ Stop Control Register	RW	-

Offset	Name	Description	Access	
0x08C	TRCVIPCSSCTLR	ViewInst Start/ Stop PE Comparator Control Register	RW	-
0x100 + (4 * n)	TRCSEQEVR<n>	Sequencer State Transition Control Register <n>	RW	-
0x118	TRCSEQRSTEVR	Sequencer Reset Control Register	RW	-
0x11C	TRCSEQSTR	Sequencer State Register	RW	-
0x120 + (4 * n)	TRCEXTINSELR<n>	External Input Select Register <n>	RW	-
0x140 + (4 * n)	TRCCNTRLDVR<n>	Counter Reload Value Register <n>	RW	-
0x150 + (4 * n)	TRCCNTCTLR<n>	Counter Control Register <n>	RW	-
0x160 + (4 * n)	TRCCNTVR<n>	Counter Value Register <n>	RW	-
0x180	TRCIDR8	ID Register 8	RO	-
0x184	TRCIDR9	ID Register 9	RO	-
0x188	TRCIDR10	ID Register 10	RO	-
0x18C	TRCIDR11	ID Register 11	RO	-
0x190	TRCIDR12	ID Register 12	RO	-
0x194	TRCIDR13	ID Register 13	RO	-
0x1C0	TRCIMSPEC0	IMP DEF Register 0	RW	-
0x1C0 + (4 * n)	TRCIMSPEC<n>	IMP DEF Register <n>	RW	-
0x1E0	TRCIDR0	ID Register 0	RO	-
0x1E4	TRCIDR1	ID Register 1	RO	-
0x1E8	TRCIDR2	ID Register 2	RO	-
0x1EC	TRCIDR3	ID Register 3	RO	-
0x1F0	TRCIDR4	ID Register 4	RO	-
0x1F4	TRCIDR5	ID Register 5	RO	-
0x1F8	TRCIDR6	ID Register 6	RO	-
0x1FC	TRCIDR7	ID Register 7	RO	-

Offset	Name	Description	Access	
0x200 + (4 * n)	TRCRSCTLR<n>	Resource Selection Control Register <n>	RW	-
0x280 + (4 * n)	TRCSSCCR<n>	Single-shot Comparator Control Register <n>	RW	-
0x2A0 + (4 * n)	TRCSSCSR<n>	Single-shot Comparator Control Status Register <n>	RW	-
0x2C0 + (4 * n)	TRCSSPCICR<n>	Single-shot Processing Element Comparator Input Control Register <n>	RW	-
0x304	TRCOSLSR	Trace OS Lock Status Register	RO	-
0x310	TRCPDCR	PowerDown Control Register	RW	-
0x314	TRCPDSR	PowerDown Status Register	RO	-
0x400 + (8 * n)	TRCACVR<n>	Address Comparator Value Register <n>	RW	-
0x480 + (8 * n)	TRCACATR<n>	Address Comparator Access Type Register <n>	RW	-
0x600 + (8 * n)	TRCCIDCVR<n>	Context Identifier Comparator Value Registers <n>	RW	-
0x640 + (8 * n)	TRCVMIDCVR<n>	Virtual Context Identifier Comparator Value Register <n>	RW	-
0x680	TRCCIDCCTLR0	Context Identifier Comparator Control Register 0	RW	-

Offset	Name	Description	Access	
0x684	TRCCIDCCTLR1	Context Identifier Comparator Control Register 1	RW	-
0x688	TRCVMIDCCTLR0	Virtual Context Identifier Comparator Control Register 0	RW	-
0x68C	TRCVMIDCCTLR1	Virtual Context Identifier Comparator Control Register 1	RW	-
0xF00	TRCITCTRL	Integration Mode Control Register	RW	-
0xFA0	TRCCLAIMSET	Claim Tag Set Register	RW	-
0xFA4	TRCCLAIMCLR	Claim Tag Clear Register	RW	-
0xFA8	TRCDEVAFF	Device Affinity Register	RO	-
0xFB0	TRCLAR	Lock Access Register	WO	-
0xFB4	TRCLSR	Lock Status Register	RO	-
0xFB8	TRCAUTHSTATUS	Authentication Status Register	RO	-
0xFBC	TRCDEVARCH	Device Architecture Register	RO	-
0xFC0	TRCDEVID2	Device Configuration Register 2	RO	-
0xFC4	TRCDEVID1	Device Configuration Register 1	RO	-
0xFC8	TRCDEVID	Device Configuration Register	RO	-
0xFCC	TRCDEVTYPE	Device Type Register	RO	-
0xFD0	TRCPIDR4	Peripheral Identification Register 4	RO	-

Offset	Name	Description	Access	
0xFD4	TRCPIDR5	Peripheral Identification Register 5	RO	-
0xFD8	TRCPIDR6	Peripheral Identification Register 6	RO	-
0xFDC	TRCPIDR7	Peripheral Identification Register 7	RO	-
0xFE0	TRCPIDR0	Peripheral Identification Register 0	RO	-
0xFE4	TRCPIDR1	Peripheral Identification Register 1	RO	-
0xFE8	TRCPIDR2	Peripheral Identification Register 2	RO	-
0xFEC	TRCPIDR3	Peripheral Identification Register 3	RO	-
0xFF0	TRCCIDR0	Component Identification Register 0	RO	-
0xFF4	TRCCIDR1	Component Identification Register 1	RO	-
0xFF8	TRCCIDR2	Component Identification Register 2	RO	-
0xFFC	TRCCIDR3	Component Identification Register 3	RO	-

In the GIC CPU interface block:

Offset	Name	Description	Access	
0x0000	GICC_CTLR	CPU Interface Control Register	RW	-
0x0004	GICC_PMR	CPU Interface Priority Mask Register	RW	-

Offset	Name	Description	Access	
0x0008	GICC_BPR	CPU Interface Binary Point Register	RW	-
0x000C	GICC_IAR	CPU Interface Interrupt Acknowledge Register	RO	-
0x0010	GICC_EOIR	CPU Interface End Of Interrupt Register	WO	-
0x0014	GICC_RPR	CPU Interface Running Priority Register	RO	-
0x0018	GICC_HPPIR	CPU Interface Highest Priority Pending Interrupt Register	RO	-
0x001C	GICC_ABPR	CPU Interface Aliased Binary Point Register	RW	-
0x0020	GICC_AIAR	CPU Interface Aliased Interrupt Acknowledge Register	RO	-
0x0024	GICC_AEOIR	CPU Interface Aliased End Of Interrupt Register	WO	-

Offset	Name	Description	Access	
0x0028	GICC_AHPPIR	CPU Interface Aliased Highest Priority Pending Interrupt Register	RO	-
0x002C	GICC_STATUSR	CPU Interface Status Register	RW	-
0x002C	GICC_STATUSR	CPU Interface Status Register	RW	-
0x00D0 + (4 * n)	GICC_APR<n>	CPU Interface Active Priorities Registers	RW	-
0x00E0 + (4 * n)	GICC_NSAPR<n>	CPU Interface Non-secure Active Priorities Registers	RW	-
0x00FC	GICC_IIDR	CPU Interface Identification Register	RO	-
0x1000	GICC_DIR	CPU Interface Deactivate Interrupt Register	WO	-

In the GIC Distributor block:

In the Dist_base block:

Offset	Name	Description	Access
0x0000	GICD_CTLR	Distributor Control Register	RW
0x0004	GICD_TYPER	Interrupt Controller Type Register	RO

Offset	Name	Description	Access
0x0008	GICD_IIDR	Distributor Implementer Identification Register	RO
0x000C	GICD_TYPER2	Interrupt Controller Type Register 2	RO
0x0010	GICD_STATUSR	Error Reporting Status Register	RW
0x0010	GICD_STATUSR	Error Reporting Status Register	RW
0x0040	GICD_SETSPI_NSR	Set Non-secure SPI Pending Register	WO
0x0048	GICD_CLRSPI_NSR	Clear Non-secure SPI Pending Register	WO
0x0050	GICD_SETSPI_SR	Set Secure SPI Pending Register	WO
0x0058	GICD_CLRSPI_SR	Clear Secure SPI Pending Register	WO
0x0080 + (4 * n)	GICD_IGROUPR<n>	Interrupt Group Registers	RW
0x0100 + (4 * n)	GICD_ISENABLER<n>	Interrupt Set-Enable Registers	RW
0x0180 + (4 * n)	GICD_ICENABLER<n>	Interrupt Clear-Enable Registers	RW
0x0200 + (4 * n)	GICD_ISPENDR<n>	Interrupt Set-Pending Registers	RW
0x0280 + (4 * n)	GICD_ICPENDR<n>	Interrupt Clear-Pending Registers	RW
0x0300 + (4 * n)	GICD_ISACTIVER<n>	Interrupt Set-Active Registers	RW

Offset	Name	Description	Access
0x0380 + (4 * n)	GICD_ICACTIVER<n>	Interrupt Clear-Active Registers	RW
0x0400 + (4 * n)	GICD_IPRIORITYR<n>	Interrupt Priority Registers	RW
0x0800 + (4 * n)	GICD_ITARGETSR<n>	Interrupt Processor Targets Registers	RW
0x0C00 + (4 * n)	GICD_ICFGR<n>	Interrupt Configuration Registers	RW
0x0D00 + (4 * n)	GICD_IGRPMODR<n>	Interrupt Group Modifier Registers	RW
0x0E00 + (4 * n)	GICD_NSACR<n>	Non-secure Access Control Registers	RW
0x0F00	GICD_SGIR	Software Generated Interrupt Register	WO
0x0F10 + (4 * n)	GICD_CPENDSGIR<n>	SGI Clear-Pending Registers	RW
0x0F20 + (4 * n)	GICD_SPENDSGIR<n>	SGI Set-Pending Registers	RW
0x0F80 + (4 * n)	GICD_INMIR<n>	Non-maskable Interrupt Registers, x = 0 to 31	RW
0x1000 + (4 * n)	GICD_IGROUPR<n>E	Interrupt Group Registers (extended SPI range)	RW
0x1200 + (4 * n)	GICD_ISENABLER<n>E	Interrupt Set-Enable Registers	RW
0x1400 + (4 * n)	GICD_ICENABLER<n>E	Interrupt Clear-Enable Registers	RW

Offset	Name	Description	Access
0x1600 + (4 * n)	GICD_ISPENDR<n>E	Interrupt Set-Pending Registers (extended SPI range)	RW
0x1800 + (4 * n)	GICD_ICPENDR<n>E	Interrupt Clear-Pending Registers (extended SPI range)	RW
0x1A00 + (4 * n)	GICD_ISACTIVER<n>E	Interrupt Set-Active Registers (extended SPI range)	RW
0x1C00 + (4 * n)	GICD_ICACTIVER<n>E	Interrupt Clear-Active Registers (extended SPI range)	RW
0x2000 + (4 * n)	GICD_IPRIORITYR<n>E	Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC.	RW
0x3000 + (4 * n)	GICD_ICFGR<n>E	Interrupt Configuration Registers (Extended SPI Range)	RW
0x3400 + (4 * n)	GICD_IGRPMODR<n>E	Interrupt Group Modifier Registers (extended SPI range)	RW
0x3600 + (4 * n)	GICD_NSACR<n>E	Non-secure Access Control Registers	RW
0x3B00 + (4 * n)	GICD_INMIR<n>E	Non-maskable Interrupt Registers for Extended SPIs, x = 0 to 31	RW

Offset	Name	Description	Access
0x6000 + (8 * n)	GICD_IROUTER<n>	Interrupt Routing Registers	RW
0x8000 + (8 * n)	GICD_IROUTER<n>E	Interrupt Routing Registers (Extended SPI Range)	RW

In the MSI_base block:

Offset	Name	Description	Access
0x0004	GICM_TYPER	Distributor MSI Type Register	RO
0x0040	GICM_SETSPI_NSR	Set Non-secure SPI Pending Register	WO
0x0048	GICM_CLRSPI_NSR	Clear Non-secure SPI Pending Register	WO
0x0050	GICM_SETSPI_SR	Set Secure SPI Pending Register	WO
0x0058	GICM_CLRSPI_SR	Clear Secure SPI Pending Register	WO
0x0FCC	GICM_IIDR	Distributor Implementer Identification Register	RO

In the GIC ITS control block:

Offset	Name	Description	Access	
0x0000	GITS_CTLR	ITS Control Register	RW	-
0x0004	GITS_IIDR	ITS Identification Register	RO	-
0x0008	GITS_TYPER	ITS Type Register	RO	-
0x0010	GITS_MPAMIDR	Report maximum PARTID and PMG Register	RO	-
0x0014	GITS_PARTIDR	Set PARTID and PMG Register	RW	-
0x0018	GITS_MPIDR	Report ITS's affinity.	RO	-

Offset	Name	Description	Access	
0x0040	GITS_STATUSR	ITS Error Reporting Status Register	RW	-
0x0048	GITS_UMSIR	ITS Unmapped MSI register	RO	-
0x0080	GITS_CBASER	ITS Command Queue Descriptor	RW	-
0x0088	GITS_CWRITER	ITS Write Register	RW	-
0x0090	GITS_CREADR	ITS Read Register	RO	-
0x0100 + (8 * n)	GITS_BASER<n>	ITS Translation Table Descriptors	RW	-
0x20020	GITS_SGIR	ITS SGI Register	WO	-

In the GIC ITS translation block:

Offset	Name	Description	Access	
0x0040	GITS_TRANSLATER	ITS Translation Register	WO	-

In the GIC Redistributor block:

In the RD_base block:

Offset	Name	Description	Access
0x0000	GICR_CTLR	Redistributor Control Register	RW
0x0004	GICR_IIDR	Redistributor Implementer Identification Register	RO
0x0008	GICR_TYPER	Redistributor Type Register	RO
0x0010	GICR_STATUSR	Error Reporting Status Register	RW
0x0010	GICR_STATUSR	Error Reporting Status Register	RW
0x0014	GICR_WAKER	Redistributor Wake Register	RW
0x0018	GICR_MPAMIDR	Report maximum PARTID and PMG Register	RO

Offset	Name	Description	Access
0x001C	GICR_PARTIDR	Set PARTID and PMG Register	RW
0x0040	GICR_SETLPIR	Set LPI Pending Register	WO
0x0048	GICR_CLRLPIR	Clear LPI Pending Register	WO
0x0070	GICR_PROPBASER	Redistributor Properties Base Address Register	RW
0x0078	GICR_PENDBASER	Redistributor LPI Pending Table Base Address Register	RW
0x00A0	GICR_INVLPIR	Redistributor Invalidate LPI Register	WO
0x00B0	GICR_INVALLR	Redistributor Invalidate All Register	WO
0x00C0	GICR_SYNCR	Redistributor Synchronize Register	RO

In the SGI_base block:

Offset	Name	Description	Access
0x0080	GICR_IGROUPR0	Interrupt Group Register 0	RW
0x0080 + (4 * n)	GICR_IGROUPR<n>E	Interrupt Group Registers	RW
0x0100	GICR_ISENABLER0	Interrupt Set-Enable Register 0	RW
0x0100 + (4 * n)	GICR_ISENABLER<n>E	Interrupt Set-Enable Registers	RW
0x0180	GICR_ICENABLER0	Interrupt Clear-Enable Register 0	RW
0x0180 + (4 * n)	GICR_ICENABLER<n>E	Interrupt Clear-Enable Registers	RW
0x0200	GICR_ISPENDR0	Interrupt Set-Pending Register 0	RW
0x0200 + (4 * n)	GICR_ISPENDR<n>E	Interrupt Set-Pending Registers	RW

Offset	Name	Description	Access
0x0280	GICR_ICPENDR0	Interrupt Clear-Pending Register 0	RW
0x0280 + (4 * n)	GICR_ICPENDR<n>E	Interrupt Clear-Pending Registers	RW
0x0300	GICR_ISACTIVER0	Interrupt Set-Active Register 0	RW
0x0300 + (4 * n)	GICR_ISACTIVER<n>E	Interrupt Set-Active Registers	RW
0x0380	GICR_ICACTIVER0	Interrupt Clear-Active Register 0	RW
0x0380 + (4 * n)	GICR_ICACTIVER<n>E	Interrupt Clear-Active Registers	RW
0x0400 + (4 * n)	GICR_IPRIORITYR<n>	Interrupt Priority Registers	RW
0x0400 + (4 * n)	GICR_IPRIORITYR<n>E	Interrupt Priority Registers (extended PPI range)	RW
0x0C00	GICR_ICFGR0	Interrupt Configuration Register 0	RW
0x0C00 + (4 * n)	GICR_ICFGR<n>E	Interrupt configuration registers	RW
0x0C04	GICR_ICFGR1	Interrupt Configuration Register 1	RW
0x0D00	GICR_IGRPMODR0	Interrupt Group Modifier Register 0	RW
0x0D00 + (4 * n)	GICR_IGRPMODR<n>E	Interrupt Group Modifier Registers	RW

Offset	Name	Description	Access
0x0E00	GICR_NSACR	Non-secure Access Control Register	RW
0x0F80	GICR_INMIR0	Non-maskable Interrupt Register for PPIs.	RW
0x0F80 + (4 * n)	GICR_INMIR<n>E	Non-maskable Interrupt Registers for Extended PPIs, x = 1 to 2.	RW

In the VLPI_base block:

Offset	Name	Description	Access
0x0070	GICR_VPROPBASER	Virtual Redistributor Properties Base Address Register	RW
0x0078	GICR_VPENDBASER	Virtual Redistributor LPI Pending Table Base Address Register	RW
0x0080	GICR_VSGIR	Redistributor virtual SGI pending state request register	WO
0x0088	GICR_VSGIPENDR	Redistributor virtual SGI pending state register	RO

In the GIC Virtual CPU interface block:

Offset	Name	Description	Access	
0x0000	GICV_CTLR	Virtual Machine Control Register	RW	-
0x0004	GICV_PMR	Virtual Machine Priority Mask Register	RW	-
0x0008	GICV_BPR	Virtual Machine Binary Point Register	RW	-

Offset	Name	Description	Access	
0x000C	GICV_IAR	Virtual Machine Interrupt Acknowledge Register	RO	-
0x0010	GICV_EOIR	Virtual Machine End Of Interrupt Register	WO	-
0x0014	GICV_RPR	Virtual Machine Running Priority Register	RO	-
0x0018	GICV_HPPIR	Virtual Machine Highest Priority Pending Interrupt Register	RO	-
0x001C	GICV_ABPR	Virtual Machine Aliased Binary Point Register	RW	-
0x0020	GICV_AIAR	Virtual Machine Aliased Interrupt Acknowledge Register	RO	-
0x0024	GICV_AEOIR	Virtual Machine Aliased End Of Interrupt Register	WO	-
0x0028	GICV_AHPPIR	Virtual Machine Aliased Highest Priority Pending Interrupt Register	RO	-

Offset	Name	Description	Access	
0x002C	GICV_STATUSR	Virtual Machine Error Reporting Status Register	RW	-
0x00D0 + (4 * n)	GICV_APR<n>	Virtual Machine Active Priorities Registers	RW	-
0x00FC	GICV_IIDR	Virtual Machine CPU Interface Identification Register	RO	-
0x1000	GICV_DIR	Virtual Machine Deactivate Interrupt Register	WO	-

In the GIC Virtual interface control block:

Offset	Name	Description	Access	
0x0000	GICH_HCR	Hypervisor Control Register	RW	-
0x0004	GICH_VTR	Virtual Type Register	RO	-
0x0008	GICH_VMCR	Virtual Machine Control Register	RW	-
0x0010	GICH_MISR	Maintenance Interrupt Status Register	RO	-
0x0020	GICH_EISR	End Interrupt Status Register	RO	-
0x0030	GICH_ELRSR	Empty List Register Status Register	RO	-
0x00F0 + (4 * n)	GICH_APR<n>	Active Priorities Registers	RW	-

Offset	Name	Description	Access	
0x0100 + (4 * n)	GICH_LR<n>	List Registers	RW	-

In the MPAM block:

In the MPAMF_BASE_ns block:

Offset	Name	Description	Acces
0x0000	MPAMF_IDR	MPAM Features Identification Register	RO
0x0018	MPAMF_IIDR	MPAM Implementation Identification Register	RO
0x0020	MPAMF_AIDR	MPAM Architecture Identification Register	RO
0x0028	MPAMF_IMPL_IDR	MPAM Implementation-Specific Partitioning Feature Identification Register	RO
0x0030	MPAMF_CPOR_IDR	MPAM Features Cache Portion Partitioning ID register	RO
0x0038	MPAMF_CCAP_IDR	MPAM Features Cache Capacity Partitioning ID register	RO
0x0040	MPAMF_MBW_IDR	MPAM Memory Bandwidth Partitioning Identification Register	RO
0x0048	MPAMF_PRI_IDR	MPAM Priority Partitioning Identification Register	RO
0x0050	MPAMF_PARTID_NRW_IDR	MPAM PARTID Narrowing ID register	RO

Offset	Name	Description	Acce
0x0080	MPAMF_MSMON_IDR	MPAM Resource Monitoring Identification Register	RO
0x0088	MPAMF_CSUMON_IDR	MPAM Features Cache Storage Usage Monitoring ID register	RO
0x0090	MPAMF_MBWUMON_IDR	MPAM Features Memory Bandwidth Usage Monitoring ID register	RO
0x00DC	MPAMF_ERR_MSI_MPAM	MPAM Error MSI Write MPAM Information Register	RW
0x00E0	MPAMF_ERR_MSI_ADDR_L	MPAM Error MSI Low-part Address Register	RW
0x00E4	MPAMF_ERR_MSI_ADDR_H	MPAM Error MSI High-part Address Register	RW
0x00E8	MPAMF_ERR_MSI_DATA	MPAM Error MSI Data Register	RW
0x00EC	MPAMF_ERR_MSI_ATTR	MPAM Error MSI Write Attributes Register	RW
0x00F0	MPAMF_ECR	MPAM Error Control Register	RW
0x00F8	MPAMF_ESR	MPAM Error Status Register	RW
0x0100	MPAMCFG_PART_SEL	MPAM Partition Configuration Selection Register	RW

Offset	Name	Description	Acce
0x0108	MPAMCFG_CMAX	MPAM Cache Maximum Capacity Partition Configuration Register	RW
0x0110	MPAMCFG_CMIN	MPAM Cache Minimum Capacity Partition Configuration Register	RW
0x0118	MPAMCFG_CASSOC	MPAM Cache Maximum Associativity Partition Configuration Register	RW
0x0200	MPAMCFG_MBW_MIN	MPAM Memory Bandwidth Minimum Partition Configuration Register	RW
0x0208	MPAMCFG_MBW_MAX	MPAM Memory Bandwidth Maximum Partition Configuration Register	RW
0x0220	MPAMCFG_MBW_WINWD	MPAM Memory Bandwidth Partitioning Window Width Configuration Register	RW
0x0300	MPAMCFG_EN	MPAM Partition Configuration Enable Register	WO/ RAZ
0x0310	MPAMCFG_DIS	MPAM Partition Configuration Disable Register	WO/ RAZ
0x0320	MPAMCFG_EN_FLAGS	MPAM Partition Configuration Enable Flags Register	RW

Offset	Name	Description	Acce
0x0400	MPAMCFG_PRI	MPAM Priority Partition Configuration Register	RW
0x0500	MPAMCFG_MBW_PROP	MPAM Memory Bandwidth Proportional Stride Partition Configuration Register	RW
0x0600	MPAMCFG_INTPARTID	MPAM Internal PARTID Narrowing Configuration Register	RW
0x0800	MSMON_CFG_MON_SEL	MPAM Monitor Instance Selection Register	RW
0x0808	MSMON_CAPT_EVNT	MPAM Capture Event Generation Register	WO/ RAZ
0x0810	MSMON_CFG_CSU_FLT	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register	RW
0x0818	MSMON_CFG_CSU_CTL	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register	RW
0x0820	MSMON_CFG_MBWU_FLT	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register	RW

Offset	Name	Description	Acce
0x0828	MSMON_CFG_MBWU_CTL	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register	RW
0x0840	MSMON_CSU	MPAM Cache Storage Usage Monitor Register	RW
0x0848	MSMON_CSU_CAPTURE	MPAM Cache Storage Usage Monitor Capture Register	RW
0x0858	MSMON_CSU_OFSR	MPAM CSU Monitor Overflow Status Register	RO
0x0860	MSMON_MBWU	MPAM Memory Bandwidth Usage Monitor Register	RW
0x0868	MSMON_MBWU_CAPTURE	MPAM Memory Bandwidth Usage Monitor Capture Register	RW
0x0880	MSMON_MBWU_L	MPAM Long Memory Bandwidth Usage Monitor Register	RW
0x0890	MSMON_MBWU_L_CAPTURE	MPAM Long Memory Bandwidth Usage Monitor Capture Register	RW
0x0898	MSMON_MBWU_OFSR	MPAM MBWU Monitor Overflow Status Register	RO

Offset	Name	Description	Acces
0x08DC	MSMON_OFLOW_MSI_MPAM	MPAM Monitor Overflow MSI Write MPAM Information Register	RW
0x08E0	MSMON_OFLOW_MSI_ADDR_L	MPAM Monitor Overflow MSI Low-part Address Register	RW
0x08E4	MSMON_OFLOW_MSI_ADDR_H	MPAM Monitor Overflow MSI Write High-part Address Register	RW
0x08E8	MSMON_OFLOW_MSI_DATA	MPAM Monitor Overflow MSI Write Data Register	RW
0x08EC	MSMON_OFLOW_MSI_ATTR	MPAM Monitor Overflow MSI Write Attributes Register	RW
0x08F0	MSMON_OFLOW_SR	MPAM Monitor Overflow Status Register	RO
0x1000 + (4 * n)	MPAMCFG_CPBM<n>	MPAM Cache Portion Bitmap Partition Configuration Register	RW
0x2000 + (4 * n)	MPAMCFG_MBW_PBM<n>	MPAM Bandwidth Portion Bitmap Partition Configuration Register	RW

In the MPAMF_BASE_rl block:

Offset	Name	Description	Acces
0x0000	MPAMF_IDR	MPAM Features Identification Register	RO
0x0018	MPAMF_IIDR	MPAM Implementation Identification Register	RO

Offset	Name	Description	Acce
0x0020	MPAMF_AIDR	MPAM Architecture Identification Register	RO
0x0028	MPAMF_IMPL_IDR	MPAM Implementation-Specific Partitioning Feature Identification Register	RO
0x0030	MPAMF_CPOR_IDR	MPAM Features Cache Portion Partitioning ID register	RO
0x0038	MPAMF_CCAP_IDR	MPAM Features Cache Capacity Partitioning ID register	RO
0x0040	MPAMF_MBW_IDR	MPAM Memory Bandwidth Partitioning Identification Register	RO
0x0048	MPAMF_PRI_IDR	MPAM Priority Partitioning Identification Register	RO
0x0050	MPAMF_PARTID_NRW_IDR	MPAM PARTID Narrowing ID register	RO
0x0080	MPAMF_MSMON_IDR	MPAM Resource Monitoring Identification Register	RO
0x0088	MPAMF_CSUMON_IDR	MPAM Features Cache Storage Usage Monitoring ID register	RO
0x0090	MPAMF_MBWUMON_IDR	MPAM Features Memory Bandwidth Usage Monitoring ID register	RO

Offset	Name	Description	Acce
0x00DC	MPAMF_ERR_MSI_MPAM	MPAM Error MSI Write MPAM Information Register	RW
0x00E0	MPAMF_ERR_MSI_ADDR_L	MPAM Error MSI Low-part Address Register	RW
0x00E4	MPAMF_ERR_MSI_ADDR_H	MPAM Error MSI High-part Address Register	RW
0x00E8	MPAMF_ERR_MSI_DATA	MPAM Error MSI Data Register	RW
0x00EC	MPAMF_ERR_MSI_ATTR	MPAM Error MSI Write Attributes Register	RW
0x00F0	MPAMF_ECR	MPAM Error Control Register	RW
0x00F8	MPAMF_ESR	MPAM Error Status Register	RW
0x0100	MPAMCFG_PART_SEL	MPAM Partition Configuration Selection Register	RW
0x0108	MPAMCFG_CMAX	MPAM Cache Maximum Capacity Partition Configuration Register	RW
0x0110	MPAMCFG_CMIN	MPAM Cache Minimum Capacity Partition Configuration Register	RW
0x0118	MPAMCFG_CASSOC	MPAM Cache Maximum Associativity Partition Configuration Register	RW

Offset	Name	Description	Acces
0x0200	MPAMCFG_MBW_MIN	MPAM Memory Bandwidth Minimum Partition Configuration Register	RW
0x0208	MPAMCFG_MBW_MAX	MPAM Memory Bandwidth Maximum Partition Configuration Register	RW
0x0220	MPAMCFG_MBW_WINWD	MPAM Memory Bandwidth Partitioning Window Width Configuration Register	RW
0x0300	MPAMCFG_EN	MPAM Partition Configuration Enable Register	WO/ RAZ
0x0310	MPAMCFG_DIS	MPAM Partition Configuration Disable Register	WO/ RAZ
0x0320	MPAMCFG_EN_FLAGS	MPAM Partition Configuration Enable Flags Register	RW
0x0400	MPAMCFG_PRI	MPAM Priority Partition Configuration Register	RW
0x0500	MPAMCFG_MBW_PROP	MPAM Memory Bandwidth Proportional Stride Partition Configuration Register	RW
0x0600	MPAMCFG_INTPARTID	MPAM Internal PARTID Narrowing Configuration Register	RW
0x0800	MSMON_CFG_MON_SEL	MPAM Monitor Instance Selection Register	RW

Offset	Name	Description	Acce
0x0808	MSMON_CAPT_EVNT	MPAM Capture Event Generation Register	WO/ RAZ
0x0810	MSMON_CFG_CSU_FLT	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register	RW
0x0818	MSMON_CFG_CSU_CTL	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register	RW
0x0820	MSMON_CFG_MBWU_FLT	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register	RW
0x0828	MSMON_CFG_MBWU_CTL	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register	RW
0x0840	MSMON_CSU	MPAM Cache Storage Usage Monitor Register	RW
0x0848	MSMON_CSU_CAPTURE	MPAM Cache Storage Usage Monitor Capture Register	RW
0x0858	MSMON_CSU_OFSR	MPAM CSU Monitor Overflow Status Register	RO
0x0860	MSMON_MBWU	MPAM Memory Bandwidth Usage Monitor Register	RW

Offset	Name	Description	Acce
0x0868	MSMON_MBWU_CAPTURE	MPAM Memory Bandwidth Usage Monitor Capture Register	RW
0x0880	MSMON_MBWU_L	MPAM Long Memory Bandwidth Usage Monitor Register	RW
0x0890	MSMON_MBWU_L_CAPTURE	MPAM Long Memory Bandwidth Usage Monitor Capture Register	RW
0x0898	MSMON_MBWU_OFSR	MPAM MBWU Monitor Overflow Status Register	RO
0x08DC	MSMON_OFLOW_MSI_MPAM	MPAM Monitor Overflow MSI Write MPAM Information Register	RW
0x08E0	MSMON_OFLOW_MSI_ADDR_L	MPAM Monitor Overflow MSI Low-part Address Register	RW
0x08E4	MSMON_OFLOW_MSI_ADDR_H	MPAM Monitor Overflow MSI Write High-part Address Register	RW
0x08E8	MSMON_OFLOW_MSI_DATA	MPAM Monitor Overflow MSI Write Data Register	RW
0x08EC	MSMON_OFLOW_MSI_ATTR	MPAM Monitor Overflow MSI Write Attributes Register	RW
0x08F0	MSMON_OFLOW_SR	MPAM Monitor Overflow Status Register	RO

Offset	Name	Description	Acces
0x1000 + (4 * n)	MPAMCFG_CPBM<n>	MPAM Cache Portion Bitmap Partition Configuration Register	RW
0x2000 + (4 * n)	MPAMCFG_MBW_PBM<n>	MPAM Bandwidth Portion Bitmap Partition Configuration Register	RW

In the MPAMF_BASE_rt block:

Offset	Name	Description	Acces
0x0000	MPAMF_IDR	MPAM Features Identification Register	RO
0x0018	MPAMF_IIDR	MPAM Implementation Identification Register	RO
0x0020	MPAMF_AIDR	MPAM Architecture Identification Register	RO
0x0028	MPAMF_IMPL_IDR	MPAM Implementation-Specific Partitioning Feature Identification Register	RO
0x0030	MPAMF_CPOR_IDR	MPAM Features Cache Portion Partitioning ID register	RO
0x0038	MPAMF_CCAP_IDR	MPAM Features Cache Capacity Partitioning ID register	RO
0x0040	MPAMF_MBW_IDR	MPAM Memory Bandwidth Partitioning Identification Register	RO

Offset	Name	Description	Acce
0x0048	MPAMF_PRI_IDR	MPAM Priority Partitioning Identification Register	RO
0x0050	MPAMF_PARTID_NRW_IDR	MPAM PARTID Narrowing ID register	RO
0x0080	MPAMF_MSMON_IDR	MPAM Resource Monitoring Identification Register	RO
0x0088	MPAMF_CSUMON_IDR	MPAM Features Cache Storage Usage Monitoring ID register	RO
0x0090	MPAMF_MBWUMON_IDR	MPAM Features Memory Bandwidth Usage Monitoring ID register	RO
0x00DC	MPAMF_ERR_MSI_MPAM	MPAM Error MSI Write MPAM Information Register	RW
0x00E0	MPAMF_ERR_MSI_ADDR_L	MPAM Error MSI Low-part Address Register	RW
0x00E4	MPAMF_ERR_MSI_ADDR_H	MPAM Error MSI High-part Address Register	RW
0x00E8	MPAMF_ERR_MSI_DATA	MPAM Error MSI Data Register	RW
0x00EC	MPAMF_ERR_MSI_ATTR	MPAM Error MSI Write Attributes Register	RW
0x00F0	MPAMF_ECR	MPAM Error Control Register	RW
0x00F8	MPAMF_ESR	MPAM Error Status Register	RW

Offset	Name	Description	Acce
0x0100	MPAMCFG_PART_SEL	MPAM Partition Configuration Selection Register	RW
0x0108	MPAMCFG_CMAX	MPAM Cache Maximum Capacity Partition Configuration Register	RW
0x0110	MPAMCFG_CMIN	MPAM Cache Minimum Capacity Partition Configuration Register	RW
0x0118	MPAMCFG_CASSOC	MPAM Cache Maximum Associativity Partition Configuration Register	RW
0x0200	MPAMCFG_MBW_MIN	MPAM Memory Bandwidth Minimum Partition Configuration Register	RW
0x0208	MPAMCFG_MBW_MAX	MPAM Memory Bandwidth Maximum Partition Configuration Register	RW
0x0220	MPAMCFG_MBW_WINWD	MPAM Memory Bandwidth Partitioning Window Width Configuration Register	RW
0x0300	MPAMCFG_EN	MPAM Partition Configuration Enable Register	WO/ RAZ
0x0310	MPAMCFG_DIS	MPAM Partition Configuration Disable Register	WO/ RAZ

Offset	Name	Description	Acces
0x0320	MPAMCFG_EN_FLAGS	MPAM Partition Configuration Enable Flags Register	RW
0x0400	MPAMCFG_PRI	MPAM Priority Partition Configuration Register	RW
0x0500	MPAMCFG_MBW_PROP	MPAM Memory Bandwidth Proportional Stride Partition Configuration Register	RW
0x0600	MPAMCFG_INTPARTID	MPAM Internal PARTID Narrowing Configuration Register	RW
0x0800	MSMON_CFG_MON_SEL	MPAM Monitor Instance Selection Register	RW
0x0808	MSMON_CAPT_EVNT	MPAM Capture Event Generation Register	WO/ RAZ
0x0810	MSMON_CFG_CSU_FLT	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register	RW
0x0818	MSMON_CFG_CSU_CTL	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register	RW
0x0820	MSMON_CFG_MBWU_FLT	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register	RW

Offset	Name	Description	Acce
0x0828	MSMON_CFG_MBWU_CTL	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register	RW
0x0840	MSMON_CSU	MPAM Cache Storage Usage Monitor Register	RW
0x0848	MSMON_CSU_CAPTURE	MPAM Cache Storage Usage Monitor Capture Register	RW
0x0858	MSMON_CSU_OFSR	MPAM CSU Monitor Overflow Status Register	RO
0x0860	MSMON_MBWU	MPAM Memory Bandwidth Usage Monitor Register	RW
0x0868	MSMON_MBWU_CAPTURE	MPAM Memory Bandwidth Usage Monitor Capture Register	RW
0x0880	MSMON_MBWU_L	MPAM Long Memory Bandwidth Usage Monitor Register	RW
0x0890	MSMON_MBWU_L_CAPTURE	MPAM Long Memory Bandwidth Usage Monitor Capture Register	RW
0x0898	MSMON_MBWU_OFSR	MPAM MBWU Monitor Overflow Status Register	RO

Offset	Name	Description	Acces
0x08DC	MSMON_OFLOW_MSI_MPAM	MPAM Monitor Overflow MSI Write MPAM Information Register	RW
0x08E0	MSMON_OFLOW_MSI_ADDR_L	MPAM Monitor Overflow MSI Low-part Address Register	RW
0x08E4	MSMON_OFLOW_MSI_ADDR_H	MPAM Monitor Overflow MSI Write High-part Address Register	RW
0x08E8	MSMON_OFLOW_MSI_DATA	MPAM Monitor Overflow MSI Write Data Register	RW
0x08EC	MSMON_OFLOW_MSI_ATTR	MPAM Monitor Overflow MSI Write Attributes Register	RW
0x08F0	MSMON_OFLOW_SR	MPAM Monitor Overflow Status Register	RO
0x1000 + (4 * n)	MPAMCFG_CPBM<n>	MPAM Cache Portion Bitmap Partition Configuration Register	RW
0x2000 + (4 * n)	MPAMCFG_MBW_PBM<n>	MPAM Bandwidth Portion Bitmap Partition Configuration Register	RW

In the MPAMF_BASE_s block:

Offset	Name	Description	Acces
0x0000	MPAMF_IDR	MPAM Features Identification Register	RO
0x0008	MPAMF_SIDR	MPAM Features Secure Identification Register	RO

Offset	Name	Description	Acce
0x0018	MPAMF_IIDR	MPAM Implementation Identification Register	RO
0x0020	MPAMF_AIDR	MPAM Architecture Identification Register	RO
0x0028	MPAMF_IMPL_IDR	MPAM Implementation-Specific Partitioning Feature Identification Register	RO
0x0030	MPAMF_CPOR_IDR	MPAM Features Cache Portion Partitioning ID register	RO
0x0038	MPAMF_CCAP_IDR	MPAM Features Cache Capacity Partitioning ID register	RO
0x0040	MPAMF_MBW_IDR	MPAM Memory Bandwidth Partitioning Identification Register	RO
0x0048	MPAMF_PRI_IDR	MPAM Priority Partitioning Identification Register	RO
0x0050	MPAMF_PARTID_NRW_IDR	MPAM PARTID Narrowing ID register	RO
0x0080	MPAMF_MSMON_IDR	MPAM Resource Monitoring Identification Register	RO
0x0088	MPAMF_CSUMON_IDR	MPAM Features Cache Storage Usage Monitoring ID register	RO

Offset	Name	Description	Acces
0x0090	MPAMF_MBWUMON_IDR	MPAM Features Memory Bandwidth Usage Monitoring ID register	RO
0x00DC	MPAMF_ERR_MSI_MPAM	MPAM Error MSI Write MPAM Information Register	RW
0x00E0	MPAMF_ERR_MSI_ADDR_L	MPAM Error MSI Low-part Address Register	RW
0x00E4	MPAMF_ERR_MSI_ADDR_H	MPAM Error MSI High-part Address Register	RW
0x00E8	MPAMF_ERR_MSI_DATA	MPAM Error MSI Data Register	RW
0x00EC	MPAMF_ERR_MSI_ATTR	MPAM Error MSI Write Attributes Register	RW
0x00F0	MPAMF_ECR	MPAM Error Control Register	RW
0x00F8	MPAMF_ESR	MPAM Error Status Register	RW
0x0100	MPAMCFG_PART_SEL	MPAM Partition Configuration Selection Register	RW
0x0108	MPAMCFG_CMAX	MPAM Cache Maximum Capacity Partition Configuration Register	RW
0x0110	MPAMCFG_CMIN	MPAM Cache Minimum Capacity Partition Configuration Register	RW

Offset	Name	Description	Acce
0x0118	MPAMCFG_CASSOC	MPAM Cache Maximum Associativity Partition Configuration Register	RW
0x0200	MPAMCFG_MBW_MIN	MPAM Memory Bandwidth Minimum Partition Configuration Register	RW
0x0208	MPAMCFG_MBW_MAX	MPAM Memory Bandwidth Maximum Partition Configuration Register	RW
0x0220	MPAMCFG_MBW_WINWD	MPAM Memory Bandwidth Partitioning Window Width Configuration Register	RW
0x0300	MPAMCFG_EN	MPAM Partition Configuration Enable Register	WO/ RAZ
0x0310	MPAMCFG_DIS	MPAM Partition Configuration Disable Register	WO/ RAZ
0x0320	MPAMCFG_EN_FLAGS	MPAM Partition Configuration Enable Flags Register	RW
0x0400	MPAMCFG_PRI	MPAM Priority Partition Configuration Register	RW
0x0500	MPAMCFG_MBW_PROP	MPAM Memory Bandwidth Proportional Stride Partition Configuration Register	RW

Offset	Name	Description	Acce
0x0600	MPAMCFG_INTPARTID	MPAM Internal PARTID Narrowing Configuration Register	RW
0x0800	MSMON_CFG_MON_SEL	MPAM Monitor Instance Selection Register	RW
0x0808	MSMON_CAPT_EVNT	MPAM Capture Event Generation Register	WO/ RAZ
0x0810	MSMON_CFG_CSU_FLT	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register	RW
0x0818	MSMON_CFG_CSU_CTL	MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register	RW
0x0820	MSMON_CFG_MBWU_FLT	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register	RW
0x0828	MSMON_CFG_MBWU_CTL	MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register	RW
0x0840	MSMON_CSU	MPAM Cache Storage Usage Monitor Register	RW

Offset	Name	Description	Acce
0x0848	MSMON_CSU_CAPTURE	MPAM Cache Storage Usage Monitor Capture Register	RW
0x0858	MSMON_CSU_OFSR	MPAM CSU Monitor Overflow Status Register	RO
0x0860	MSMON_MBWU	MPAM Memory Bandwidth Usage Monitor Register	RW
0x0868	MSMON_MBWU_CAPTURE	MPAM Memory Bandwidth Usage Monitor Capture Register	RW
0x0880	MSMON_MBWU_L	MPAM Long Memory Bandwidth Usage Monitor Register	RW
0x0890	MSMON_MBWU_L_CAPTURE	MPAM Long Memory Bandwidth Usage Monitor Capture Register	RW
0x0898	MSMON_MBWU_OFSR	MPAM MBWU Monitor Overflow Status Register	RO
0x08DC	MSMON_OFLOW_MSI_MPAM	MPAM Monitor Overflow MSI Write MPAM Information Register	RW
0x08E0	MSMON_OFLOW_MSI_ADDR_L	MPAM Monitor Overflow MSI Low-part Address Register	RW
0x08E4	MSMON_OFLOW_MSI_ADDR_H	MPAM Monitor Overflow MSI Write High-part Address Register	RW

Offset	Name	Description	Acce
0x08E8	MSMON_OFLOW_MSI_DATA	MPAM Monitor Overflow MSI Write Data Register	RW
0x08EC	MSMON_OFLOW_MSI_ATTR	MPAM Monitor Overflow MSI Write Attributes Register	RW
0x08F0	MSMON_OFLOW_SR	MPAM Monitor Overflow Status Register	RO
0x1000 + (4 * n)	MPAMCFG_CPBM<n>	MPAM Cache Portion Bitmap Partition Configuration Register	RW
0x2000 + (4 * n)	MPAMCFG_MBW_PBM<n>	MPAM Bandwidth Portion Bitmap Partition Configuration Register	RW

In the PMU block:

Offset	Name	Descripti
0x000 + (8 * n) for n in 30:0	PMEVCNTR<n>_EL0	Performance Monitors Eve Count Regist
0x000 + (8 * n) for n in 30:0	PMEVCNTR<n>_EL0	Performance Monitors Eve Count Regist
0x000 + (8 * n) for n in 30:0	PMEVCNTR<n>_EL0	Performance Monitors Eve Count Regist
0x0F8	PMCCNTR_EL0	Performance Monitors Cyc Counter
0x0F8	PMCCNTR_EL0	Performance Monitors Cyc Counter
0x0FC	PMCCNTR_EL0[63:32]	Performance Monitors Cyc Counter

Offset	Name	Descripti
0x100	PMICNTR_EL0	Performance Monitors Instruction Counter Regi
0x200	PMPCSR	Program Cou Sample Regis
0x200	PMPCSR	Program Cou Sample Regis
0x204	PMPCSR[63:32]	Program Cou Sample Regis
0x208	PMVCIDSR	CONTEXTIDI and VMID Sa Register
0x208	PMCID1SR	CONTEXTIDI Sample Regis
0x20C	PMVIDSR	VMID Sample Register
0x220	PMPCSR	Program Cou Sample Regis
0x220	PMPCSR	Program Cou Sample Regis

Offset	Name	Descripti
0x224	PMPCSR[63:32]	Program Cou Sample Regis
0x228	PMCCIDSR	CONTEXTIDI Sample Regis
0x228	PMCID1SR	CONTEXTIDI Sample Regis
0x22C	PMCID2SR	CONTEXTIDI Sample Regis
0x230	PMPCSCTL	PC Sample-ba Profiling Con Register
0x400 + (8 * n) for n in 30:0	PMEVTYPER<n>_EL0[63:0]	Performance Monitors Eve Type Registe
0x400 + (4 * n) for n in 30:0	PMEVTYPER<n>_EL0[31:0]	Performance Monitors Eve Type Registe
0x47C	PMCCFILTR_EL0[31:0]	Performance Monitors Cyc Counter Filte Register
0x480	PMICFILTR_EL0[31:0]	Performance Monitors Instruction Counter Filte Register
0x4F8	PMCCFILTR_EL0	Performance Monitors Cyc Counter Filte Register
0x500	PMICFILTR_EL0	Performance Monitors Instruction Counter Filte Register
0x600 + (8 * n) for n in 30:0	PMEVCNTSVR<n>_EL1	Performance Monitors Eve Count Saved Register <n>

Offset	Name	Descripti
0x6F8	PMCCNTSVR_EL1	Performance Monitors Cyc Count Saved Register
0x700	PMICNTSVR_EL1	Performance Monitors Instruction C Saved Value Register
0x800 + (4 * n) for n in 63:0	PMEVFILT2R<n>[31:0]	Performance Monitors Eve Filter Registe
0x800 + (8 * n) for n in 63:0	PMEVFILT2R<n>[63:0]	Performance Monitors Eve Filter Registe
0xA00 + (4 * n) for n in 30:0	PMEVTYPER<n>_EL0[63:32]	Performance Monitors Eve Type Registe
0xA7C	PMCCFILTR_EL0[63:32]	Performance Monitors Cyc Counter Filte Register
0xA80	PMICFILTR_EL0[63:32]	Performance Monitors Instruction Counter Filte Register
0xC00	PMCNTENSET_EL0	Performance Monitors Cou Enable Set Register

Offset	Name	Descripti
0xC00	PMCNTENSET_EL0	Performance Monitors Cou Enable Set Register
0xC10	PMCNTEN	Performance Monitors Cou Enable regist
0xC20	PMCNTENCLR_EL0	Performance Monitors Cou Enable Clear Register
0xC20	PMCNTENCLR_EL0	Performance Monitors Cou Enable Clear Register
0xC40	PMINTENSET_EL1	Performance Monitors Inte Enable Set Register
0xC40	PMINTENSET_EL1	Performance Monitors Inte Enable Set Register
0xC50	PMINTEN	Performance Monitors Inte Enable regist
0xC60	PMINTENCLR_EL1	Performance Monitors Inte Enable Clear Register

Offset	Name	Descripti
0xC60	PMINTENCLR_EL1	Performance Monitors Inte Enable Clear Register
0xC80	PMOVSCLR_EL0	Performance Monitors Ove Flag Status C register
0xC80	PMOVSCLR_EL0	Performance Monitors Ove Flag Status C register
0xC90	PMOVS	Performance Monitors Ove Flag Status register
0xCA0	PMSWINC_EL0	Performance Monitors Soft Increment Register
0xCA0	PMZR_EL0	Performance Monitors Zer with Mask
0xCC0	PMOVSSET_EL0	Performance Monitors Ove Flag Status S Register

Offset	Name	Descripti
0xCC0	PMOVSSET_EL0	Performance Monitors Ove Flag Status S Register
0xCE0	PMCGCR0	Counter Grou Configuration Register 0
0xE00	PMCFGR	Performance Monitors Configuration Register
0xE00	PMCFGR	Performance Monitors Configuration Register
0xE04	PMCR_EL0	Performance Monitors Con Register
0xE08	PMIIDR	Performance Monitors Implementati Identification Register
0xE10	PMCR_EL0	Performance Monitors Con Register
0xE20	PMCEID0	Performance Monitors Con Event Identification register 0
0xE24	PMCEID1	Performance Monitors Con Event Identification register 1
0xE28	PMCEID2	Performance Monitors Con Event Identification register 2

Offset	Name	Descripti
0xE2C	PMCEID3	Performance Monitors Con Event Identification register 3
0xE30	PMSSCR_EL1	Performance Monitors Sna Status and Capture Regi
0xE40	PMMIR	Performance Monitors Mac Identification Register
0xE40	PMMIR	Performance Monitors Mac Identification Register
0xF00	PMITCTRL	Performance Monitors Integration m Control regis
0xFA8	PMDEVAFF	Performance Monitors Dev Affinity regist
0xFA8	PMDEVAFF0	Performance Monitors Dev Affinity regist
0xFAC	PMDEVAFF1	Performance Monitors Dev Affinity regist
0xFB0	PMLAR	Performance Monitors Loc Access Regist
0xFB4	PMLSR	Performance Monitors Loc Status Regist
0xFB8	PMAUTHSTATUS	Performance Monitors Authenticatio Status registe
0xFBC	PMDEVARCH	Performance Monitors Dev Architecture register

Offset	Name	Descripti
0xFC8	PMDEVID	Performance Monitors Dev ID register
0xFCC	PMDEVTYPE	Performance Monitors Dev Type register
0xFD0	PMPIDR4	Performance Monitors Peripheral Identification Register 4
0xFE0	PMPIDR0	Performance Monitors Peripheral Identification Register 0
0xFE4	PMPIDR1	Performance Monitors Peripheral Identification Register 1
0xFE8	PMPIDR2	Performance Monitors Peripheral Identification Register 2
0xFEC	PMPIDR3	Performance Monitors Peripheral Identification Register 3
0xFF0	PMCIDR0	Performance Monitors Component Identification Register 0
0xFF4	PMCIDR1	Performance Monitors Component Identification Register 1

Offset	Name	Descripti
0xFF8	PMCIDR2	Performance Monitors Component Identification Register 2
0xFFC	PMCIDR3	Performance Monitors Component Identification Register 3

In the RAS block:

Offset	Name	Description	Access	
0x000 + (64 * n)	ERR<n>FR	Error Record <n> Feature Register	RO	-
0x008 + (64 * n)	ERR<n>CTLR	Error Record <n> Control Register	RW	-
0x010 + (64 * n)	ERR<n>STATUS	Error Record <n> Primary Status Register	RW	-
0x018 + (64 * n)	ERR<n>ADDR	Error Record <n> Address Register	RW	-
0x020 + (64 * n)	ERR<n>MISC0	Error Record <n> Miscellaneous Register 0	RW	-
0x028 + (64 * n)	ERR<n>MISC1	Error Record <n> Miscellaneous Register 1	RW	-
0x030 + (64 * n)	ERR<n>MISC2	Error Record <n> Miscellaneous Register 2	RW	-
0x038 + (64 * n)	ERR<n>MISC3	Error Record <n> Miscellaneous Register 3	RW	-
0x800 + (64 * n)	ERR<n>PFGF	Error Record <n> Pseudo-fault Generation Feature Register	RO	-
0x800 + (8 * n)	ERRIMPDEF<n>	IMPLEMENTATION DEFINED Register <n>	RW	-
0x808 + (64 * n)	ERR<n>PFGCTL	Error Record <n> Pseudo-fault Generation Control Register	RW	-

Offset	Name	Description	Access	
0x810 + (64 * n)	ERR<n>PFGCDN	Error Record <n> Pseudo-fault Generation Countdown Register	RW	-
0xE00	ERRGSR	Error Group Status Register	RO	-
0xE10	ERRIIDR	Implementation Identification Register	RO	-
0xE40	ERRACR	Access Configuration Register	RW	-
0xE80	ERRFHICR0	Fault Handling Interrupt Configuration Register 0	RW	-
0xE80 + (8 * n)	ERRIRQCR<n>	Generic Error Interrupt Configuration Register <n>	RW	-
0xE88	ERRFHICR1	Fault Handling Interrupt Configuration Register 1	RW	-
0xE8C	ERRFHICR2	Fault Handling Interrupt Configuration Register 2	RW	-
0xE90	ERRERICR0	Error Recovery Interrupt Configuration Register 0	RW	-
0xE98	ERRERICR1	Error Recovery Interrupt Configuration Register 1	RW	-
0xE9C	ERRERICR2	Error Recovery Interrupt Configuration Register 2	RW	-
0xEA0	ERRCRICR0	Critical Error Interrupt Configuration Register 0	RW	-

Offset	Name	Description	Access	
0xEA8	ERRCRICR1	Critical Error Interrupt Configuration Register 1	RW	-
0xEAC	ERRCRICR2	Critical Error Interrupt Configuration Register 2	RW	-
0xEF8	ERRIRQSR	Error Interrupt Status Register	RW	-
0xFA8	ERRDEVAFF	Device Affinity Register	RO	-
0xFBC	ERRDEVARCH	Device Architecture Register	RO	-
0xFC8	ERRDEVID	Device Configuration Register	RO	-
0xFD0	ERRPIDR4	Peripheral Identification Register 4	RO	-
0xFE0	ERRPIDR0	Peripheral Identification Register 0	RO	-
0xFE4	ERRPIDR1	Peripheral Identification Register 1	RO	-
0xFE8	ERRPIDR2	Peripheral Identification Register 2	RO	-
0xFEC	ERRPIDR3	Peripheral Identification Register 3	RO	-
0xFF0	ERRCIDR0	Component Identification Register 0	RO	-
0xFF4	ERRCIDR1	Component Identification Register 1	RO	-
0xFF8	ERRCIDR2	Component Identification Register 2	RO	-
0xFFC	ERRCIDR3	Component Identification Register 3	RO	-

In the TRBE block:

Offset	Name	Description	Access	
0x000	TRBBASER_EL1	Trace Buffer Base Address Register	RW	-
0x008	TRBPTR_EL1	Trace Buffer Write Pointer Register	RW	-
0x010	TRBLIMITR_EL1	Trace Buffer Limit Address Register	RW	-
0x018	TRBSR_EL1	Trace Buffer Status/ syndrome Register	RW	-
0x020	TRBTRG_EL1	Trace Buffer Trigger Counter Register	RW	-
0x028	TRBMAR_EL1	Trace Buffer Memory Attribute Register	RW	-
0x030	TRBIDR_EL1	Trace Buffer ID Register	RO	-
0x038	TRBCR	Trace Buffer Control Register	RW	-
0x040	TRBMPAM_EL1	Trace Buffer MPAM Configuration Register	RW	-
0xF00	TRBITCTRL	Integration Mode Control Register	RW	-
0xFA8	TRBDEVAFF	Device Affinity Register	RO	-
0xFB0	TRBLAR	Lock Access Register	WO	-
0xFB4	TRBLSR	Lock Status Register	RO	-
0xFB8	TRBAUTHSTATUS	Authentication Status Register	RO	-
0xFBC	TRBDEVARCH	Trace Buffer Device Architecture Register	RO	-
0xFC0	TRBDEVID2	Device Configuration Register 2	RO	-
0xFC4	TRBDEVID1	Device Configuration Register 1	RO	-
0xFC8	TRBDEVID	Device Configuration Register	RO	-
0xFCC	TRBDEVTYPE	Device Type Register	RO	-
0xFD0	TRBPIDR4	Peripheral Identification Register 4	RO	-
0xFD4	TRBPIDR5	Peripheral Identification Register 5	RO	-
0xFD8	TRBPIDR6	Peripheral Identification Register 6	RO	-

Offset	Name	Description	Access	
0xFDC	TRBPIDR7	Peripheral Identification Register 7	RO	-
0xFE0	TRBPIDR0	Peripheral Identification Register 0	RO	-
0xFE4	TRBPIDR1	Peripheral Identification Register 1	RO	-
0xFE8	TRBPIDR2	Peripheral Identification Register 2	RO	-
0xFEC	TRBPIDR3	Peripheral Identification Register 3	RO	-
0xFF0	TRBCIDR0	Component Identification Register 0	RO	-
0xFF4	TRBCIDR1	Component Identification Register 1	RO	-
0xFF8	TRBCIDR2	Component Identification Register 2	RO	-
0xFFC	TRBCIDR3	Component Identification Register 3	RO	-

In the Timer block:

In the CNTBaseN block:

Offset	Name	Description	Access
0x000	CNTPCT[31:0]	Counter-timer Physical Count	RO
0x004	CNTPCT[63:32]	Counter-timer Physical Count	RO
0x008	CNTVCT[31:0]	Counter-timer Virtual Count	RO
0x00C	CNTVCT[63:32]	Counter-timer Virtual Count	RO
0x010	CNTFRQ	Counter-timer Frequency	RO
0x014	CNTEL0ACR	Counter-timer EL0 Access Control Register	RW

Offset	Name	Description	Access
0x018	CNTVOFF[31:0]	Counter-timer Virtual Offset	RO
0x01C	CNTVOFF[63:32]	Counter-timer Virtual Offset	RO
0x020	CNTP_CVAL[31:0]	Counter-timer Physical Timer CompareValue	RW
0x024	CNTP_CVAL[63:32]	Counter-timer Physical Timer CompareValue	RW
0x028	CNTP_TVAL	Counter-timer Physical Timer TimerValue	RW
0x02C	CNTP_CTL	Counter-timer Physical Timer Control	RW
0x030	CNTV_CVAL[31:0]	Counter-timer Virtual Timer CompareValue	RW
0x034	CNTV_CVAL[63:32]	Counter-timer Virtual Timer CompareValue	RW
0x038	CNTV_TVAL	Counter-timer Virtual Timer TimerValue	RW
0x03C	CNTV_CTL	Counter-timer Virtual Timer Control	RW
0xFD0 + (4 * n)	CounterID<n>	Counter ID registers	RO

In the CNTCTLBase block:

Offset	Name	Description	Access
0x000	CNTFRQ	Counter-timer Frequency	RO
0x004	CNTNSAR	Counter-timer Non-secure Access Register	RW
0x008	CNTTIDR	Counter-timer Timer ID Register	RO

Offset	Name	Description	Access
0x040 + (4 * n)	CNTACR<n>	Counter-timer Access Control Registers	RW
0x080 + (8 * n)	CNTVOFF<n>[31:0]	Counter-timer Virtual Offsets	RW
0x084 + (8 * n)	CNTVOFF<n>[63:32]	Counter-timer Virtual Offsets	RW
0xFD0 + (4 * n)	CounterID<n>	Counter ID registers	RO

In the CNTControlBase block:

Offset	Name	Description	Access
0x000	CNTCR	Counter Control Register	RW
0x004	CNTSR	Counter Status Register	RO
0x008	CNTCV[63:0]	Counter Count Value register	RW
0x020	CNTFID0	Counter Frequency ID	ImplementationDefined:RO
0x020 + (4 * n)	CNTFID<n>	Counter Frequency IDs, n > 0	ImplementationDefined:RO
0x10	CNTSCR	Counter Scale Register	RW
0x1C	CNTID	Counter Identification Register	RO
0xFD0 + (4 * n)	CounterID<n>	Counter ID registers	RO

In the CNTEL0BaseN block:

Offset	Name	Description	Access
0x000	CNTPCT[31:0]	Counter-timer Physical Count	RO
0x004	CNTPCT[63:32]	Counter-timer Physical Count	RO

Offset	Name	Description	Access
0x008	CNTVCT[31:0]	Counter-timer Virtual Count	RO
0x00C	CNTVCT[63:32]	Counter-timer Virtual Count	RO
0x010	CNTFRQ	Counter-timer Frequency	RO
0x020	CNTP_CVAL[31:0]	Counter-timer Physical Timer CompareValue	RW
0x024	CNTP_CVAL[63:32]	Counter-timer Physical Timer CompareValue	RW
0x028	CNTP_TVAL	Counter-timer Physical Timer TimerValue	RW
0x02C	CNTP_CTL	Counter-timer Physical Timer Control	RW
0x030	CNTV_CVAL[31:0]	Counter-timer Virtual Timer CompareValue	RW
0x034	CNTV_CVAL[63:32]	Counter-timer Virtual Timer CompareValue	RW
0x038	CNTV_TVAL	Counter-timer Virtual Timer TimerValue	RW
0x03C	CNTV_CTL	Counter-timer Virtual Timer Control	RW
0xFD0 + (4 * n)	CounterID<n>	Counter ID registers	RO

In the CNTReadBase block:

Offset	Name	Description	Access
0x000	CNTCV[63:0]	Counter Count Value register	RO
0xFD0 + (4 * n)	CounterID<n>	Counter ID registers	RO

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