ID_AA64DFR1_EL1, AArch64 Debug Feature Register 1

The ID_AA64DFR1_EL1 characteristics are:

Purpose

Provides top level information about the debug system in AArch64.

Configuration

There are no configuration notes.

Attributes

ID_AA64DFR1_EL1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ABL_CMPs								RES0				EBEP				ITE				ABLE				PMICNTR				SPMU			
CTX_CMPs								WRPs								BRPs								SYSPMUID							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ABL_CMPs, bits [63:56]
When FEAT_ABLE is implemented:

Number of breakpoints that support address linking, minus 1.

The values `0x40` to `0xFF` are reserved.

The value of this field is never greater than either ID_AA64DFR1_EL1.WRPs or ID_AA64DFR1_EL1.BRPs.

Otherwise:

Reserved, res0.

Bits [55:52]

Reserved, res0.

EBEP, bits [51:48]

Exception-based event profiling. Defined values are:

EBEP	Meaning
0b0000	Exception-based event profiling not implemented.
0b0001	Exception-based event profiling implemented.

All other values are reserved.

FEAT_EBEP implements the functionality identified by the value 0b0001.

ITE, bits [47:44]

Instrumentation Trace Extension. Defined values are:

ITE	Meaning
0b0000	Instrumentation Trace Extension not implemented.
0b0001	Instrumentation Trace Extension implemented.

All other values are reserved.

FEAT_ITE implements the functionality identified by the value 0b0001.

ABLE, bits [43:40]

Address Breakpoint Linking Extension. Defined values are:

ABLE	Meaning
0b0000	Address Breakpoint Linking Extension not implemented.
0b0001	Address Breakpoint Linking Extension implemented.

All other values are reserved.

FEAT_ABLE implements the functionality identified by the value 0b0001.

PMICNTR, bits [39:36]

PMU fixed-function instruction counter. Defined values are:

PMICNTR	Meaning
0b0000	PMU fixed-function instruction counter not implemented.

0b0001	PMU fixed-function instruction counter implemented.

All other values are reserved.

FEAT_PMUv3_ICNTR implements the functionality identified by the value 0b0001.

If FEAT_PMUv3 is not implemented, then the only permitted value is 0b0000.

SPMU, bits [35:32]

System PMU extension. Defined values are:

SPMU	Meaning
0b0000	System PMU extension not implemented.
0b0001	System PMU extension implemented.

All other values are reserved.

FEAT_SPMU implements the functionality identified by the value 0b0001.

CTX_CMPs, bits [31:24]
When FEAT_Debugv8p9 is implemented and ID_AA64DFR0_EL1.CTX_CMPs == 0b1111:

Number of breakpoints that are context-aware, minus 1.

The value 0x00 means 16 breakpoints that are context-aware are implemented. Otherwise, this field is the number of breakpoints that are context-aware, minus 1.

The values 0x01 to 0x0F and 0x40 to 0xFF are reserved.

The value of this field is never greater than ID_AA64DFR1_EL1.BRPs.

Otherwise:

Reserved, res0.

WRPs, bits [23:16]
When FEAT_Debugv8p9 is implemented and ID_AA64DFR0_EL1.WRPs == 0b1111:

Number of watchpoints, minus 1.

The value `0x00` means 16 watchpoints are implemented. Otherwise, this field is the number of watchpoints, minus 1.

The values `0x01` to `0x0F` and `0x40` to `0xFF` are reserved.

Otherwise:

Reserved, res0.

BRPs, bits [15:8]
When FEAT_Debugv8p9 is implemented and ID_AA64DFR0_EL1.BRPs == 0b1111:

Number of breakpoints, minus 1.

The value `0x00` means 16 breakpoints are implemented. Otherwise, this field is the number of breakpoints, minus 1.

The values `0x01` to `0x0F` and `0x40` to `0xFF` are reserved.

Otherwise:

Reserved, res0.

SYSPMUID, bits [7:0]
When FEAT_SPMU is implemented:

System PMU ID. Indicates the largest value that can be written to SPMSELR_EL0.SYSPMUSEL. Defined values are:

SYSPMUID	Meaning
`0x00..0x1F`	The largest supported value that can be written to SPMSELR_EL0.SYSPMUSEL.

All other values are reserved.

Since System PMUs might not be contiguously accessible, this field does not necessarily indicate the total number of accessible System PMUs.

Otherwise:

Reserved, res0.

Accessing ID_AA64DFR1_EL1

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, ID_AA64DFR1_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0101	0b001

```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AA64DFR1_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64DFR1_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64DFR1_EL1;
```

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