TRBPIDR3, Peripheral Identification Register 3

The TRBPIDR3 characteristics are:

Purpose

Provides discovery information about the component.

For additional information, see the CoreSight Architecture Specification.

Configuration

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBPIDR3 are res0.

TRBPIDR3 is in the Core power domain.

Attributes

TRBPIDR3 is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
RES0	REVAND	CMOD

Bits [31:8]

Reserved, res0.

REVAND, bits [7:4]

Component minor revision. TRBPIDR2.REVISION and TRBPIDR3.REVAND together form the revision number of the component, with TRBPIDR2.REVISION being the most significant part and TRBPIDR3.REVAND the least significant part. When a component is changed, TRBPIDR2.REVISION or TRBPIDR3.REVAND are increased to ensure that software can differentiate the different revisions of the component. TRBPIDR3.REVAND should be set to `0b0000` when TRBPIDR2.REVISION is increased.

This field has an implementation defined value.

Access to this field is **RO**.

CMOD, bits [3:0]

Customer Modified.

Indicates the component has been modified.

A value of `0b0000` means the component is not modified from the original design.

Any other value means the component has been modified in an implementation defined way.

For any two components with the same Unique Component Identifier:

- If TRBPIDR3.CMOD is zero in both components, then the components are identical.
- If TRBPIDR3.CMOD has the same nonzero value in both components, then this does not necessarily mean that they have the same modifications.
- If TRBPIDR3.CMOD is nonzero in either component, the two components might not be identical despite having the same Unique Component Identifier.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing TRBPIDR3

TRBPIDR3 can be accessed through the external debug interface:

Component	Offset	Instance
TRBE	`0xFEC`	TRBPIDR3

This interface is accessible as follows:

- When DoubleLockStatus() or !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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