ST3B (scalar plus scalar)

Contiguous store three-byte structures from three vectors (scalar index)

Contiguous store three-byte structures, each from the same element number in three vector registers to the memory address generated by a 64-bit scalar base and a 64-bit scalar index register and added to the base address. After each structure access the index value is incremented by three. The index register is not updated by the instruction.

Each predicate element applies to the same element number in each of the three vector registers, or equivalently to the three consecutive bytes in memory which make up each structure. Inactive structures are not written to memory.

31 30 29 28 27 26 25	24	23	22 21	20 19 18 17 16	15 14 13	12 11 10	9 8 7 6 5	4 3 2 1 0
1 1 1 0 0 1 0	0	0	1 0	Rm	0 1 1	Pg	Rn	Zt
	msz<1>	msz<0>						

ST3B { <Zt1>.B, <Zt2>.B, <Zt3>.B }, <Pg>, [<Xn|SP>, <Xm>]

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if Rm == '11111' then UNDEFINED;
integer t = UInt(Zt);
integer n = UInt(Rn);
integer m = UInt(Rm);
integer g = UInt(Pg);
constant integer esize = 8;
constant integer nreg = 3;
```

Assembler Symbols

<Zt1>   Is the name of the first scalable vector register to be transferred, encoded in the "Zt" field.

<Zt2>   Is the name of the second scalable vector register to be transferred, encoded as "Zt" plus 1 modulo 32.

<Zt3>   Is the name of the third scalable vector register to be transferred, encoded as "Zt" plus 2 modulo 32.

<Pg>   Is the name of the governing scalable predicate register P0-P7, encoded in the "Pg" field.

<Xn|SP> Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field.

<Xm>   Is the 64-bit name of the general-purpose offset register, encoded in the "Rm" field.

Operation

```
    CheckSVEEnabled();
    constant integer VL = CurrentVL;
    constant integer PL = VL DIV 8;
    constant integer elements = VL DIV esize;
    bits(64) base;
    bits(PL) mask = P[g, PL];
    bits(64) offset;
    constant integer mbytes = esize DIV 8;
    array [0..2] of bits(VL) values;
    boolean contiguous = TRUE;
    boolean nontemporal = FALSE;
    boolean tagchecked = TRUE;
    AccessDescriptor accdesc = CreateAccDescSVE(MemOp_STORE, nontemporal, c

    if !AnyActiveElement(mask, esize) then
        if n == 31 && ConstrainUnpredictableBool(Unpredictable_CHECKSPNONEA
            CheckSPAlignment();
    else
        if n == 31 then CheckSPAlignment();
        base = if n == 31 then SP[] else X[n, 64];
        offset = X[m, 64];

    for r = 0 to nreg-1
        values[r] = Z[(t+r) MOD 32, VL];

    for e = 0 to elements-1
        for r = 0 to nreg-1
            if ActivePredicateElement(mask, e, esize) then
                integer eoff = UInt(offset) + (e * nreg) + r;
                bits(64) addr = base + eoff * mbytes;
                Mem[addr, mbytes, accdesc] = Elem[values[r], e, esize];
```

Operational information

If FEAT_SVE2 is implemented or FEAT_SME is implemented, then if PSTATE.DIT is 1, the timing of this instruction is insensitive to the value of the data being loaded or stored when its governing predicate register contains the same value for each execution.

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56