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External Registers

TRBPTR_EL1, Trace Buffer Write Pointer Register

The TRBPTR EL1 characteristics are:

Purpose

Defines the current write pointer for the trace buffer.

Configuration

External register TRBPTR_EL1 bits [63:0] are architecturally mapped to AArch64 System register TRBPTR_EL1[63:0].

This register is present only when FEAT_TRBE_EXT is implemented. Otherwise, direct accesses to TRBPTR EL1 are res0.

TRBPTR EL1 is in the Core power domain.

Attributes

TRBPTR_EL1 is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

PTR	
PTR	

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PTR, bits [63:0]

Trace Buffer current write pointer address.

Defines the virtual address of the next entry to be written to the trace buffer.

The architecture places restrictions on the values that software can write to the pointer.

Note

As a result of the restrictions an implementation might treat some of PTR[M:0] as res0, where M is defined by TRBIDR EL1.Align.

The reset behavior of this field is:

• On a Cold reset, this field resets to an architecturally unknown value.

Accessing TRBPTR_EL1

The PE might ignore a write to TRBPTR_EL1 if any of the following apply:

- <u>TRBLIMITR_EL1</u>.E == 1 and the Trace Buffer Unit is using Selfhosted mode.
- <u>TRBLIMITR_EL1</u>.XE == 1 and the Trace Buffer Unit is using External mode.

TRBPTR_EL1 can be accessed through the external debug interface:

Component	Offset	Instance
TRBE	0x008	TRBPTR_EL1

This interface is accessible as follows:

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalTraceBufferAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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