EDPIDR1, External Debug Peripheral Identification Register 1

The EDPIDR1 characteristics are:

Purpose

Provides information to identify an external debug component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

When FEAT_DoPD is implemented, EDPIDR1 is in the Core power domain. Otherwise, EDPIDR1 is in the Debug power domain.

Implementation of this register is optional.

This register is required for CoreSight compliance.

Attributes

EDPIDR1 is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
RES0	DES_0	PART_1

Bits [31:8]

Reserved, res0.

DES_0, bits [7:4]

Designer, least significant nibble of JEP106 ID code. For Arm Limited, this field is `0b1011`.

This field has an implementation defined value.

Access to this field is **RO**.

PART_1, bits [3:0]

Part number, most significant nibble.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing EDPIDR1

EDPIDR1 can be accessed through the external debug interface:

Component	Offset	Instance
Debug	0xFE4	EDPIDR1

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered(), accesses to this register are **RO**.
- Otherwise, accesses to this register generate an error response.

28/03/2023 16:01; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94