GCSSTTR

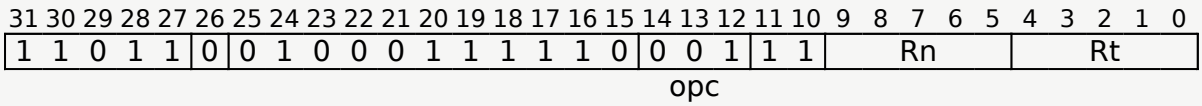
Guarded Control Stack unprivileged Store stores a doubleword from a register to memory. The address that is used for the store is calculated from a base register.

Memory accesses made by the instruction behave as if the instruction was executed at EL0 if the *Effective value* of PSTATE.UAO is 0 and either:

- The instruction is executed at EL1 and *HCR_EL2*.{NV, NV1} is not {1, 1}.
- The instruction is executed at EL2 when the *Effective value* of *HCR_EL2*.{E2H, TGE} is {1, 1}.

Otherwise, the memory access operates with the restrictions determined by the Exception level at which the instruction is executed.

Integer
(FEAT_GCS)




```
GCSSTTR <Xt>, [<Xn|SP>]
```

```
if !IsFeatureImplemented(FEAT_GCS) then UNDEFINED;
integer n = UInt(Rn);
integer t = UInt(Rt);
```

Assembler Symbols

<Xt>	Is the 64-bit name of the general-purpose register to be transferred, encoded in the "Rt" field.
<Xn|SP>	Is the 64-bit name of the general-purpose base register or stack pointer, encoded in the "Rn" field.

Operation

```
bits(64) address;
bits(64) data;

bits(2) effective_el = if AArch64.IsUnprivAccessPriv() then PSTATE.EL el

if effective_el == PSTATE.EL then
    CheckGCSSTREnabled();

AccessDescriptor accdesc = CreateAccDescGCS(effective_el, MemOp_STORE);

if n == 31 then
    CheckSPAlignment();
```

```
    address = SP[];
else
    address = X[n, 64];

data = X[t, 64];
Mem[address, 8, accdesc] = data;
```

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56