

# AMDEVARCH, Activity Monitors Device Architecture Register

The AMDEVARCH characteristics are:

## Purpose

Identifies the programmers' model architecture of the AMU component.

## Configuration

It is implementation defined whether AMDEVARCH is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is optional.

This register is present only when FEAT\_AMUv1 is implemented.

## Attributes

AMDEVARCH is a 32-bit register.

## Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARCHITECT											PRESENT	REVISION				ARCHID															

### ARCHITECT, bits [31:21]

Defines the architecture of the component. For AMU, this is Arm Limited.

Bits [31:28] are the JEP106 continuation code, 0x4.

Bits [27:21] are the JEP106 ID code, 0x3B.

Reads as 0b01000111011.

Access to this field is **RO**.

### PRESENT, bit [20]

Indicates that the DEVARCH is present.

Reads as 0b1.

Access to this field is **RO**.

### REVISION, bits [19:16]

Defines the architecture revision. For architectures defined by Arm this is the minor revision.

REVISION	Meaning
0b0000	Architecture revision is AMUv1.

All other values are reserved.

Access to this field is **RO**.

### ARCHID, bits [15:0]

Defines this part to be an AMU component. For architectures defined by Arm this is further subdivided.

For AMU:

- Bits [15:12] are the architecture version, 0x0.
- Bits [11:0] are the architecture part number, 0xA66.

This corresponds to AMU architecture version AMUv1.

Reads as 0x0A66.

Access to this field is **RO**.

## Accessing AMDEVARCH

**AMDEVARCH can be accessed through the memory-mapped interfaces:**

Component	Offset	Instance
AMU	0xFBC	AMDEVARCH

Accesses on this interface are **RO**.

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