# SMIDR_EL1, Streaming Mode Identification Register

The SMIDR_EL1 characteristics are:

## Purpose

Provides additional identification mechanisms for scheduling purposes, for a PE that supports Streaming SVE mode.

## Configuration

This register is present only when FEAT_SME is implemented. Otherwise, direct accesses to SMIDR_EL1 are undefined.

## Attributes

SMIDR_EL1 is a 64-bit register.

## Field descriptions

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Implementer | | | | | | | | Revision | | | | | | | | SMPS | RES0 | | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

### Bits [63:32]

Reserved, res0.

### Implementer, bits [31:24]

The Implementer code. This field must hold an implementer code that has been assigned by Arm. Assigned codes include the following:

| Implementer | Meaning |
|---|---|
| 0x00 | Reserved for software use. |
| 0x41 | Arm Limited. |
| 0x42 | Broadcom Corporation. |
| 0x43 | Cavium Inc. |
| 0x44 | Digital Equipment Corporation. |

| | |
|---|---|
| 0x46 | Fujitsu Ltd. |
| 0x49 | Infineon Technologies AG. |
| 0x4D | Motorola or Freescale Semiconductor Inc. |
| 0x4E | NVIDIA Corporation. |
| 0x50 | Applied Micro Circuits Corporation. |
| 0x51 | Qualcomm Inc. |
| 0x56 | Marvell International Ltd. |
| 0x69 | Intel Corporation. |
| 0xC0 | Ampere Computing. |

Arm can assign codes that are not published in this manual. All values not assigned by Arm are reserved and must not be used.

It is not required that this value is the same as the value of MIDR_EL1.Implementer.

This field has an implementation defined value.

Access to this field is **RO**.

**Revision, bits [23:16]**

Revision number for the Streaming Mode Compute Unit (SMCU).

This field has an implementation defined value.

Access to this field is **RO**.

**SMPS, bit [15]**

Indicates support for Streaming SVE mode execution priority.

| SMPS | Meaning |
|---|---|
| 0b0 | Priority control not supported. |
| 0b1 | Priority control supported. |

**Bits [14:12]**

Reserved, res0.

**Affinity, bits [11:0]**

The SMCU affinity of the accessing PE.

- A value of zero indicates that the PE's implementation of Streaming SVE mode is not shared with other PEs.

- Otherwise, the value identifies which SMCU is associated with this PE. The Affinity value associated with each SMCU is unique within the system as a whole.

## Accessing SMIDR_EL1

Accesses to this register use the following encodings in the System register encoding space:

### MRS <Xt>, SMIDR_EL1

| op0 | op1 | CRn | CRm | op2 |
|---|---|---|---|---|
| 0b11 | 0b001 | 0b0000 | 0b0000 | 0b110 |

```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = SMIDR_EL1;
elsif PSTATE.EL == EL2 then
    X[t, 64] = SMIDR_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = SMIDR_EL1;
```



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