

PM, PMU Exception Mask

The PM characteristics are:

Purpose

Allows access to the PMU exception Mask bit.

Configuration

This register is present only when FEAT_SEBEP is implemented.
Otherwise, direct accesses to PM are undefined.

Attributes

PM is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															PM
RES0																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:33]

Reserved, res0.

PM, bit [32]

PMU Exception Mask.

PM	Meaning
0b0	Does not cause the PMU exception to be masked.
0b1	Causes the PMU exception to be masked.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Bits [31:0]

Reserved, res0.

Accessing PM

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, PM

op0	op1	CRn	CRm	op2
0b11	0b000	0b0100	0b0011	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    X[t, 64] = Zeros(31):PSTATE.PM:Zeros(32);
elsif PSTATE.EL == EL2 then
    X[t, 64] = Zeros(31):PSTATE.PM:Zeros(32);
elsif PSTATE.EL == EL3 then
    X[t, 64] = Zeros(31):PSTATE.PM:Zeros(32);
```

MSR PM, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b0100	0b0011	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    PSTATE.PM = X[t, 64]<32>;
elsif PSTATE.EL == EL2 then
    PSTATE.PM = X[t, 64]<32>;
elsif PSTATE.EL == EL3 then
    PSTATE.PM = X[t, 64]<32>;
```

MSR PM, #<imm>

op0	op1	CRn	CRm	op2
0b00	0b001	0b0100	0b001x	0b000

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

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