

## GICD\_STATUSR, Error Reporting Status Register

The GICD\_STATUSR characteristics are:

### Purpose

Provides software with a mechanism to detect:

- Accesses to reserved locations.
- Writes to read-only locations.
- Reads of write-only locations.

### Configuration

If the GIC implementation supports two Security states this register is Banked to provide Secure and Non-secure copies.

### Attributes

GICD\_STATUSR is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																												WROD	RWOD	WRD	RRD

#### Bits [31:4]

Reserved, res0.

#### WROD, bit [3]

Write to an RO location.

WROD	Meaning
0b0	Normal operation.
0b1	A write to an RO location has been detected.

When a violation is detected, software must write 1 to this register to reset it.

### **RWOD, bit [2]**

Read of a WO location.

<b>RWOD</b>	<b>Meaning</b>
0b0	Normal operation.
0b1	A read of a WO location has been detected.

When a violation is detected, software must write 1 to this register to reset it.

### **WRD, bit [1]**

Write to a reserved location.

<b>WRD</b>	<b>Meaning</b>
0b0	Normal operation.
0b1	A write to a reserved location has been detected.

When a violation is detected, software must write 1 to this register to reset it.

### **RRD, bit [0]**

Read of a reserved location.

<b>RRD</b>	<b>Meaning</b>
0b0	Normal operation.
0b1	A read of a reserved location has been detected.

When a violation is detected, software must write 1 to this register to reset it.

## **Accessing GICD\_STATUSR**

This is an optional register. If the register is not implemented, the location is RAZ/WI.

**GICD\_STATUSR can be accessed through the memory-mapped interfaces:**

<b>Component</b>	<b>Frame</b>	<b>Offset</b>	<b>Instance</b>
GIC Distributor	Dist_base	0x0010	GICD_STATUSR (S)

This interface is accessible as follows:

- When an access is Secure, accesses to this register are **RW**.

- When FEAT\_RME is implemented and an access is Root, accesses to this register are **RW**.

Component	Frame	Offset	Instance
GIC Distributor	Dist_base	0x0010	GICD_STATUSR (NS)

This interface is accessible as follows:

- When an access is Non-secure, accesses to this register are **RW**.
- When FEAT\_RME is implemented and an access is Realm, accesses to this register are **RAZ/WI**.

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