SCTLR2_EL3, System Control Register (EL3)

The SCTLR2_EL3 characteristics are:

Purpose

Provides top level control of the system, including its memory system, at EL3.

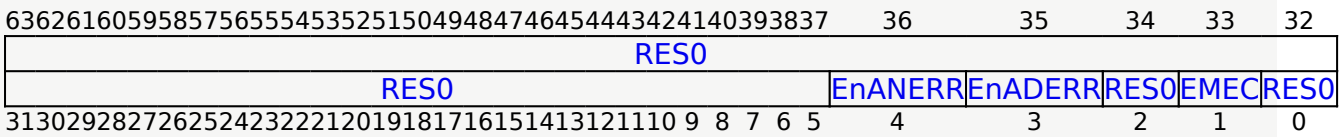
Configuration

This register is present only when FEAT_SCTLR2 is implemented. Otherwise, direct accesses to SCTLR2_EL3 are undefined.

Attributes

SCTLR2_EL3 is a 64-bit register.

Field descriptions



Bits [63:5]

Reserved, res0.

EnANERR, bit [4]
When FEAT_ANERR is implemented:

Enable Asynchronous Normal Read Error.

EnANERR	Meaning
0b0	External abort on Normal memory reads generate synchronous Data Abort exceptions in the EL3 translation regime.
0b1	External abort on Normal memory reads generate synchronous Data Abort or asynchronous SError exceptions in the EL3 translation regime.

It is implementation-specific whether this field applies to memory reads generated by each of the following:

- FP&SIMD register loads.
- SVE register loads.
- SME register loads.
- LD<op>, SWP and CAS{P} Atomic instructions that return a value to the PE.
- ST64BV{0} instructions that return a value to the PE.
- RCW instructions that return a value to the PE.

Setting this field to 0 does not guarantee that the PE is able to take a synchronous Data Abort exception for an External abort on a Normal memory read in every case. There might be implementation-specific circumstances when an error on a load cannot be taken synchronously. These circumstances should be rare enough that treating such occurrences as fatal does not cause a significant increase in failure rate.

Setting this field to 0 might have a performance impact for Normal memory reads.

This field is ignored by the PE and treated as zero when SCR_EL3.SCTLR2En == 0.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

EnADERR, bit [3]
When FEAT_ADERR is implemented:

Enable Asynchronous Device Read Error.

EnADERR	Meaning
0b0	External abort on Device memory reads generate synchronous Data Abort exceptions in the EL3 translation regime.
0b1	External abort on Device memory reads generate synchronous Data Abort or asynchronous SError exceptions in the EL3 translation regime.

It is implementation-specific whether this field applies to memory reads generated by each of the following:

- FP&SIMD register loads.
- SVE register loads.
- SME register loads.
- LD<op>, SWP and CAS{P} Atomic instructions that return a value to the PE.
- ST64BV{0} instructions that return a value to the PE.
- RCW instructions that return a value to the PE.

Setting this field to 0 does not guarantee that the PE is able to take a synchronous Data Abort exception for an External abort on a Device memory read in every case. There might be implementation-specific circumstances when an error on a load cannot be taken synchronously. These circumstances should be rare enough that treating such occurrences as fatal does not cause a significant increase in failure rate.

Setting this field to 0 might have a performance impact for Device memory reads.

This field is ignored by the PE and treated as zero when SCR_EL3.SCTLR2En == 0.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [2]

Reserved, res0.

EMEC, bit [1]
When FEAT_MEC is implemented:

Enables MEC for the Realm physical address space at EL3.

EMEC	Meaning
0b0	MEC is not enabled for the Realm physical address space at EL3.
0b1	MEC is enabled for the Realm physical address space at EL3.

This bit is permitted to be cached in a TLB.

The reset behavior of this field is:

- On a Warm reset, this field resets to `0`.

Otherwise:

Reserved, res0.

Bit [0]

Reserved, res0.

Accessing SCTLR2_EL3

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, SCTLR2_EL3

op0	op1	CRn	CRm	op2
0b11	0b110	0b0001	0b0000	0b011

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] = SCTLR2_EL3;
```

MSR SCTLR2_EL3, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b110	0b0001	0b0000	0b011

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
```

```
    SCTLR2_EL3 = X[t, 64];
```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