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BFMLS (multiple and single vector)

Multi-vector BFloat16 floating-point fused multiply-subtract by vector

Multiply the corresponding BFloat16 floating-point elements of the two or four first source vector with corresponding elements of the second source vector and destructively subtract without intermediate rounding from the corresponding elements of the ZA single-vector groups. The vector numbers forming the single-vector group within each half of or each guarter of the ZA array are selected by the sum of the vector select register and immediate offset, modulo half or quarter the number of ZA array vectors.

The vector group symbol, VGx2 or VGx4, indicates that the ZA operand consists of two or four ZA single-vector groups respectively. The vector group symbol is preferred for disassembly, but optional in assembler source code.

This instruction follows SME2.1 ZA-targeting non-widening BFloat16 numerical behaviors.

This instruction is unpredicated.

ID AA64SMFR0 EL1.B16B16 indicates whether this instruction is implemented.

It has encodings from 2 classes: <u>Two ZA single-vectors</u> and <u>Four ZA single-</u> vectors

Two ZA single-vectors (FEAT SVE B16B16)

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
                                                                 0 1 off3
1 1 0 0 0 0 0 1 0 1 1 0
                               Zm
                                     |0| Rv |1 1 1
                                                         Zn
                                                                   S
```

```
BFMLS ZA.H[<Wv>, <offs>{, VGx2}], { <Zn1>.H-<math><Zn2>.H }, <Zm>.H
```

```
if !<u>HaveSME2</u>() | !IsFeatureImplemented(FEAT_SVE_B16B16) then UNDEFINED
integer v = \underline{UInt}('010':Rv);
integer n = UInt(Zn);
integer m = <u>UInt('0':Zm);</u>
integer offset = <u>UInt</u>(off3);
boolean sub_op = TRUE;
constant integer nreg = 2;
```

Four ZA single-vectors (FEAT SVE B16B16)

```
31\ 30\ 29\ 28\ 27\ 26\ 25\ 24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0
| 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 | 1 | 1 \ 1 |
                                                        0 | Rv | 1
                                                                                   Zn
                                                                                              0 1
                                                                                                       off3
                                              Zm
                               SZ
```

```
BFMLS ZA.H[<Wv>, <offs>{, VGx4}], { <Zn1>.H-<Zn4>.H }, <Zm>.H
if !HaveSME2() | !IsFeatureImplemented(FEAT_SVE_B16B16) then UNDEFINED
integer v = UInt('010':Rv);
integer n = UInt(Zn);
integer m = UInt('0':Zm);
integer offset = UInt(off3);
boolean sub_op = TRUE;
constant integer nreg = 4;
```

Assembler Symbols

<wv></wv>	Is the 32-bit name of the vector select register W8-W11, encoded in the "Rv" field.
<offs></offs>	Is the vector select offset, in the range 0 to 7, encoded in the "off3" field.
<zn1></zn1>	Is the name of the first scalable vector register of a multivector sequence, encoded as "Zn".
<zn4></zn4>	Is the name of the fourth scalable vector register of a multivector sequence, encoded as "Zn" plus 3 modulo 32.
<zn2></zn2>	Is the name of the second scalable vector register of a multi-vector sequence, encoded as "Zn" plus 1 modulo 32.
<zm></zm>	Is the name of the second source scalable vector register Z0-Z15, encoded in the "Zm" field.

Operation

```
CheckStreamingSVEAndZAEnabled();
constant integer VL = CurrentVL;
constant integer elements = VL DIV 16;
integer vectors = VL DIV 8;
integer vstride = vectors DIV nreg;
bits (32) vbase = X[v, 32];
integer vec = (UInt(vbase) + offset) MOD vstride;
bits(VL) result;
for r = 0 to nreg-1
    bits (VL) operand1 = \mathbb{Z}[(n+r)] MOD 32, VL];
    bits(VL) operand2 = \mathbb{Z}[m, VL];
    bits (VL) operand3 = \underline{ZAvector}[vec, VL];
    for e = 0 to elements-1
         bits (16) element 1 = \underline{\text{Elem}} [operand 1, e, 16];
         bits(16) element2 = Elem[operand2, e, 16];
bits(16) element3 = Elem[operand3, e, 16];
         if sub_op then element1 = BFNeg(element1);
         Elem[result, e, 16] = BFMulAdd ZA(element3, element1, element2,
    ZAvector[vec, VL] = result;
    vec = vec + vstride;
```

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