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## ERR<n>MISC2, Error Record <n> Miscellaneous Register 2, n = 0 - 65534

The ERR<n>MISC2 characteristics are:

### Purpose

implementation defined error syndrome register. The miscellaneous syndrome registers might contain:

- Information to locate where the error was detected.
- If the error was detected within a FRU, the identity of the FRU.
- A Corrected error counter or counters.
- Other state information not present in the corresponding status and address registers.

### Configuration

This register is present only when (an implementation implements ERR<n>MISC2 or RAS System Architecture v1.1 is implemented) and error record <n> is implemented. Otherwise, direct accesses to ERR<n>MISC2 are res0.

[ERR<q>FR](#) describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record then q = n.

For implementation defined fields in ERR<n>MISC2, writing zero returns the error record to an initial quiescent state.

In particular, if any implementation defined syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, nonzero, and ignore writes are compliant with this requirement.

Arm recommends that if RAS System Architecture v1.1 is not implemented then ERR<n>MISC2 does not require zeroing to return the record to a quiescent state.

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### Note

Arm recommends that any implementation defined syndrome field that can generate a

Fault Handling, Error Recovery, Critical, or implementation defined, interrupt request is disabled at Cold reset and is enabled by software writing an implementation defined nonzero value to an implementation defined field in [ERR<q>CTRL](#).

## Attributes

ERR<n>MISC2 is a 64-bit register.

## Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
IMPLEMENTATION DEFINED																															
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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

### IMPLEMENTATION DEFINED, bits [63:0]

implementation defined syndrome.

## Accessing ERR<n>MISC2

Reads from ERR<n>MISC2 return an implementation defined value and writes have implementation defined behavior.

If the Common Fault Injection Mechanism is implemented by the node that owns this error record, and [ERR<q>PFGF](#).MV is 1, then some parts of this register are read/write when [ERR<n>STATUS](#).MV is 0. See [ERR<n>PFGF](#).MV for more information.

For other parts of this register, or if the Common Fault Injection Mechanism is not implemented, then Arm recommends that:

- Miscellaneous syndrome for multiple errors, such as a corrected error counter, is read/write.
- When [ERR<n>STATUS](#).MV is 1, the miscellaneous syndrome specific to the most recently recorded error ignores writes.

### Note

These recommendations allow a counter to be reset in the presence of a persistent error, while preventing specific information, such as that identifying a FRU, from being lost if an error is detected while the previous error is being logged.

**ERR<n>MISC2 can be accessed through the memory-mapped interfaces:**

Component	Offset	Instance
RAS	0x030 + (64 * n)	ERR<n>MISC2

Accesses on this interface are **RW**.

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