dex by	Sh
coding	Pseud

BaseSIMD&FPSVESMEIndex byInstructionsInstructionsInstructionsInstructionsEncoding

SQXTUNT

Signed saturating unsigned extract narrow (top)

Saturate the signed integer value in each source element to an unsigned integer value that is half the original source element width, and place the results in the odd-numbered half-width destination elements, leaving the even-numbered elements unchanged.

0 1 0 0 0 1 0 1 0 tszh 1 tszl 0 0 0 0 1 0 1 0 1 Zn Zd	31	30	29	28	27	26	25	24	23	22	21	20 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	0	0	1	0	1	0	tszh	1	tszl	0	0	0	0	1	0	1	0	1			Zn					Zd		

SQXTUNT <Zd>.<T>, <Zn>.<Tb>

```
if !HaveSVE2() && !HaveSME() then UNDEFINED;
bits(3) tsize = tszh:tszl;
integer esize;
case tsize of
   when '001' esize = 16;
   when '010' esize = 32;
   when '100' esize = 64;
   otherwise UNDEFINED;
integer n = UInt(Zn);
integer d = UInt(Zd);
```

Assembler Symbols

<Zd>

Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T>

Is the size specifier, encoded in "tszh:tszl":

tszh	tszl	<t></t>
0	00	RESERVED
0	01	В
0	10	Н
Х	11	RESERVED
1	00	S
1	01	RESERVED
1	10	RESERVED

<Zn>

Is the name of the first source scalable vector register, encoded in the "Zn" field.

Is the size specifier, encoded in "tszh:tszl":

tszh	tszl	<tb></tb>						
0	00	RESERVED						
0	01	Н						
0	10	S						
X	11	RESERVED						
1	00	D						
1	01	RESERVED						
1	10	RESERVED						

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV esize;
bits(VL) operand1 = Z[n, VL];
bits(VL) result = Z[d, VL];
constant integer halfesize = esize DIV 2;

for e = 0 to elements-1
   integer element1 = SInt(Elem[operand1, e, esize]);
   bits(halfesize) res = UnsignedSat(element1, halfesize);
   Elem[result, 2*e + 1, halfesize] = res;
Z[d, VL] = result;
```

<u>Base</u> <u>SIMD&FP</u> <u>SVE</u> <u>SME</u> <u>Index by</u> <u>Instructions</u> <u>Instructions</u> <u>Instructions</u> <u>Encoding</u>

 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no_diffs_2023_09_RC2,\ sve\ v2023-06_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$

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