

VMECID_A_EL2, Alternate MECID for EL1&0 stage 2 translation regime

The VMECID_A_EL2 characteristics are:

Purpose

Alternate MECID for EL1&0 stage 2 translation regime.

Configuration

This register is present only when FEAT_MEC is implemented, IsCurrentSecurityState(SS_Realm) and (EL2 is implemented or EL3 is implemented). Otherwise, direct accesses to VMECID_A_EL2 are undefined.

Attributes

VMECID_A_EL2 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																MECID															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits [63:16]

Reserved, res0.

MECID, bits [15:0]

If MECIDWidth is less than 16, bits[15:MECIDWidth] are res0.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing VMECID_A_EL2

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, VMECID_A_EL2

op0	op1	CRn	CRm	op2
0b11	0b100	0b1010	0b1001	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if !IsCurrentSecurityState(SS_Realm) then
        UNDEFINED;
    else
        X[t, 64] = VMECID_A_EL2;
elsif PSTATE.EL == EL3 then
    X[t, 64] = VMECID_A_EL2;
```

MSR VMECID_A_EL2, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b100	0b1010	0b1001	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if !IsCurrentSecurityState(SS_Realm) then
        UNDEFINED;
    else
        VMECID_A_EL2 = X[t, 64];
elsif PSTATE.EL == EL3 then
    VMECID_A_EL2 = X[t, 64];
```

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