

**FTSSEL**

Floating-point trigonometric select coefficient

The `FTSSEL` instruction selects the coefficient for the final multiplication in the polynomial series approximation. The instruction places the value 1.0 or a copy of the first source vector element in the destination element, depending on bit 0 of the quadrant number `q` held in the corresponding element of the second source vector. The sign bit of the destination element is copied from bit 1 of the corresponding value of `q`. This instruction is unpredicated.

To compute  $\sin(x)$  or  $\cos(x)$  the instruction is executed with elements of the first source vector set to  $x$ , adjusted to be in the range  $-\pi/4 < x \leq \pi/4$ . The elements of the second source vector hold the corresponding value of the quadrant `q` number as an integer not a floating-point value. The value `q` satisfies the relationship  $(2q-1)\pi/4 < x \leq (2q+1)\pi/4$ .

This instruction is illegal when executed in Streaming SVE mode, unless `FEAT_SME_FA64` is implemented and enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	size	1	Zm				1	0	1	1	0	0	Zn				Zd							

**FTSSEL** `<Zd>.<T>, <Zn>.<T>, <Zm>.<T>`

```
if !HaveSVE() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer n = UInt(Zn);
integer m = UInt(Zm);
integer d = UInt(Zd);
```

**Assembler Symbols**

`<Zd>` Is the name of the destination scalable vector register, encoded in the "Zd" field.

`<T>` Is the size specifier, encoded in "size":

size	<T>
00	RESERVED
01	H
10	S
11	D

`<Zn>` Is the name of the first source scalable vector register, encoded in the "Zn" field.

<Zm>

Is the name of the second source scalable vector register, encoded in the "Zm" field.

## Operation

```
CheckNonStreamingSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV esize;
bits(VL) operand1 = Z[n, VL];
bits(VL) operand2 = Z[m, VL];
bits(VL) result;

for e = 0 to elements-1
    bits(esize) element1 = Elem[operand1, e, esize];
    bits(esize) element2 = Elem[operand2, e, esize];
    Elem[result, e, esize] = FPTrigSSel(element1, element2);

Z[d, VL] = result;
```

[Base  
Instructions](#)

[SIMD&FP  
Instructions](#)

[SVE  
Instructions](#)

[SME  
Instructions](#)

[Index by  
Encoding](#)

[Sh  
Pseudocode](#)

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56

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