PMDEVAFF, Performance Monitors Device Affinity register

The PMDEVAFF characteristics are:

Purpose

Copy of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the Performance Monitor component relates to.

Configuration

This register is present only when FEAT_PMUv3_EXT64 is implemented. Otherwise, direct accesses to PMDEVAFF are res0.

Attributes

PMDEVAFF is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MPIDR_EL1																															
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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

MPIDR_EL1, bits [63:0]

MPIDR_EL1. Read-only copy of MPIDR_EL1, as seen from the highest implemented Exception level.

Accessing PMDEVAFF

Accesses to this register use the following encodings:

Accessible at offset 0xFA8 from PMU

- When FEAT_DoPD is implemented and !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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