TRCSTALLCTLR, Stall Control Register

The TRCSTALLCTLR characteristics are:

Purpose

Enables trace unit functionality that prevents trace unit buffer overflows.

Configuration

External register TRCSTALLCTLR bits [31:0] are architecturally mapped to AArch64 System register TRCSTALLCTLR[31:0].

This register is present only when FEAT_ETE is implemented, FEAT_TRC_EXT is implemented and TRCIDR3.STALLCTL == 1. Otherwise, direct accesses to TRCSTALLCTLR are res0.

Attributes

TRCSTALLCTLR is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																		NOOVERFLOW		RES0				ISTALL		RES0				LEVEL	

Bits [31:14]

Reserved, res0.

NOOVERFLOW, bit [13]
When TRCIDR3.NOOVERFLOW == 1:

Trace overflow prevention.

NOOVERFLOW	Meaning
0b0	Trace unit buffer overflow prevention is disabled.
0b1	Trace unit buffer overflow prevention is enabled.

Note that enabling this feature might cause a significant performance impact.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [12:9]

Reserved, res0.

ISTALL, bit [8]

Instruction stall control. Controls if a trace unit can stall the PE when the trace buffer space is less than LEVEL.

ISTALL	Meaning
`0b0`	The trace unit must not stall the PE.
`0b1`	The trace unit can stall the PE.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Bits [7:4]

Reserved, res0.

LEVEL, bits [3:0]

Threshold level field. The field can support 16 monotonic levels from `0b0000` to `0b1111`.

The value `0b0000` defines the Minimal invasion level. This setting has a greater risk of a trace unit buffer overflow.

The value `0b1111` defines the Maximum invasion level. This setting has a reduced risk of a trace unit buffer overflow.

Note that for some implementations, invasion might occur at the minimal invasion level.

One or more of the least significant bits of LEVEL are permitted to be res0. Arm recommends that LEVEL[3:2] are fully implemented. Arm strongly recommends that LEVEL[3] is always implemented. If one or more bits are res0 and are written with a nonzero value, the

effective value of LEVEL is rounded down to the nearest power of 2 value which has the res0 bits as zero. For example, if LEVEL[1:0] are res0 and a value of `0b1110` is written to LEVEL, the effective value of LEVEL is `0b1100`.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Accessing TRCSTALLCTLR

Must be programmed if implemented.

Writes are constrained unpredictable if the trace unit is not in the Idle state.

TRCSTALLCTLR can be accessed through the external debug interface:

Component	Offset	Instance
ETE	`0x02C`	TRCSTALLCTLR

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or ! IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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