# GICR_ICACTIVER0, Interrupt Clear-Active Register 0

The GICR_ICACTIVER0 characteristics are:

## Purpose

Deactivates the corresponding SGI or PPI. These registers are used when saving and restoring GIC state.

## Configuration

A copy of this register is provided for each Redistributor.

## Attributes

GICR_ICACTIVER0 is a 32-bit register.

## Field descriptions

| 31 | 30 | 29 | 28 | 27 | |
|---|---|---|---|---|---|
| Clear_active_bit31 | Clear_active_bit30 | Clear_active_bit29 | Clear_active_bit28 | Clear_active_bit27 | Clear_a |

### Clear_active_bit<x>, bit [x], for x = 31 to 0

Removes the active state from interrupt number x. Reads and writes have the following behavior:

| Clear_active_bit<x> | Meaning |
|---|---|
| 0b0 | If read, indicates that the corresponding interrupt is not active, and is not active and pending.<br>If written, has no effect. |

| | |
|---|---|
| 0b1 | If read, indicates that the corresponding interrupt is active, or is active and pending.<br>If written, deactivates the corresponding interrupt, if the interrupt is active. If the interrupt is already deactivated, the write has no effect. |

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

## Accessing GICR_ICACTIVER0

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICACTIVER0, the corresponding bit is RAZ/WI and equivalent functionality is provided by GICD_ICACTIVER<n> with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by GICD_ICACTIVER<n>.

When GICD_CTLR.DS == 0, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.

**GICR_ICACTIVER0 can be accessed through the memory-mapped interfaces:**

| Component | Frame | Offset | Instance |
|---|---|---|---|
| GIC Redistributor | SGI_base | 0x0380 | GICR_ICACTIVER0 |

Accesses on this interface are **RW**.