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SYS

System instruction. For more information, see *Op0 equals 0b01*, cache maintenance, *TLB maintenance*, and address translation instructions for the encodings of System instructions.

This instruction is used by the aliases <u>AT</u>, <u>BRB</u>, <u>CFP</u>, <u>COSP</u>, <u>CPP</u>, <u>DC</u>, <u>DVP</u>, <u>GCSPOPCX</u>, <u>GCSPOPX</u>, <u>GCSPUSHM</u>, <u>GCSPUSHX</u>, <u>GCSSS1</u>, <u>IC</u>, <u>TLBI</u>, and TRCIT.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

1 1 0 1 0 1 0 1 0 0 0 0 1 0 1 0 0 0 CRn CRm 0p2 Rt

L
```

```
SYS #<op1>, <Cn>, <Cm>, #<op2>{, <Xt>}
```

```
AArch64.CheckSystemAccess('01', op1, CRn, CRm, op2, Rt, L);
integer t = UInt(Rt);
integer sys_op1 = UInt(op1);
integer sys_op2 = UInt(op2);
integer sys_crn = UInt(CRn);
integer sys_crm = UInt(CRm);
```

Assembler Symbols

```
Is a 3-bit unsigned immediate, in the range 0 to 7, encoded in the "op1" field.
Is a name 'Cn', with 'n' in the range 0 to 15, encoded in the "CRn" field.
Is a name 'Cm', with 'm' in the range 0 to 15, encoded in the "CRm" field.
Is a 3-bit unsigned immediate, in the range 0 to 7, encoded in the "op2" field.
Is the 64-bit name of the optional general-purpose source register, defaulting to '11111', encoded in the "Rt" field.
```

Alias Conditions

Alias	Is preferred when
AT	CRn == '0111' && CRm == '100x' && <u>SysOp</u> (op1,'0111',CRm,op2)
BRB	op1 == '001' && CRn == '0111' && CRm == '0010' && <u>SysOp</u> ('00
CFP	op1 == '011' && CRn == '0111' && CRm == '0011' && op2 == '1
COSP	op1 == '011' && CRn == '0111' && CRm == '0011' && op2 == '1
CPP	op1 == '011' && CRn == '0111' && CRm == '0011' && op2 == '1

Alias	Is preferred when
<u>DC</u>	CRn == '0111' && <u>SysOp</u> (op1,'0111',CRm,op2) == <u>Sys DC</u>
<u>DVP</u>	op1 == '011' && CRn == '0111' && CRm == '0011' && op2 == '1
GCSPOPCX	op1 == '000' && CRn == '0111' && CRm == '0111' && op2 == '1
GCSPOPX	op1 == '000' && CRn == '0111' && CRm == '0111' && op2 == '1
GCSPUSHM	op1 == '011' && CRn == '0111' && CRm == '0111' && op2 == '0
GCSPUSHX	op1 == '000' && CRn == '0111' && CRm == '0111' && op2 == '1
GCSSS1	op1 == '011' && CRn == '0111' && CRm == '0111' && op2 == '0
<u>IC</u>	CRn == '0111' && <u>SysOp</u> (op1,'0111',CRm,op2) == <u>Sys_IC</u>
<u>TLBI</u>	CRn == '100x' && SysOp(op1, CRn, CRm, op2) == Sys_TLBI
TRCIT	op1 == '011' && CRn == '0111' && CRm == '0010' && op2 == '1

Operation

AArch64.SysInstr(1, sys_op1, sys_crn, sys_crm, sys_op2, t);

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56

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