PMCCNTSVR_EL1, Performance Monitors Cycle Count Saved Value Register

The PMCCNTSVR_EL1 characteristics are:

Purpose

Captures the PMU Cycle counter, PMU.PMCCNTR_EL0.

Configuration

External register PMCCNTSVR_EL1 bits [63:0] are architecturally mapped to AArch64 System register PMCCNTSVR_EL1[63:0].

This register is present only when FEAT_PMUv3_SS is implemented. Otherwise, direct accesses to PMCCNTSVR_EL1 are res0.

Attributes

PMCCNTSVR_EL1 is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
CCNT																															
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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

CCNT, bits [63:0]

Sampled Cycle Count. The value of PMU.PMCCNTR_EL0 at the last successful Capture event.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMCCNTSVR_EL1

Accesses to this register use the following encodings:

Accessible at offset 0x6F8 from PMU

- When !AllowExternalPMSSAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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