x by	<u>Sh</u>
ding	<u>Pseu</u>

<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<b>Encoding</b>

#### FRINT<r>

Floating-point round to integral value (predicated)

Round to an integral floating-point value with the specified rounding option from each active floating-point element of the source vector, and place the results in the corresponding elements of the destination vector. Inactive elements in the destination vector register remain unmodified.

<r></r>	Rounding Option
N	to nearest, with ties to even
A	to nearest, with ties away from zero
M	toward minus Infinity
P	toward plus Infinity
Z	toward zero
I	current FPCR rounding mode
X	current FPCR rounding mode, signalling inexact

It has encodings from 7 classes: <u>Current mode</u>, <u>Current mode signalling inexact</u>, <u>Nearest with ties to away</u>, <u>Nearest with ties to even</u>, <u>Toward zero</u>, <u>Toward minus infinity and Toward plus infinity</u>

## **Current mode**

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 1 1 0 0 1 0 1 size 0 0 0 0 1 1 1 1 0 1 Pg Zn Zd
```

```
FRINTI \langle Zd \rangle . \langle T \rangle, \langle Pg \rangle /M, \langle Zn \rangle . \langle T \rangle
```

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Zd);
boolean exact = FALSE;
FPRounding rounding = FPRoundingMode(FPCR[]);</pre>
```

#### **Current mode signalling inexact**

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 1 1 0 0 1 0 1 size 0 0 0 0 1 1 0 1 Pg Zn Zd
```

```
FRINTX <Zd>.<T>, <Pg>/M, <Zn>.<T>
```

```
if ! HaveSVE() && ! HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);</pre>
```

```
integer d = <u>UInt(Zd);</u>
boolean exact = TRUE;
<u>FPRounding</u> rounding = <u>FPRoundingMode(FPCR[]);</u>
```

### **Nearest with ties to away**

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 1 1 0 0 1 0 1 size 0 0 0 1 0 0 1 0 1 Pg Zn Zd
```

## FRINTA $\langle Zd \rangle$ . $\langle T \rangle$ , $\langle Pq \rangle /M$ , $\langle Zn \rangle$ . $\langle T \rangle$

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Zd);
boolean exact = FALSE;
FPRounding rounding = FPRounding TIEAWAY;</pre>
```

#### Nearest with ties to even

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 1 1 0 0 1 0 1 size 0 0 0 0 0 0 0 1 0 1 Pg Zn Zd

## FRINTN $\langle Zd \rangle$ . $\langle T \rangle$ , $\langle Pg \rangle /M$ , $\langle Zn \rangle$ . $\langle T \rangle$

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Zd);
boolean exact = FALSE;
FPRounding rounding = FPRounding TIEEVEN;</pre>
```

### **Toward zero**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 1 1 0 0 1 0 1 size 0 0 0 0 1 1 1 0 1 Pg Zn Zd

## FRINTZ $\langle Zd \rangle$ . $\langle T \rangle$ , $\langle Pg \rangle /M$ , $\langle Zn \rangle$ . $\langle T \rangle$

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Zd);
boolean exact = FALSE;
FPRounding rounding = FPRounding_ZERO;</pre>
```

# **Toward minus infinity**

31	30	29	28	27	26	25	24	23 22	21	20	19	18	17	16	15	14	13	12	11 10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	1	size	0	0	0	0	1	0	1	0	1		Pg			Zn					Zd		

# FRINTM $\langle Zd \rangle$ . $\langle T \rangle$ , $\langle Pq \rangle /M$ , $\langle Zn \rangle$ . $\langle T \rangle$

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Zd);
boolean exact = FALSE;
FPRounding rounding = FPRounding NEGINF;</pre>
```

# Toward plus infinity

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0 1 1 0 0 1 0 1 size 0 0 0 0 0 1 1 0 1 Pg Zn Zd

## FRINTP $\langle Zd \rangle$ . $\langle T \rangle$ , $\langle Pg \rangle /M$ , $\langle Zn \rangle$ . $\langle T \rangle$

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
if size == '00' then UNDEFINED;
constant integer esize = 8 << UInt(size);
integer g = UInt(Pg);
integer n = UInt(Zn);
integer d = UInt(Zd);
boolean exact = FALSE;
FPRounding rounding = FPRounding POSINF;</pre>
```

### **Assembler Symbols**

<Zd>

Is the name of the destination scalable vector register, encoded in the "Zd" field.

<T>

Is the size specifier, encoded in "size":

size	<t></t>
0.0	RESERVED
01	Н
10	S
11	D

<Pg>

Is the name of the governing scalable predicate register P0-P7, encoded in the "Pg" field.

<7.n>

Is the name of the source scalable vector register, encoded in the "Zn" field.

# **Operation**

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
constant integer elements = VL DIV esize;
bits(PL) mask = P[g, PL];
```

```
bits(VL) operand = if AnyActiveElement(mask, esize) then Z[n, VL] else
bits(VL) result = Z[d, VL];

for e = 0 to elements-1
   if ActivePredicateElement(mask, e, esize) then
        bits(esize) element = Elem[operand, e, esize];
        Elem[result, e, esize] = FPRoundInt(element, FPCR[], rounding,

Z[d, VL] = result;
```

## **Operational information**

This instruction might be immediately preceded in program order by a MOVPRFX instruction. The MOVPRFX instruction must conform to all of the following requirements, otherwise the behavior of the MOVPRFX and this instruction is unpredictable:

- The MOVPRFX instruction must be unpredicated, or be predicated using the same governing predicate register and source element size as this instruction.
- The MOVPRFX instruction must specify the same destination register as this instruction.
- The destination register must not refer to architectural register state referenced by any other source operand register of this instruction.

BaseSIMD&FPSVESMEIndex byInstructionsInstructionsInstructionsInstructions

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