TRCIDR6, ID Register 6

The TRCIDR6 characteristics are:

Purpose

Returns the tracing capabilities of the trace unit.

Configuration

External register TRCIDR6 bits [31:0] are architecturally mapped to AArch64 System register TRCIDR6[31:0].

This register is present only when FEAT_ETE is implemented and FEAT_TRC_EXT is implemented. Otherwise, direct accesses to TRCIDR6 are res0.

Attributes

TRCIDR6 is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																													EXLEVEL_RL_EL2	EXLEVEL_RL_EL1	EXLEVEL_R

Bits [31:3]

Reserved, res0.

EXLEVEL_RL_EL2, bit [2]

Indicates if Realm EL2 is implemented.

EXLEVEL_RL_EL2	Meaning
0b0	Realm EL2 is not implemented.
0b1	Realm EL2 is implemented.

EXLEVEL_RL_EL1, bit [1]

Indicates if Realm EL1 is implemented.

EXLEVEL_RL_EL1	Meaning

0b0	Realm EL1 is not implemented.
0b1	Realm EL1 is implemented.

EXLEVEL_RL_EL0, bit [0]

Indicates if Realm EL0 is implemented.

EXLEVEL_RL_EL0	Meaning
0b0	Realm EL0 is not implemented.
0b1	Realm EL0 is implemented.

Accessing TRCIDR6

TRCIDR6 can be accessed through the external debug interface:

Component	Offset	Instance
ETE	0x1F8	TRCIDR6

This interface is accessible as follows:

- When OSLockStatus() or !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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