TCR2_EL2, Extended Translation Control Register (EL2)

The TCR2_EL2 characteristics are:

Purpose

The control register for stage 1 of the EL2&0 translation regime.

Configuration

This register is present only when FEAT_TCR2 is implemented. Otherwise, direct accesses to TCR2_EL2 are undefined.

Attributes

TCR2_EL2 is a 64-bit register.

Field descriptions

When HCR_EL2.E2H == 0:

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RES0																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																		AMEC1	AMEC0	HAFT	PTTWI	RES0				D128	AIE	POE	RES0	PIE	PnCH

Unless stated otherwise, all the bits in TCR2_EL2, when they have the value 1, are permitted to be cached in a TLB.

Bits [63:14]

Reserved, res0.

AMEC1, bit [13]
When FEAT_MEC is implemented and FEAT_VHE is implemented:

This field controls the enabling of the Alternate MECID translations for the EL2&0 TTBR1 translation regime.

TCR2_EL2.AMEC1 is provided to enable the safe update of TTBR_EL2 and MECID_A_EL2, by disabling access and speculation to AMEC == 1 Block or Page descriptors during the update.

AMEC1	Meaning

0b0	Use of a Block or Page descriptor containing AMEC == 1 generates a Translation fault.
0b1	Accesses translated by a Block or Page descriptor containing AMEC == 1 are associated with the MECID configured in MECID_A1_EL2.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When IsCurrentSecurityState(SS_Secure), access to this field is **RES0**.
- When IsCurrentSecurityState(SS_NonSecure), access to this field is **RES0**.
- When SCTLR2_EL2.EMEC != 0, access to this field is **RES1**.

Otherwise:

Reserved, res0.

AMEC0, bit [12]
When FEAT_MEC is implemented:

This field controls the enabling of the Alternate MECID translations for the EL2 and EL2&0 TTBR0 translation regimes.

TCR2_EL2.AMEC0 is provided to enable the safe update of TTBR_EL2 and MECID_A_EL2, by disabling access and speculation to AMEC=1 Block or Page descriptors during the update.

AMEC0	Meaning
0b0	Use of a Block or Page descriptor containing AMEC == 1 generates a Translation fault.
0b1	Accesses translated by a Block or Page descriptor containing AMEC == 1 are associated with the MECID configured in MECID_A0_EL2.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When IsCurrentSecurityState(SS_Secure), access to this field is **RES0**.
- When IsCurrentSecurityState(SS_NonSecure), access to this field is **RES0**.
- When SCTLR2_EL2.EMEC != 0, access to this field is **RES1**.

Otherwise:

Reserved, res0.

HAFT, bit [11]
When FEAT_HAFT is implemented:

Hardware managed Access Flag for Tables.

Enables the Hardware managed Access Flag for Tables.

HAFT	Meaning
`0b0`	Hardware managed Access Flag for Tables is disabled.
`0b1`	Hardware managed Access Flag for Tables is enabled.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

PTTWI, bit [10]
When FEAT_THE is implemented:

Permit Translation table walk Incoherence.

Permits RCWS instructions to have Reduced Coherence property.

PTTWI	Meaning
0b0	Write accesses generated by RCWS at EL2 or EL2&0 do not have the Reduced Coherence property.
0b1	Write accesses generated by RCWS at EL2 or EL2&0 have the Reduced Coherence property.

This bit is permitted to be built as a read-only bit with a fixed value of 0.

This field is ignored by the PE and treated as zero when SCR_EL3.TCR2En == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [9:6]

Reserved, res0.

D128, bit [5]
When FEAT_D128 is implemented:

Enable 128-bit Page Table Descriptors.

Enables VMSAv9-128 translation system for the Stage 1 EL2 Translation Process.

D128	Meaning
0b0	Translation system follows VMSA-64 translation process.
0b1	Translation system follows VMSAv9-128 translation process.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.

- Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

AIE, bit [4]
When FEAT_AIE is implemented:

Enable Attribute Indexing Extension. Control for Attribute Indexing Extension for Stage 1 EL2 Translation Process.

AIE	Meaning
0b0	Attribute Indexing Extension Disabled.
0b1	Attribute Indexing Extension Enabled.

This field is res1 when TCR2_EL2.D128 is set.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

POE, bit [3]
When FEAT_S1POE is implemented:

POE. Controls setting of permission overlay for EL2 accesses in stage 1 of the EL2 translation regime.

POE	Meaning
0b0	Permission overlay disabled for EL2 access in stage 1 of EL2 translation regime.
0b1	Permission overlay enabled for EL2 access in stage 1 of EL2 translation regime.

This bit is not permitted to be cached in a TLB.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [2]

Reserved, res0.

PIE, bit [1]
When FEAT_S1PIE is implemented:

Select Permission Model. Controls setting of indirect permission model in Stage 1 EL2 Translation Process.

PIE	Meaning
`0b0`	Direct permission model.
`0b1`	Indirect permission model.

This field is res1 when TCR2_EL2.D128 is set.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to `0`.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

PnCH, bit [0]
When FEAT_THE is implemented:

Protected attribute enable.Indicates use of bit[52] of the stage 1 translation table entry.

PnCH	Meaning
`0b0`	Bit[52] of each stage 1 translation table entry does not indicate protected attribute.

0b1	Bit[52] of each stage 1 translation table entry indicates protected attribute.

This field is res0 when TCR2_EL2.D128 is set.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

When HCR_EL2.E2H == 1:

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	3
RES0																													
RES0																DisCH1	DisCH0	RES0	AMEC0	HAFT	PTTWI	SKL1	SKL0	D128	AIE	POE	E0P		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2

Unless stated otherwise, all the bits in TCR2_EL2, when they have the value 1, are permitted to be cached in a TLB.

Bits [63:16]

Reserved, res0.

DisCH1, bit [15]
When FEAT_D128 is implemented and TCR2_EL2.D128 == 1:

Disable Contiguous Hint for Start Table for VARange 1.

DisCH1	Meaning
0b0	Contiguous Hint of Block or Page descriptors of the Start Table for VARange 1 are not affected by this field.
0b1	Contiguous Hint of Block or Page descriptors of the Start Table for VARange 1 are disabled.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.

- Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

DisCH0, bit [14]
When FEAT_D128 is implemented and TCR2_EL2.D128 == 1:

Disable Contiguous Hint for Start Table for VARange 0.

DisCH0	Meaning
0b0	Contiguous Hint of Block or Page descriptors of the Start Table for VARange 0 are not affected by this field.
0b1	Contiguous Hint of Block or Page descriptors of the Start Table for VARange 0 are disabled.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [13]

Reserved, res0.

AMEC0, bit [12]
When FEAT_MEC is implemented:

This field controls the enabling of the Alternate MECID translations for the EL2 and EL2&0 TTBR0 translation regimes.

TCR2_EL2.AMEC0 is provided to enable the safe update of TTBR_EL2 and MECID_A_EL2, by disabling access and speculation to AMEC=1 Block or Page descriptors during the update.

AMEC0	Meaning

0b0	Use of a Block or Page descriptor containing AMEC == 1 generates a Translation fault.
0b1	Accesses translated by a Block or Page descriptor containing AMEC == 1 are associated with the MECID configured in MECID_A0_EL2.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When IsCurrentSecurityState(SS_Secure), access to this field is **RES0**.
- When IsCurrentSecurityState(SS_NonSecure), access to this field is **RES0**.
- When SCTLR2_EL2.EMEC != 0, access to this field is **RES1**.

Otherwise:

Reserved, res0.

HAFT, bit [11]
When FEAT_HAFT is implemented:

Hardware managed Access Flag for Tables.

Enables the Hardware managed Access Flag for Tables.

HAFT	Meaning
0b0	Hardware managed Access Flag for Tables is disabled.
0b1	Hardware managed Access Flag for Tables is enabled.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

PTTWI, bit [10]
When FEAT_THE is implemented:

Permit Translation table walk Incoherence.

Permits RCWS instructions to have Reduced Coherence property.

PTTWI	Meaning
0b0	Write accesses generated by RCWS do not have the Reduced Coherence property.
0b1	Write accesses generated by RCWS have the Reduced Coherence property.

This bit is permitted to be built as a read-only bit with a fixed value of 0.

This field is ignored by the PE and treated as zero when SCR_EL3.TCR2En == 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

SKL1, bits [9:8]
When FEAT_D128 is implemented:

Skip Level associated with translation table walks using TTBR1_EL2.

This determines the number of levels to be skipped in the regular start level of the Stage 1 EL2&0 translation table walks using TTBR1_EL2.

SKL1	Meaning
0b00	Skip 0 level in the regular start level.
0b01	Skip 1 level in the regular start level.

0b10	Skip 2 levels in the regular start level.
0b11	Skip 3 levels in the regular start level.

This field is IGNORED when TCR2_EL2.D128 is 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

SKL0, bits [7:6]
When FEAT_D128 is implemented:

Skip Level associated with translation table walks using TTBR0_EL2.

This determines the number of levels to be skipped in the regular start level of the Stage 1 EL2&0 translation table walks using TTBR0_EL2.

SKL0	Meaning
0b00	Skip 0 level in the regular start level.
0b01	Skip 1 level in the regular start level.
0b10	Skip 2 levels in the regular start level.
0b11	Skip 3 levels in the regular start level.

This field is IGNORED when TCR2_EL2.D128 is 0.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

D128, bit [5]
When FEAT_D128 is implemented:

Enable 128-bit Page Table Descriptors.

Enables VMSAv9-128 translation system for the Stage 1 EL2&0 Translation Process.

D128	Meaning
0b0	Translation system follows VMSA-64 translation process.
0b1	Translation system follows VMSAv9-128 translation process.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

AIE, bit [4]
When FEAT_AIE is implemented:

Enable Attribute Indexing Extension. Control for Attribute Indexing Extension for Stage 1 EL2&0 Translation Process.

AIE	Meaning
0b0	Attribute Indexing Extension Disabled.
0b1	Attribute Indexing Extension Enabled.

This field is res1 when TCR2_EL2.D128 is set.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

POE, bit [3]
When FEAT_S1POE is implemented:

POE. Controls setting of permission overlay for EL2 accesses in stage 1 of the EL2&0 translation regime.

POE	Meaning
0b0	Permission overlay disabled for EL2 access in stage 1 of EL2&0 translation regime.
0b1	Permission overlay enabled for EL2 access in stage 1 of EL2&0 translation regime.

This bit is not permitted to be cached in a TLB.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

E0POE, bit [2]
When FEAT_S1POE is implemented:

EL0 POE. controls setting of permission overlay in stage 1 of the EL2 translation regime.

E0POE	Meaning
0b0	Permission overlay disabled for EL0 access in stage 1 of EL2&0 translation regime.
0b1	Permission overlay enabled for EL0 access in stage 1 of EL2&0 translation regime.

This bit is not permitted to be cached in a TLB.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

PIE, bit [1]
When FEAT_S1PIE is implemented:

Select Permission Model. Controls setting of indirect permission model in Stage 1 EL2 Translation Process.

PIE	Meaning
0b0	Direct permission model.
0b1	Indirect permission model.

This field is res1 when TCR2_EL2.D128 is set.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

PnCH, bit [0]
When FEAT_THE is implemented:

Protected attribute enable.Indicates use of bit[52] of the stage 1 translation table entry.

PnCH	Meaning
0b0	Bit[52] of each stage 1 translation table entry does not indicate protected attribute.
0b1	Bit[52] of each stage 1 translation table entry indicate protected attribute.

This field is res1 when TCR2_EL2.D128 is set.

The reset behavior of this field is:

- On a Warm reset:
  - When EL3 is not implemented, this field resets to 0.
  - Otherwise, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Accessing TCR2_EL2

When FEAT_VHE is implemented, and HCR_EL2.E2H is 1, without explicit synchronization, accesses from EL2 using the register name TCR2_EL2 or TCR2_EL1 are not guaranteed to be ordered with respect to accesses using the other register name.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, TCR2_EL2

op0	op1	CRn	CRm	op2
0b11	0b100	0b0010	0b0000	0b011

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TCR2En == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TCR2En == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = TCR2_EL2;
elsif PSTATE.EL == EL3 then
    X[t, 64] = TCR2_EL2;
```

MSR TCR2_EL2, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b100	0b0010	0b0000	0b011

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TCR2En == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TCR2En == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        TCR2_EL2 = X[t, 64];
elsif PSTATE.EL == EL3 then
    TCR2_EL2 = X[t, 64];
```

MRS <Xt>, TCR2_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0010	0b0000	0b011

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TCR2En == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TRVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGRTR_EL2.TCR_EL1 == '1'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!IsHCRXEL2Enabled() ||
HCRX_EL2.TCR2En == '0') then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TCR2En == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        X[t, 64] = NVMem[0x270];
```

```
    else
        X[t, 64] = TCR2_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TCR2En == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TCR2En == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HCR_EL2.E2H == '1' then
        X[t, 64] = TCR2_EL2;
    else
        X[t, 64] = TCR2_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = TCR2_EL1;
```

MSR TCR2_EL1, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b0010	0b0000	0b011

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TCR2En == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT) && (!HaveEL(EL3) ||
SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TCR_EL1 == '1'
then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!IsHCRXEL2Enabled() ||
HCRX_EL2.TCR2En == '0') then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TCR2En == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> ==
'111' then
        NVMem[0x270] = X[t, 64];
    else
        TCR2_EL1 = X[t, 64];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
```

```
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TCR2En == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TCR2En == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HCR_EL2.E2H == '1' then
        TCR2_EL2 = X[t, 64];
    else
        TCR2_EL1 = X[t, 64];
elsif PSTATE.EL == EL3 then
    TCR2_EL1 = X[t, 64];
```

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