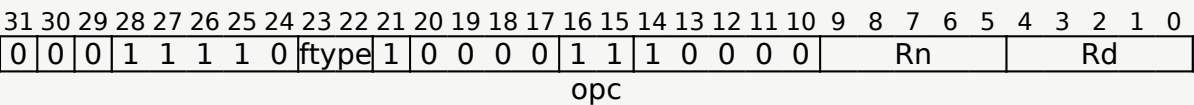


**FSQRT (scalar)**

Floating-point Square Root (scalar). This instruction calculates the square root of the value in the SIMD&FP source register and writes the result to the SIMD&FP destination register.

A floating-point exception can be generated by this instruction. Depending on the settings in *FPCR*, the exception results in either a flag being set in *FPSR*, or a synchronous exception being generated. For more information, see *Floating-point exception traps*.

Depending on the settings in the *CPACR\_EL1*, *CPTR\_EL2*, and *CPTR\_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.



**Half-precision (ftype == 11)  
(FEAT\_FP16)**

FSQRT <Hd>, <Hn>

**Single-precision (ftype == 00)**

FSQRT <Sd>, <Sn>

**Double-precision (ftype == 01)**

FSQRT <Dd>, <Dn>

```
if ftype == '10' || (ftype == '11' && !IsFeatureImplemented(FEAT_FP16))
integer d = UInt(Rd);
integer n = UInt(Rn);

constant integer esize = 8 << UInt(ftype EOR '10');
```

**Assembler Symbols**

- <Dd> Is the 64-bit name of the SIMD&FP destination register, encoded in the "Rd" field.
- <Dn> Is the 64-bit name of the SIMD&FP source register, encoded in the "Rn" field.
- <Hd> Is the 16-bit name of the SIMD&FP destination register, encoded in the "Rd" field.

|      |  |
|------|--|
| <Hn> | Is the 16-bit name of the SIMD&FP source register, encoded in the "Rn" field.      |
| <Sd> | Is the 32-bit name of the SIMD&FP destination register, encoded in the "Rd" field. |
| <Sn> | Is the 32-bit name of the SIMD&FP source register, encoded in the "Rn" field.      |

## Operation

```

CheckFPEnabled64() ;

FPCRType fpcr = FPCR[];
boolean merge = IsMerging(fpcr);
bits(128) result = if merge then V[d, 128] else 0<127:0>;

bits(esize) operand = V[n, esize];

Elem[result, 0, esize] = FPSqrt(operand, fpcr);

V[d, 128] = result;

```

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode  
no\_diffs\_2023\_09\_RC2, sve v2023-06\_rel ; Build timestamp: 2023-09-18T17:56

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