MECID_RL_A_EL3, Realm PA space Alternate MECID for EL3 stage 1 translation regime

The MECID_RL_A_EL3 characteristics are:

Purpose

Realm PA space Alternate MECID for EL3 stage 1 translation regime.

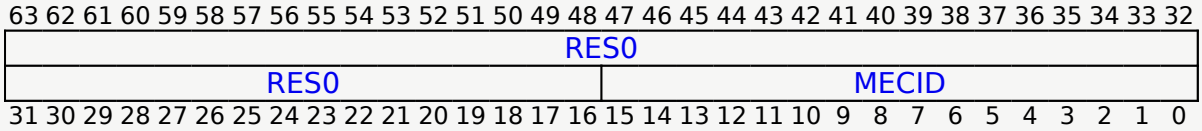
Configuration

This register is present only when FEAT_MEC is implemented. Otherwise, direct accesses to MECID_RL_A_EL3 are undefined.

Attributes

MECID_RL_A_EL3 is a 64-bit register.

Field descriptions



Bits [63:16]

Reserved, res0.

MECID, bits [15:0]

If MECIDWidth is less than 16, bits[15:MECIDWidth] are res0.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing MECID_RL_A_EL3

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, MECID_RL_A_EL3

op0	op1	CRn	CRm	op2
0b11	0b110	0b1010	0b1010	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] = MECID_RL_A_EL3;
```

MSR MECID_RL_A_EL3, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b110	0b1010	0b1010	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    MECID_RL_A_EL3 = X[t, 64];
```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