PMPIDR0, Performance Monitors Peripheral Identification Register 0

The PMPIDR0 characteristics are:

Purpose

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

This register is present only when FEAT_PMUv3_EXT is implemented and an implementation implements PMPIDR0. Otherwise, direct accesses to PMPIDR0 are res0.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

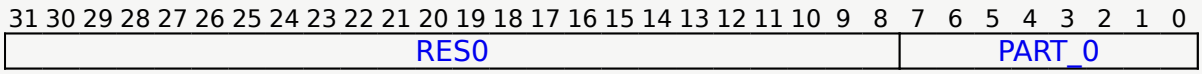
This register is required for CoreSight compliance.

Attributes

PMPIDR0 is a 32-bit register.

This register is part of the PMU block.

Field descriptions



Bits [31:8]

Reserved, res0.

PART_0, bits [7:0]

Part number, least significant byte.

This field has an implementation defined value.

Access to this field is **RO**.

Accessing PMPIDR0

Accesses to this register use the following encodings:

Accessible at offset 0xFE0 from PMU

- When FEAT_DoPD is implemented and !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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