		<u>VE                                    </u>	<del></del>
--	--	---	-------------

## **SSBB**

Speculative Store Bypass Barrier is a memory barrier that prevents speculative loads from bypassing earlier stores to the same virtual address under certain conditions. For more information and details of the semantics, see *Speculative Store Bypass Barrier (SSBB)*.

This is an alias of DSB. This means:

- The encodings in this description are named to match the encodings of <u>DSB</u>.
- The description of <u>DSB</u> gives the operational pseudocode, any constrained unpredictable behavior, and any operational information for this instruction.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 1 1 0 0 1 0 1 0 1 0 0 0 0 1 1 0 0 0 1 1 1 1 1 1 1 CRm opc
```

**SSBB** 

is equivalent to

**DSB** #0

and is always the preferred disassembly.

## **Operation**

The description of <u>DSB</u> gives the operational pseudocode for this instruction.

<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	<u>Index by</u>
<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<u>Instructions</u>	<b>Encoding</b>

 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no\_diffs\_2023\_09\_RC2,\ sve\ v2023-06\_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$ 

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