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External Registers

# AMCIDRO, Activity Monitors Component Identification Register 0

The AMCIDRO characteristics are:

### **Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Component identification scheme'.

### **Configuration**

It is implementation defined whether AMCIDR0 is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is optional.

This register is present only when FEAT\_AMUv1 is implemented.

#### **Attributes**

AMCIDR0 is a 32-bit register.

## Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6	5	4	3	2	1	0
RES0			PRMBL_0				

#### Bits [31:8]

Reserved, res0.

#### **PRMBL 0, bits [7:0]**

Preamble.

Reads as 0x0D.

Access to this field is **RO**.

## **Accessing AMCIDR0**

#### AMCIDRO can be accessed through the memory-mapped interfaces:

Component	Offset	Instance		
AMU	0xFF0	AMCIDR0		

Accesses on this interface are RO.

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