AArch64
Instructions

Index by Encoding

External Registers

AMEVCNTR0<n>, Activity Monitors Event Counter Registers 0, n = 0 - 3

The AMEVCNTR0<n> characteristics are:

Purpose

Provides access to the architected activity monitor event counters.

Configuration

External register AMEVCNTR0<n> bits [63:0] are architecturally mapped to AArch64 System register AMEVCNTR0<n> EL0[63:0].

External register AMEVCNTR0<n> bits [63:0] are architecturally mapped to AArch32 System register <u>AMEVCNTR0<n>[63:0]</u>.

It is implementation defined whether AMEVCNTR0<n> is implemented in the Core power domain or in the Debug power domain.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR0<n> are res0.

Attributes

AMEVCNTR0<n> is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

05 02 01 00 33 30 37 30 33 3 1 33 32	<u> </u>	10 15 11 15 12 11 10	3 3 3 3 3 3 7 3 3 3 3 3 1 3 3 3 <u>3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 </u>
	A CALT		
	Δ (N I		
	710111		
	A CNIT		
	Δ (N I		
	ACIVI		

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

ACNT, bits [63:0]

Architected activity monitor event counter n.

Value of architected activity monitor event counter n, where n is the number of this register and is a number from 0 to 3.

The reset behavior of this field is:

• On an AMU reset, this field resets to 0.

Accessing AMEVCNTR0<n>

If <n> is greater than or equal to the number of architected activity monitor event counters, reads of AMEVCNTR0<n> are RAZ. Software must treat reserved accesses as res0. See 'Access requirements for reserved and unallocated registers'.

Note

<u>AMCGCR</u>.CGONC identifies the number of architected activity monitor event counters.

AMEVCNTR0<n> can be accessed through the memory-mapped interfaces:

Component	Offset	Instance	Range
AMU	0x000	AMEVCNTR0 <n></n>	31:0
	+ (8 *		
	n)		

Accesses on this interface are **RO**.

Component	Offset	Instance	Range
AMU	0x004	AMEVCNTR0 <n></n>	63:32
	+ (8 *		
	n)		

Accesses on this interface are **RO**.

AArch32AArch64AArch32AArch64Index byExternalRegistersRegistersInstructionsInstructionsEncodingRegisters

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