ERR<n>PFGCDN, Error Record <n> Pseudofault Generation Countdown Register, n = 0 - 65534

The ERR<n>PFGCDN characteristics are:

Purpose

Generates one of the errors enabled in the corresponding <u>ERR<n>PFGCTL</u> register.

Configuration

This register is present only when error record <n> is implemented, the node implements the Common Fault Injection Model Extension (ERR<n>FR.INJ != 0b00) and error record <n> is the first error record owned by a node. Otherwise, direct accesses to ERR<n>PFGCDN are res0.

<u>ERR<n>FR</u> describes the features implemented by the node.

Attributes

ERR<n>PFGCDN is a 64-bit register.

Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

03 02 01 00 33 30 37 30 33 31 33 32 31 30 13 10 17 10 13 11 13 12 11 10 33 30 37 30 33 31 33 32
DECO
RESU
11250
CDM
(L)N
CDIT

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bits [63:32]

Reserved, res0.

CDN, bits [31:0]

Countdown value.

This field is copied to Error Generation Counter when either:

- Software writes 1 to ERR<n>PFGCTL.CDNEN.
- The Error Generation Counter decrements to zero and ERR<n>PFGCTL.R is 1.

While <u>ERR<n>PFGCTL</u>.CDNEN is 1 and the Error Generation Counter is nonzero, the counter decrements by 1 for each cycle at an implementation defined clock rate. When the counter reaches zero, one of the errors enabled in the <u>ERR<n>PFGCTL</u> register is generated.

Note

The current Error Generation Counter value is not visible to software.

The reset behavior of this field is:

• On a Cold reset, this field resets to an architecturally unknown value.

Accessing ERR<n>PFGCDN

ERR<n>PFGCDN can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
RAS	0x810 +	ERR <n>PFGCDN</n>
	(64 * n)	

Accesses on this interface are **RW**.

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