PMEVCNTSVR<n>_EL1, Performance Monitors Event Count Saved Value Register <n>, n = 0 - 30

The PMEVCNTSVR<n>_EL1 characteristics are:

Purpose

Captures the PMU Event counter <n>, PMU.PMEVCNTR<n>_EL0.

Configuration

External register PMEVCNTSVR<n>_EL1 bits [63:0] are architecturally mapped to AArch64 System register PMEVCNTSVR<n>_EL1[63:0].

This register is present only when FEAT_PMUv3_SS is implemented. Otherwise, direct accesses to PMEVCNTSVR<n>_EL1 are res0.

PMEVCNTSVR<n>_EL1 is in the Core power domain.

If event counter n is not implemented:

- When IsCorePowered() && !DoubleLockStatus() && ! OSLockStatus() && AllowExternalPMUAccess(), accesses are res0.
- Otherwise, it is constrained unpredictable whether accesses to this register are res0 or generate an error response.

Attributes

PMEVCNTSVR<n>_EL1 is a 64-bit register.

This register is part of the PMU block.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
EVCNT																															
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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

EVCNT, bits [63:0]

Sampled Event Count. The value of PMU.PMEVCNTR<n>_EL0 at the last successful Capture event.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMEVCNTSVR<n>_EL1

Accesses to this register use the following encodings:

```
Accessible at offset 0x600 + (8 * n)
from PMU
```

- When !AllowExternalPMSSAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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