# GICD_CTLR, Distributor Control Register

The GICD_CTLR characteristics are:

## Purpose

Enables interrupts and affinity routing.

## Configuration

The format of this register depends on the Security state of the access and the number of Security states supported, which is specified by GICD_CTLR.DS.

## Attributes

GICD_CTLR is a 32-bit register.

## Field descriptions

### When access is Secure, in a system that supports two Security states:

| 31 | 30–8 | 7 | 6 | 5 | 4 | 3 | 2 | |
|---|---|---|---|---|---|---|---|---|
| RWP | RES0 | E1NWF | DS | ARE_NS | ARE_S | RES0 | EnableGrp1S | Enab |

#### RWP, bit [31]

Register Write Pending. Read only. Indicates whether a register write is in progress or not:

| RWP | Meaning |
|---|---|
| 0b0 | No register write in progress. The effects of previous register writes to the affected register fields are visible to all logical components of the GIC architecture, including the CPU interfaces. |

| | |
|---|---|
| 0b1 | Register write in progress. The effects of previous register writes to the affected register fields are not guaranteed to be visible to all logical components of the GIC architecture, including the CPU interfaces, as the effects of the changes are still being propagated. |

This field tracks writes to:

- GICD_CTLR[2:0], the Group Enables, for transitions from 1 to 0 only.
- GICD_CTLR[7:4], the ARE bits, E1NWF bit and DS bit.
- GICD_ICENABLER<n>.

Updates to other register fields are not tracked by this field.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**Bits [30:8]**

Reserved, res0.

**E1NWF, bit [7]**

Enable 1 of N Wakeup Functionality.

It is implementation defined whether this bit is programmable, or RAZ/WI.

If it is implemented, then it has the following behavior:

| E1NWF | Meaning |
|---|---|
| 0b0 | A PE that is asleep cannot be picked for 1 of N interrupts. |
| 0b1 | A PE that is asleep can be picked for 1 of N interrupts as determined by implementation defined controls. |

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**DS, bit [6]**

Disable Security.

| DS | Meaning |
|---|---|
| 0b0 | Non-secure accesses are not permitted to access and modify registers that control Group 0 interrupts. |
| 0b1 | Non-secure accesses are permitted to access and modify registers that control Group 0 interrupts. |

If DS is written from 0 to 1 when GICD_CTLR.ARE_S == 1, then GICD_CTLR.ARE for the single Security state is RAO/WI.

If the Distributor only supports a single Security state, this bit is RAO/WI.

If the Distributor supports two Security states, it implementation defined whether this bit is programmable or implemented as RAZ/WI.

When this field is set to 1, all accesses to GICD_CTLR access the single Security state view, and all bits are accessible.

When set to 1, this field can only be cleared by a hardware reset.

Writing this bit from 0 to 1 is unpredictable if any of the following is true:

- GICD_CTLR.EnableGrp0==1.
- GICD_CTLR.EnableGrp1S==1.
- GICD_CTLR.EnableGrp1NS==1.
- One or more INTID is in the Active or Active and Pending state.

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

**ARE_NS, bit [5]**

Affinity Routing Enable, Non-secure state.

| ARE_NS | Meaning |
|---|---|
| 0b0 | Affinity routing disabled for Non-secure state. |
| 0b1 | Affinity routing enabled for Non-secure state. |

When affinity routing is enabled for the Secure state, this field is RAO/WI.

Changing the ARE_NS settings from 0 to 1 is unpredictable except when GICD_CTLR.EnableGrp1 Non-secure == 0.

Changing the ARE_NS settings from 1 to 0 is unpredictable.

If GICv2 backwards compatibility for Non-secure state is not implemented, this field is RAO/WI.

The reset behavior of this field is:

- On a GIC reset, this field resets to `0`.

**ARE_S, bit [4]**

Affinity Routing Enable, Secure state.

| ARE_S | Meaning |
|---|---|
| `0b0` | Affinity routing disabled for Secure state. |
| `0b1` | Affinity routing enabled for Secure state. |

Changing the ARE_S setting from 0 to 1 is unpredictable except when all of the following apply:

- GICD_CTLR.EnableGrp0==0.
- GICD_CTLR.EnableGrp1S==0.
- GICD_CTLR.EnableGrp1NS==0.

Changing the ARE_S settings from 1 to 0 is unpredictable.

If GICv2 backwards compatibility for Secure state is not implemented, this field is RAO/WI.

The reset behavior of this field is:

- On a GIC reset, this field resets to `0`.

**Bit [3]**

Reserved, res0.

**EnableGrp1S, bit [2]**

Enable Secure Group 1 interrupts.

| EnableGrp1S | Meaning |
|---|---|
| `0b0` | Secure Group 1 interrupts are disabled. |
| `0b1` | Secure Group 1 interrupts are enabled. |

If GICD_CTLR.ARE_S == 0, this field is res0.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

#### EnableGrp1NS, bit [1]

Enable Non-secure Group 1 interrupts.

| EnableGrp1NS | Meaning |
|---|---|
| 0b0 | Non-secure Group 1 interrupts are disabled. |
| 0b1 | Non-secure Group 1 interrupts are enabled. |

**Note**

This field also controls whether LPIs are forwarded to the PE.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

#### EnableGrp0, bit [0]

Enable Group 0 interrupts.

| EnableGrp0 | Meaning |
|---|---|
| 0b0 | Group 0 interrupts are disabled. |
| 0b1 | Group 0 interrupts are enabled. |

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

### When access is Non-secure, in a system that supports two Security states:

| 31 | 30:5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| RWP | RES0 | ARE_NS | RES0 | EnableGrp1A | EnableGrp1 | |

**RWP, bit [31]**

This bit is a read-only alias of the Secure GICD_CTLR.RWP bit.

**Bits [30:5]**

Reserved, res0.

**ARE_NS, bit [4]**

This bit is a read/write alias of the Secure GICD_CTLR.ARE_NS bit.

If GICv2 backwards compatibility for Non-secure state is not implemented, this field is RAO/WI.

**Bits [3:2]**

Reserved, res0.

**EnableGrp1A, bit [1]**

If ARE_NS == 1, then this bit is a read/write alias of the Secure GICD_CTLR.EnableGrp1NS bit.

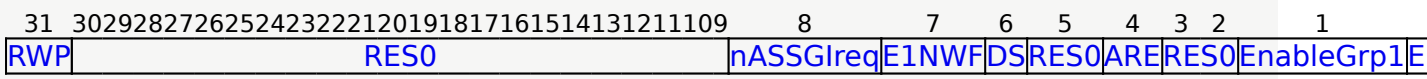
If ARE_NS == 0, then this bit is res0.

**EnableGrp1, bit [0]**

If ARE_NS == 0, then this bit is a read/write alias of the Secure GICD_CTLR.EnableGrp1NS bit.

If ARE_NS == 1, then this bit is res0.

## When in a system that supports only a single Security state:




**RWP, bit [31]**

Register Write Pending. Read only. Indicates whether a register write is in progress or not:

| RWP | Meaning |
|---|---|
| 0b0 | No register write in progress. The effects of previous register writes to the affected register fields are visible to all logical components of the GIC architecture, including the CPU interfaces. |

| | |
|---|---|
| 0b1 | Register write in progress. The effects of previous register writes to the affected register fields are not guaranteed to be visible to all logical components of the GIC architecture, including the CPU interfaces, as the effects of the changes are still being propagated. |

This field tracks updates to:

- GICD_CTLR[2:0], the Group Enables, for transitions from 1 to 0 only.
- GICD_CTLR[7:4], the ARE bits, E1NWF bit and DS bit.
- GICD_ICENABLER<n>, the bits that allow disabling of SPIs.

Updates to other register fields are not tracked by this field.

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**Bits [30:9]**

Reserved, res0.

**nASSGIreq, bit [8]**
**When FEAT_GICv4p1 is implemented:**

Controls whether SGIs have an active state.

This bit is res0 if GICD_TYPER2.GICD_TYPER2.nASSGIcap is 0.

This bit is WI when any of GICD_CTLR.{EnableGrp0,EnableGrp1} is 1.

| nASSGIreq | Meaning |
|---|---|
| 0b0 | SGIs have an active state and must be deactivated. |
| 0b1 | SGIs do not have an active state and do not require deactivation. |

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

**Otherwise:**

Reserved, res0.

**E1NWF, bit [7]**

Enable 1 of N Wakeup Functionality.

It is implementation defined whether this bit is programmable, or RAZ/WI.

If it is implemented, then it has the following behavior:

| E1NWF | Meaning |
|---|---|
| 0b0 | A PE that is asleep cannot be picked for 1 of N interrupts. |
| 0b1 | A PE that is asleep can be picked for 1 of N interrupts as determined by implementation defined controls. |

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

**DS, bit [6]**

Disable Security. This field is RAO/WI.

**Bit [5]**

Reserved, res0.

**ARE, bit [4]**

Affinity Routing Enable.

| ARE | Meaning |
|---|---|
| 0b0 | Affinity routing disabled. |
| 0b1 | Affinity routing enabled. |

Changing the ARE settings from 0 to 1 is unpredictable except when all of the following apply:

- GICD_CTLR.EnableGrp1==0.
- GICD_CTLR.EnableGrp0==0.

Changing ARE from 1 to 0 is unpredictable.

If GICv2 backwards compatibility is not implemented, this field is RAO/WI.

The reset behavior of this field is:

- On a GIC reset, this field resets to `0`.

#### Bits [3:2]

Reserved, res0.

#### EnableGrp1, bit [1]

Enable Group 1 interrupts.

| EnableGrp1 | Meaning |
|---|---|
| `0b0` | Group 1 interrupts disabled. |
| `0b1` | Group 1 interrupts enabled. |

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

#### EnableGrp0, bit [0]

Enable Group 0 interrupts.

| EnableGrp0 | Meaning |
|---|---|
| `0b0` | Group 0 interrupts are disabled. |
| `0b1` | Group 0 interrupts are enabled. |

The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

## Accessing GICD_CTLR

If an interrupt is pending within a CPU interface when the corresponding GICD_CTLR.EnableGrpX bit is written from 1 to 0 the interrupt must be retrieved from the CPU interface.

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**Note**

This might have no effect on the forwarded interrupt if it has already been activated.

When a write changes the value of ARE for a Security state or the value of the DS bit, the format used for interpreting the remaining bits provided in the write data is the format that applied before the write takes effect.

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**GICD_CTLR can be accessed through the memory-mapped interfaces:**

| Component | Frame | Offset | Instance |
|---|---|---|---|
| GIC Distributor | Dist_base | 0x0000 | GICD_CTLR |

Accesses on this interface are **RW**.

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