PMUACR_EL1, Performance Monitors User Access Control Register

The PMUACR_EL1 characteristics are:

Purpose

Enables or disables EL0 access to specfic Performance Monitors.

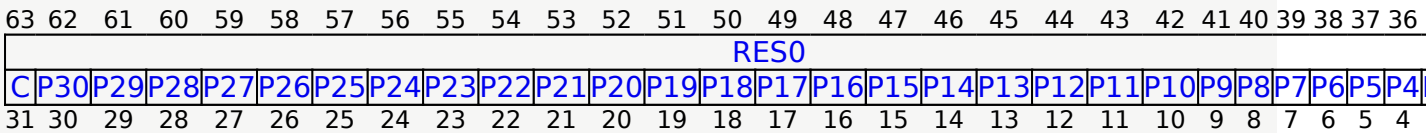
Configuration

This register is present only when FEAT_PMUv3p9 is implemented. Otherwise, direct accesses to PMUACR_EL1 are undefined.

Attributes

PMUACR_EL1 is a 64-bit register.

Field descriptions



Bits [63:33]

Reserved, res0.

F<m>, bit [m+32], for m = 0
When FEAT_PMUv3_ICNTR is implemented:

EL0 accesses to fixed-function counter <m> enable.

F<m>	Meaning
0b0	If the Effective value of PMUSERENR_EL0.UEN is 1 then EL0 accesses to fixed-function counter <m> and associated controls are RAZ/WI.

0b1	If the Effective value of PMUSERENR_EL0.UEN is 1 then EL0 accesses to fixed-function counter <m> and associated controls are read-only or read/write.

When the Effective value of PMUSERENR_EL0.UEN is 1 and PMUACR_EL1.F0 is 1:

- If PMUSERENR_EL0.IR == 0 then PMICNTR_EL0 and its associated controls are read/write at EL0.
- If PMUSERENR_EL0.IR == 1 then PMICNTR_EL0 and its associated controls are read-only at EL0.

This field is ignored by the PE when any of the following are true:

- EL1 is using AArch32.
- PMUSERENR_EL0.UEN is 0.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

C, bit [31]

EL0 accesses to PMCCNTR_EL0 enable.

C	Meaning
0b0	If the Effective value of PMUSERENR_EL0.UEN is 1 then EL0 accesses to PMCCNTR_EL0 and associated controls are RAZ/WI.
0b1	If the Effective value of PMUSERENR_EL0.UEN is 1 then EL0 accesses to PMCCNTR_EL0 and associated controls are read-only or read/write.

When the Effective value of PMUSERENR_EL0.UEN is 1 and PMUACR_EL1.C is 1:

- If PMUSERENR_EL0.CR == 0 then PMCCNTR_EL0 and its associated controls are read/write at EL0.

- If PMUSERENR_EL0.CR == 1 then PMCCNTR_EL0 and its associated controls are read-only at EL0.

This field is ignored by the PE when any of the following are true:

- EL1 is using AArch32.
- PMUSERENR_EL0.UEN is 0.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

P<m>, bit [m], for m = 30 to 0

EL0 accesses to PMEVCNTR<m>_EL0 enable.

P<m>	Meaning
0b0	If the Effective value of PMUSERENR_EL0.UEN is 1 then EL0 accesses to PMEVCNTR<m>_EL0 and associated controls are RAZ/WI.
0b1	If the Effective value of PMUSERENR_EL0.UEN is 1 then EL0 accesses to PMEVCNTR<m>_EL0 and associated controls are read-only or read/write.

When the Effective value of PMUSERENR_EL0.UEN is 1 and PMUACR_EL1.P<m> is 1:

- If PMUSERENR_EL0.ER == 0 then PMEVCNTR<m>_EL0 and its associated controls are read/write at EL0.
- If PMUSERENR_EL0.ER == 1 then PMEVCNTR<m>_EL0 and its associated controls are read-only at EL0.

This field is ignored by the PE when any of the following are true:

- EL1 is using AArch32.
- PMUSERENR_EL0.UEN is 0.

Accessing this field has the following behavior:

- This field reads-as-zero and ignores writes if any of the following are true:
    - All of the following are true:
        - EL2 is implemented and enabled in the current Security state.
        - m >= UInt(MDCR_EL2.HPMN).
        - Accessed at EL1.
    - m >= UInt(PMCR_EL0.N).

- Otherwise access to this field is read/write.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing PMUACR_EL1

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, PMUACR_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b1001	0b1110	0b100

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD ==
'1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGRTR2_EL2.nPMUACR_EL1 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = PMUACR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
```

```
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD ==
'1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = PMUACR_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = PMUACR_EL1;
```

MSR PMUACR_EL1, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b000	0b1001	0b1110	0b100

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD ==
'1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HDFGWTR2_EL2.nPMUACR_EL1 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
```

```
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            PMUACR_EL1 = X[t, 64];
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
    && boolean IMPLEMENTATION_DEFINED "EL3 trap priority
    when SDD == '1'" && MDCR_EL3.EnPM2 == '0' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD ==
    '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.EnPM2 == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            PMUACR_EL1 = X[t, 64];
    elsif PSTATE.EL == EL3 then
        PMUACR_EL1 = X[t, 64];
```

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