<u>Base</u>	SIMD&FP	<u>SVE</u>	<u>SME</u>	Index by
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PFALSE

Set all predicate elements to false

Set all elements in the destination predicate to false.

For programmer convenience, an assembler must also accept predicate-ascounter register name for the destination predicate register.

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 0 1 0 0 1 0 1 0 0 0 1 1 0 0 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 Pd
```

```
PFALSE <Pd>.B
```

```
if !HaveSVE() && !HaveSME() then UNDEFINED;
integer d = UInt(Pd);
```

Assembler Symbols

<Pd>

Is the name of the destination scalable predicate register, encoded in the "Pd" field.

Operation

```
CheckSVEEnabled();
constant integer VL = CurrentVL;
constant integer PL = VL DIV 8;
P[d, PL] = Zeros(PL);
```

Operational information

If FEAT_SVE2 is implemented or FEAT_SME is implemented, then if PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel; Build timestamp: 2023-09-18T17:56

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