TRCCIDCCTLR0, Context Identifier Comparator Control Register 0

The TRCCIDCCTLR0 characteristics are:

Purpose

Contains Context identifier mask values for the TRCCIDCVR<n> registers, for n = 0 to 3.

Configuration

External register TRCCIDCCTLR0 bits [31:0] are architecturally mapped to AArch64 System register TRCCIDCCTLR0[31:0].

This register is present only when FEAT_ETE is implemented, FEAT_TRC_EXT is implemented, UInt(TRCIDR4.NUMCIDC) > 0x0 and UInt(TRCIDR2.CIDSIZE) > 0. Otherwise, direct accesses to TRCCIDCCTLR0 are res0.

Attributes

TRCCIDCCTLR0 is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22
COMP3[7]	COMP3[6]	COMP3[5]	COMP3[4]	COMP3[3]	COMP3[2]	COMP3[1]	COMP3[0]	COMP2[7]	COMP2[6

COMP3[<m>], bit [m+24], for m = 7 to 0
When UInt(TRCIDR4.NUMCIDC) > 3:

TRCCIDCVR3 mask control. Specifies the mask value that the trace unit applies to TRCCIDCVR3. Each bit in this field corresponds to a byte in TRCCIDCVR3.

COMP3[<m>]	Meaning
0b0	The trace unit includes TRCCIDCVR3[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.

0b1	The trace unit ignores TRCCIDCVR3[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.

This bit is res0 if m >= TRCIDR2.CIDSIZE.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

COMP2[<m>], bit [m+16], for m = 7 to 0
When UInt(TRCIDR4.NUMCIDC) > 2:

TRCCIDCVR2 mask control. Specifies the mask value that the trace unit applies to TRCCIDCVR2. Each bit in this field corresponds to a byte in TRCCIDCVR2.

COMP2[<m>]	Meaning
0b0	The trace unit includes TRCCIDCVR2[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.
0b1	The trace unit ignores TRCCIDCVR2[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.

This bit is res0 if m >= TRCIDR2.CIDSIZE.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

COMP1[<m>], bit [m+8], for m = 7 to 0
When UInt(TRCIDR4.NUMCIDC) > 1:

TRCCIDCVR1 mask control. Specifies the mask value that the trace unit applies to TRCCIDCVR1. Each bit in this field corresponds to a byte in TRCCIDCVR1.

COMP1[<m>]	Meaning
0b0	The trace unit includes TRCCIDCVR1[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.
0b1	The trace unit ignores TRCCIDCVR1[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.

This bit is res0 if m >= TRCIDR2.CIDSIZE.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

COMP0[<m>], bit [m], for m = 7 to 0
When UInt(TRCIDR4.NUMCIDC) > 0:

TRCCIDCVR0 mask control. Specifies the mask value that the trace unit applies to TRCCIDCVR0. Each bit in this field corresponds to a byte in TRCCIDCVR0.

COMP0[<m>]	Meaning
0b0	The trace unit includes TRCCIDCVR0[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.
0b1	The trace unit ignores TRCCIDCVR0[(mÃ—8+7):(mÃ—8)] when it performs the Context identifier comparison.

This bit is res0 if m >= TRCIDR2.CIDSIZE.

The reset behavior of this field is:

- On a Trace unit reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Accessing TRCCIDCCTLR0

If software uses the TRCCIDCVR<n> registers, for n = 0 to 3, then it must program this register.

If software sets a mask bit to 1 then it must program the relevant byte in TRCCIDCVR<n> to `0x00`.

If any bit is 1 and the relevant byte in TRCCIDCVR<n> is not `0x00`, the behavior of the Context Identifier Comparator is constrained unpredictable. In this scenario the comparator might match unexpectedly or might not match.

Writes are constrained unpredictable if the trace unit is not in the Idle state.

TRCCIDCCTLR0 can be accessed through the external debug interface:

Component	Offset	Instance
ETE	`0x680`	TRCCIDCCTLR0

This interface is accessible as follows:

- When OSLockStatus(), or !AllowExternalTraceAccess() or ! IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

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