TRCIDR3, ID Register 3

The TRCIDR3 characteristics are:

Purpose

Returns the base architecture of the trace unit.

Configuration

External register TRCIDR3 bits [31:0] are architecturally mapped to AArch64 System register TRCIDR3[31:0].

This register is present only when FEAT_ETE is implemented and FEAT_TRC_EXT is implemented. Otherwise, direct accesses to TRCIDR3 are res0.

Attributes

TRCIDR3 is a 32-bit register.

Field descriptions

31	30	29 28	27	26	25	24	23	22	21
NOOVERFLOW	NUMPROC[2:0]		SYSSTALL	STALLCTL	SYNCPR	TRCERR	RES0	EXLEVEL_NS_EL2	EXLEVEL_NS

NOOVERFLOW, bit [31]

Indicates if overflow prevention is implemented.

NOOVERFLOW	Meaning
0b0	Overflow prevention is not implemented.
0b1	Overflow prevention is implemented.

If TRCIDR3.STALLCTL == 0 then this field is 0.

NUMPROC, bits [13:12, 30:28]

Indicates the number of PEs available for tracing.

NUMPROC	Meaning
0b00000	The trace unit can trace one PE.

This field reads as 0b00000.

The NUMPROC field is split as follows:

- NUMPROC[2:0] is TRCIDR3[30:28].
- NUMPROC[4:3] is TRCIDR3[13:12].

SYSSTALL, bit [27]

Indicates if stalling of the PE is permitted.

SYSSTALL	Meaning
0b0	Stalling of the PE is not permitted.
0b1	Stalling of the PE is permitted.

The value of this field might be dynamic and change based on system conditions.

If TRCIDR3.STALLCTL == 0 then this field is 0.

STALLCTL, bit [26]

Indicates if trace unit implements stalling of the PE.

STALLCTL	Meaning
0b0	Stalling of the PE is not implemented.
0b1	Stalling of the PE is implemented.

SYNCPR, bit [25]

Indicates if an implementation has a fixed synchronization period.

SYNCPR	Meaning
0b0	TRCSYNCPR is read/write so software can change the synchronization period.
0b1	TRCSYNCPR is read-only so the synchronization period is fixed.

This field reads as 0.

TRCERR, bit [24]

Indicates forced tracing of System Error exceptions is implemented.

TRCERR	Meaning

0b0	Forced tracing of System Error exceptions is not implemented.
0b1	Forced tracing of System Error exceptions is implemented.

This field reads as 1.

Bit [23]

Reserved, res0.

EXLEVEL_NS_EL2, bit [22]

Indicates if Non-secure EL2 is implemented.

EXLEVEL_NS_EL2	Meaning
0b0	Non-secure EL2 is not implemented.
0b1	Non-secure EL2 is implemented.

EXLEVEL_NS_EL1, bit [21]

Indicates if Non-secure EL1 is implemented.

EXLEVEL_NS_EL1	Meaning
0b0	Non-secure EL1 is not implemented.
0b1	Non-secure EL1 is implemented.

EXLEVEL_NS_EL0, bit [20]

Indicates if Non-secure EL0 is implemented.

EXLEVEL_NS_EL0	Meaning
0b0	Non-secure EL0 is not implemented.
0b1	Non-secure EL0 is implemented.

EXLEVEL_S_EL3, bit [19]

Indicates if EL3 is implemented.

EXLEVEL_S_EL3	Meaning
0b0	EL3 is not implemented.

0b1	EL3 is implemented.

EXLEVEL_S_EL2, bit [18]

Indicates if Secure EL2 is implemented.

EXLEVEL_S_EL2	Meaning
0b0	Secure EL2 is not implemented.
0b1	Secure EL2 is implemented.

EXLEVEL_S_EL1, bit [17]

Indicates if Secure EL1 is implemented.

EXLEVEL_S_EL1	Meaning
0b0	Secure EL1 is not implemented.
0b1	Secure EL1 is implemented.

EXLEVEL_S_EL0, bit [16]

Indicates if Secure EL0 is implemented.

EXLEVEL_S_EL0	Meaning
0b0	Secure EL0 is not implemented.
0b1	Secure EL0 is implemented.

Bits [15:14]

Reserved, res0.

CCITMIN, bits [11:0]

Indicates the minimum value that can be programmed in TRCCCCTLR.THRESHOLD.

If TRCIDR0.TRCCCI == 1 then the minimum value of this field is 0x001.

If TRCIDR0.TRCCCI == 0 then this field is zero.

Accessing TRCIDR3

TRCIDR3 can be accessed through the external debug interface:

Component	Offset	Instance
ETE	0x1EC	TRCIDR3

This interface is accessible as follows:

- When OSLockStatus() or !IsTraceCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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