

# GICR\_NSACR, Non-secure Access Control Register

The GICR\_NSACR characteristics are:

## Purpose

Enables Secure software to permit Non-secure software to create SGIs targeting the PE connected to this Redistributor by writing to [ICC\\_SGI1R\\_EL1](#), [ICC\\_ASGI1R\\_EL1](#) or [ICC\\_SGI0R\\_EL1](#).

For more information, see 'Forwarding an SGI to a target PE' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

## Configuration

For a description on when a write to [ICC\\_SGI0R\\_EL1](#), [ICC\\_SGI1R\\_EL1](#) or [ICC\\_ASGI1R\\_EL1](#) is permitted to generate an interrupt, see 'Use of control registers for SGI forwarding' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

## Attributes

GICR\_NSACR is a 32-bit register.

## Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NS_access0	NS_access1	NS_access2	NS_access3	NS_access4	NS_access5	NS_access6	NS_access7	NS_access8	NS_access9	NS_access10	NS_access11	NS_access12	NS_access13	NS_access14	NS_access15	NS_access16	NS_access17	NS_access18	NS_access19	NS_access20	NS_access21	NS_access22	NS_access23	NS_access24	NS_access25	NS_access26	NS_access27	NS_access28	NS_access29	NS_access30	NS_access31

**NS\_access<x>, bits [2x+1:2x], for x = 15 to 0**

Configures the level of Non-secure access permitted when the SGI is in Secure Group 0 or Secure Group 1, as defined from [GICR\\_IGROUPR0](#) and [GICR\\_IGRPMODR0](#). A field is provided for each SGI. The possible values of each 2-bit field are:

NS_access<x>	Meaning
0b00	Non-secure writes are not permitted to generate Secure Group 0 SGIs or Secure Group 1 SGIs.

0b01	Non-secure writes are permitted to generate a Secure Group 0 SGI.
0b10	As 0b01, but additionally Non-secure writes to are permitted to generate a Secure Group 1 SGI.
0b11	Reserved. If the field is programmed to the reserved value, then the hardware will treat the field as if it has been programmed to an implementation defined choice of the valid values. However, to maintain the principle that as the value increases additional accesses are permitted Arm strongly recommends that implementations treat this value as 0b10. It is implementation defined whether the value read back is the value programmed or the valid value chosen.

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The reset behavior of this field is:

- On a GIC reset, this field resets to an architecturally unknown value.

## Accessing GICR\_NSACR

This register is used when affinity routing is enabled. When affinity routing is not enabled for the Security state of the interrupt, [GICD\\_NSACR<n>](#) with n=0 provides equivalent functionality.

This register does not support PPIs.

**GICR\_NSACR can be accessed through the memory-mapped interfaces:**

Component	Frame	Offset	Instance
GIC Redistributor	SGI_base	0x0E00	GICR_NSACR

This interface is accessible as follows:

- When GICD\_CTLR.DS == 1, accesses to this register are **RAZ/WI**.
- When GICD\_CTLR.DS == 0 and an access is Secure, accesses to this register are **RW**.
- When GICD\_CTLR.DS == 0 and an access is Non-secure, accesses to this register are **RAZ/WI**.
- When GICD\_CTLR.DS == 0, FEAT\_RME is implemented and an access is Root, accesses to this register are **RW**.
- When GICD\_CTLR.DS == 0, FEAT\_RME is implemented and an access is Realm, accesses to this register are **RAZ/WI**.

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