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FCSEL

Floating-point Conditional Select (scalar). This instruction allows the SIMD&FP destination register to take the value from either one or the other of two SIMD&FP source registers. If the condition passes, the first SIMD&FP source register value is taken, otherwise the second SIMD&FP source register value is taken.

Depending on the settings in the *CPACR_EL1*, *CPTR_EL2*, and *CPTR_EL3* registers, and the current Security state and Exception level, an attempt to execute the instruction might be trapped.

31 30 29	28 27	26 2	25 24	23 22	21	20 19 18 17 1	6 15 14 13	12	11 1	9	8	7	6	5	4	3	2	1	0
0 0 0	1 1	1	1 0	ftype	1	Rm	cond		1 1			Rn					Rd		

```
Half-precision (ftype == 11)
(FEAT_FP16)
```

```
FCSEL <Hd>, <Hn>, <Hm>, <cond>
```

Single-precision (ftype == 00)

```
FCSEL <Sd>, <Sn>, <Sm>, <cond>
```

Double-precision (ftype == 01)

```
FCSEL <Dd>, <Dn>, <Dm>, <cond>
if ftype == '10' || (ftype == '11' && !IsFeatureImplemented(FEAT_FP16))
integer d = UInt(Rd);
integer n = UInt(Rn);
integer m = UInt(Rm);
```

Assembler Symbols

<dd></dd>	Is the 64-bit name of the SIMD&FP destination register, encoded in the "Rd" field.
<dn></dn>	Is the 64-bit name of the first SIMD&FP source register, encoded in the "Rn" field.
<dm></dm>	Is the 64-bit name of the second SIMD&FP source register, encoded in the "Rm" field.
<hd></hd>	Is the 16-bit name of the SIMD&FP destination register, encoded in the "Rd" field.

constant integer datasize = 8 << UInt(ftype EOR '10');</pre>

<hn></hn>	Is the 16-bit name of the first SIMD&FP source register, encoded in the "Rn" field.
<hm></hm>	Is the 16-bit name of the second SIMD&FP source register, encoded in the "Rm" field.
<sd></sd>	Is the 32-bit name of the SIMD&FP destination register, encoded in the "Rd" field.
<sn></sn>	Is the 32-bit name of the first SIMD&FP source register, encoded in the "Rn" field.
<sm></sm>	Is the 32-bit name of the second SIMD&FP source register, encoded in the "Rm" field.
<cond></cond>	Is one of the standard conditions, encoded in the "cond" field in the standard way.

Operation

```
CheckFPEnabled64(); bits(datasize) result; result = if ConditionHolds(cond) then V[n, datasize] else V[m, datasize] V[d, datasize] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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 $Internal\ version\ only: is a\ v33.64,\ AdvSIMD\ v29.12,\ pseudocode\ no_diffs_2023_09_RC2,\ sve\ v2023-06_rel\ ;\ Build\ timestamp:\ 2023-09-18T17:56$

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