PMICFILTR_EL0, Performance Monitors Instruction Counter Filter Register

The PMICFILTR_EL0 characteristics are:

Purpose

Configures the Instruction Counter.

Configuration

External register PMICFILTR_EL0 bits [63:0] are architecturally mapped to AArch64 System register PMICFILTR_EL0[63:0].

This register is present only when FEAT_PMUv3_ICNTR is implemented. Otherwise, direct accesses to PMICFILTR_EL0 are res0.

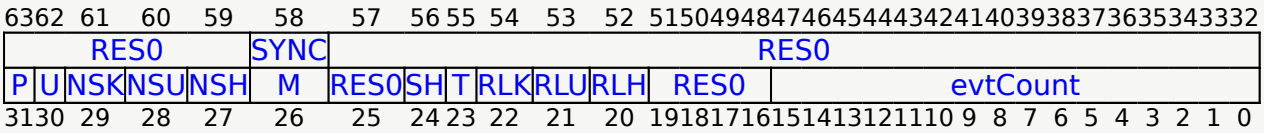
PMICFILTR_EL0 is in the Core power domain.

Attributes

PMICFILTR_EL0 is a 64-bit register.

This register is part of the PMU block.

Field descriptions



Bits [63:59]

Reserved, res0.

SYNC, bit [58]
When FEAT_SEBEP is implemented:

Synchronous mode. Controls whether a PMU exception generated by the counter is synchronous or asynchronous.

SYNC	Meaning
0b0	Asynchronous PMU exception is enabled.

0b1	Synchronous PMU exception is enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [57:32]

Reserved, res0.

P, bit [31]

EL1 filtering. Controls counting instructions in EL1.

P	Meaning
0b0	This field has no effect on filtering of instructions.
0b1	Instructions in EL1 are not counted.

If Secure and Non-secure states are implemented, then counting instructions in Non-secure EL1 is further controlled by PMICFILTR_EL0.NSK.

If FEAT_RME is implemented, then counting instructions in Realm EL1 is further controlled by PMICFILTR_EL0.RLK.

If EL3 is implemented, then counting instructions in EL3 is further controlled by PMICFILTR_EL0.M.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

U, bit [30]

EL0 filtering. Controls counting instructions in EL0.

U	Meaning
0b0	This field has no effect on filtering of instructions.
0b1	Instructions in EL0 are not counted.

If Secure and Non-secure states are implemented, then counting instructions in Non-secure EL0 is further controlled by PMICFILTR_EL0.NSU.

If FEAT_RME is implemented, then counting instructions in Realm EL0 is further controlled by PMICFILTR_EL0.RLU.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

NSK, bit [29]
When EL3 is implemented:

Non-secure EL1 filtering. Controls counting instructions in Non-secure EL1. If PMICFILTR_EL0.NSK is not equal to PMICFILTR_EL0.P, then instructions in Non-secure EL1 are not counted. Otherwise, PMICFILTR_EL0.NSK has no effect on filtering of instructions in Non-secure EL1.

NSK	Meaning
0b0	When PMICFILTR_EL0.P == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.P == 1, instructions in Non-secure EL1 are not counted.
0b1	When PMICFILTR_EL0.P == 0, instructions in Non-secure EL1 are not counted. When PMICFILTR_EL0.P == 1, this field has no effect on filtering of instructions.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

NSU, bit [28]
When EL3 is implemented:

Non-secure EL0 filtering. Controls counting instructions in Non-secure EL0. If PMICFILTR_EL0.NSU is not equal to PMICFILTR_EL0.U, then instructions in Non-secure EL0 are not counted. Otherwise, PMICFILTR_EL0.NSU has no effect on filtering of instructions in Non-secure EL0.

NSU	Meaning
0b0	When PMICFILTR_EL0.U == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.U == 1, instructions in Non-secure EL0 are not counted.
0b1	When PMICFILTR_EL0.U == 0, instructions in Non-secure EL0 are not counted. When PMICFILTR_EL0.U == 1, this field has no effect on filtering of instructions.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

NSH, bit [27]
When EL2 is implemented:

EL2 filtering. Controls counting instructions in EL2.

NSH	Meaning
0b0	Instructions in EL2 are not counted.
0b1	This field has no effect on filtering of instructions.

If EL3 is implemented and FEAT_SEL2 is implemented, then counting instructions in Secure EL2 is further controlled by PMICFILTR_EL0.SH.

If FEAT_RME is implemented, then counting instructions in Realm EL2 is further controlled by PMICFILTR_EL0.RLH.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

M, bit [26]
When EL3 is implemented:

EL3 filtering. Controls counting instructions in EL3. If PMICFILTR_EL0.M is not equal to PMICFILTR_EL0.P, then instructions in EL3 are not counted. Otherwise, PMICFILTR_EL0.M has no effect on filtering of instructions in EL3.

M	Meaning
0b0	When PMICFILTR_EL0.P == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.P == 1, instructions in EL3 are not counted.
0b1	When PMICFILTR_EL0.P == 0, instructions in EL3 are not counted. When PMICFILTR_EL0.P == 1, this field has no effect on filtering of instructions.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bit [25]

Reserved, res0.

SH, bit [24]
When EL3 is implemented and FEAT_SEL2 is implemented:

Secure EL2 filtering. Controls counting instructions in Secure EL2. If PMICFILTR_EL0.SH is equal to PMICFILTR_EL0.NSH, then instructions in Secure EL2 are not counted. Otherwise,

PMICFILTR_EL0.SH has no effect on filtering of instructions in Secure EL2.

SH	Meaning
0b0	When PMICFILTR_EL0.NSH == 0, instructions in Secure EL2 are not counted. When PMICFILTR_EL0.NSH == 1, this field has no effect on filtering of instructions.
0b1	When PMICFILTR_EL0.NSH == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.NSH == 1, instructions in Secure EL2 are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When !IsSecureEL2Enabled(), access to this field is **RES0**.
- Otherwise, access to this field is **RW**.

Otherwise:

Reserved, res0.

T, bit [23]
When FEAT_TME is implemented:

Non-transactional state filtering. Controls counting instructions in Non-transactional state.

T	Meaning
0b0	This field has no effect on filtering of instructions.
0b1	Instructions in Non-transactional state are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

RLK, bit [22]
When FEAT_RME is implemented:

Realm EL1 filtering. Controls counting instructions in Realm EL1. If PMICFILTR_EL0.RLK is not equal to PMICFILTR_EL0.P, then instructions in Realm EL1 are not counted. Otherwise, PMICFILTR_EL0.RLK has no effect on filtering of instructions in Realm EL1.

RLK	Meaning
0b0	When PMICFILTR_EL0.P == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.P == 1, instructions in Realm EL1 are not counted.
0b1	When PMICFILTR_EL0.P == 0, instructions in Realm EL1 are not counted. When PMICFILTR_EL0.P == 1, this field has no effect on filtering of instructions.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

RLU, bit [21]
When FEAT_RME is implemented:

Realm EL0 filtering. Controls counting instructions in Realm EL0. If PMICFILTR_EL0.RLU is not equal to PMICFILTR_EL0.U, then instructions in Realm EL0 are not counted. Otherwise, PMICFILTR_EL0.RLU has no effect on filtering of instructions in Realm EL0.

RLU	Meaning

0b0	When PMICFILTR_EL0.U == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.U == 1, instructions in Realm EL0 are not counted.
0b1	When PMICFILTR_EL0.U == 0, instructions in Realm EL0 are not counted. When PMICFILTR_EL0.U == 1, this field has no effect on filtering of instructions.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

RLH, bit [20]
When FEAT_RME is implemented:

Realm EL2 filtering. Controls counting instructions in Realm EL2. If PMICFILTR_EL0.RLH is equal to PMICFILTR_EL0.NSH, then instructions in Realm EL2 are not counted. Otherwise, PMICFILTR_EL0.RLH has no effect on filtering of instructions in Realm EL2.

RLH	Meaning
0b0	When PMICFILTR_EL0.NSH == 0, instructions in Realm EL2 are not counted. When PMICFILTR_EL0.NSH == 1, this field has no effect on filtering of instructions.
0b1	When PMICFILTR_EL0.NSH == 0, this field has no effect on filtering of instructions. When PMICFILTR_EL0.NSH == 1, instructions in Realm EL2 are not counted.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, res0.

Bits [19:16]

Reserved, res0.

evtCount, bits [15:0]

Event to count.

Reads as `0x0008`.

Access to this field is **RO**.

Accessing PMICFILTR_EL0

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT32 is implemented

[31:0] Accessible at offset 0x480 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

When FEAT_PMUv3_EXT64 is implemented

Accessible at offset 0x500 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RW**.

When FEAT_PMUv3_EXT32 is implemented

[63:32] Accessible at offset 0xA80 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

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