Base SIMD&FP Instructions Instructions

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EXTR

Extract register extracts a register from a pair of registers.

This instruction is used by the alias ROR (immediate).

31 30 29 28 27 26 25 2	24 23 22 21	20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5	4 3 2 1 0
sf 0 0 1 0 0 1	1 1 N 0	Rm	imms	Rn	Rd

```
32-bit (sf == 0 \&\& N == 0 \&\& imms == 0xxxxx)
```

"imms" field.

```
EXTR <Wd>, <Wn>, <Wm>, #<lsb>
```

64-bit (sf == 1 && N == 1)

```
EXTR <Xd>, <Xn>, <Xm>, #<lsb>
if N != sf then UNDEFINED;
if sf == '0' && imms<5> == '1' then UNDEFINED;

integer d = UInt(Rd);
integer n = UInt(Rn);
integer m = UInt(Rm);
constant integer datasize = 32 << UInt(sf);
constant integer lsb = UInt(imms);</pre>
```

Assembler Symbols

<wd></wd>	Is the 32-bit name of the general-purpose destination register, encoded in the "Rd" field.
<wn></wn>	Is the 32-bit name of the first general-purpose source register, encoded in the "Rn" field.
<wm></wm>	Is the 32-bit name of the second general-purpose source register, encoded in the "Rm" field.
<xd></xd>	Is the 64-bit name of the general-purpose destination register, encoded in the "Rd" field.
<xn></xn>	Is the 64-bit name of the first general-purpose source register, encoded in the "Rn" field.
<xm></xm>	Is the 64-bit name of the second general-purpose source register, encoded in the "Rm" field.
<lsb></lsb>	For the 32-bit variant: is the least significant bit position

from which to extract, in the range 0 to 31, encoded in the

For the 64-bit variant: is the least significant bit position from which to extract, in the range 0 to 63, encoded in the "imms" field.

Alias Conditions

Alias	Is preferred when		
ROR (immediate)	Rn == Rm		

Operation

```
bits(datasize) result;
bits(datasize) operand1 = X[n, datasize];
bits(datasize) operand2 = X[m, datasize];
bits(2*datasize) concat = operand1:operand2;
result = concat<(lsb+datasize)-1:lsb>;
X[d, datasize] = result;
```

Operational information

If PSTATE.DIT is 1:

- The execution time of this instruction is independent of:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.
- The response of this instruction to asynchronous exceptions does not vary based on:
 - The values of the data supplied in any of its registers.
 - The values of the NZCV flags.

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