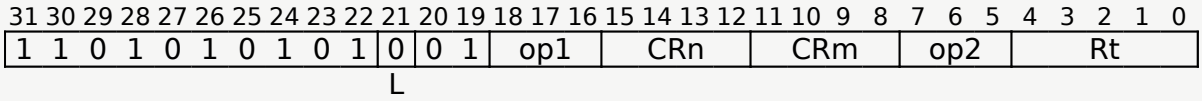
SYSP

128-bit System instruction.
This instruction is used by the alias TLBIP.

System
(FEAT_SYSINSTR128)



SYSP #<op1>, <Cn>, <Cm>, #<op2>{, <Xt1>, <Xt2>}

```
if !IsFeatureImplemented(FEAT_SYSINSTR128) then UNDEFINED;
if Rt<0> == '1' && Rt != '11111' then UNDEFINED;
AArch64.CheckSystemAccess('01', op1, CRn, CRm, op2, Rt, L);

integer t = UInt(Rt);
integer t2 = if t == 31 then 31 else UInt(Rt) + 1;

integer sys_op1 = UInt(op1);
integer sys_op2 = UInt(op2);
integer sys_crn = UInt(CRn);
integer sys_crm = UInt(CRm);
```

Assembler Symbols

<op1>	Is a 3-bit unsigned immediate, in the range 0 to 6, encoded in the "op1" field.
<Cn>	Is a name 'Cn', with 'n' in the range 8 to 9, encoded in the "CRn" field.
<Cm>	Is a name 'Cm', with 'm' in the range 0 to 7, encoded in the "CRm" field.
<op2>	Is a 3-bit unsigned immediate, in the range 0 to 7, encoded in the "op2" field.
<Xt1>	Is the 64-bit name of the first optional general-purpose source register, defaulting to '11111', encoded in the "Rt" field.
<Xt2>	Is the 64-bit name of the second optional general-purpose source register, defaulting to '11111', encoded as "Rt" +1. Defaults to '11111' if "Rt" = '11111'.

Alias Conditions

Alias	Is preferred when
TLBIP	`CRn == '100x' && SysOp(op1,CRn,CRm,op2) == Sys_TLBIP`

Operation

```
AArch64.SysInstr128(1, sys_op1, sys_crn, sys_crm, sys_op2, t, t2);
```

Internal version only: isa v33.64, AdvSIMD v29.12, pseudocode no_diffs_2023_09_RC2, sve v2023-06_rel ; Build timestamp: 2023-09-18T17:56