

GICD_IPRIORITYR<n>, Interrupt Priority Registers, n = 0 - 254

The GICD_IPRIORITYR<n> characteristics are:

Purpose

Holds the priority of the corresponding interrupt.

Configuration

These registers are available in all configurations of the GIC. When [GICD_CTLR.DS](#)=0, these registers are Common.

The number of implemented GICD_IPRIORITYR<n> registers is 8*([GICD_TYPER.ITLinesNumber](#)+1). Registers are numbered from 0.

GICD_IPRIORITYR0 to GICD_IPRIORITYR7 are Banked for each connected PE with [GICR_TYPER.Processor_Number](#) < 8.

Accessing GICD_IPRIORITYR0 to GICD_IPRIORITYR7 from a PE with [GICR_TYPER.Processor_Number](#) > 7 is constrained unpredictable:

- Register is RAZ/WI.
- An unknown banked copy of the register is accessed.

Attributes

GICD_IPRIORITYR<n> is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Priority_offset_3B								Priority_offset_2B								Priority_offset_1B								Priority_offset_0B							

Priority_offset_3B, bits [31:24]

Interrupt priority value from an implementation defined range, at byte offset 3. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

Priority_offset_2B, bits [23:16]

Interrupt priority value from an implementation defined range, at byte offset 2. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

Priority_offset_1B, bits [15:8]

Interrupt priority value from an implementation defined range, at byte offset 1. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

Priority_offset_0B, bits [7:0]

Interrupt priority value from an implementation defined range, at byte offset 0. Lower priority values correspond to greater priority of the interrupt.

The reset behavior of this field is:

- On a GIC reset, this field resets to 0.

For interrupt ID m , when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_IPRIORITYR< n > number, n , is given by $n = m \text{ DIV } 4$.
- The offset of the required GICD_IPRIORITYR< n > register is $(0x400 + (4*n))$.
- The byte offset of the required Priority field in this register is $m \text{ MOD } 4$, where:
 - Byte offset 0 refers to register bits [7:0].
 - Byte offset 1 refers to register bits [15:8].
 - Byte offset 2 refers to register bits [23:16].
 - Byte offset 3 refers to register bits [31:24].

Accessing GICD_IPRIORITYR< n >

These registers are always used when affinity routing is not enabled. When affinity routing is enabled for the Security state of an interrupt:

- [GICR_IPRIORITYR< \$n\$ >](#) is used instead of GICD_IPRIORITYR< n > where $n = 0$ to 7 (that is, for SGIs and PPIs).
- GICD_IPRIORITYR< n > is RAZ/WI where $n = 0$ to 7.

These registers are byte-accessible.

A register field corresponding to an unimplemented interrupt is RAZ/WI.

A GIC might implement fewer than eight priority bits, but must implement at least bits [7:4] of each field. In each field, unimplemented bits are RAZ/WI, see 'Interrupt prioritization' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

When [GICD_CTLR.DS](#)==0:

- A register bit that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.
- A Non-secure access to a field that corresponds to a Non-secure Group 1 interrupt behaves as described in 'Software accesses of interrupt priority' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

It is implementation defined whether changing the value of a priority field changes the priority of an active interrupt.

Note

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

GICD_IPRIORITYR<n> can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Distributor	Dist_base	0x0400 + (4 * n)	GICD_IPRIORITYR<n>

Accesses on this interface are **RW**.

