

## CTIPIDR4, CTI Peripheral Identification Register 4

The CTIPIDR4 characteristics are:

### Purpose

Provides information to identify a CTI component.

For more information, see 'About the Peripheral identification scheme'.

### Configuration

CTIPIDR4 is in the Debug power domain.

Implementation of this register is optional.

This register is required for CoreSight compliance.

### Attributes

CTIPIDR4 is a 32-bit register.

### Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES0																								SIZE		DES 2					

#### Bits [31:8]

Reserved, res0.

#### SIZE, bits [7:4]

Size of the component.  $\log_2$  of the number of 4KB pages from the start of the component to the end of the component ID registers.

Reads as 0b0000.

Access to this field is **RO**.

#### DES\_2, bits [3:0]

Designer, JEP106 continuation code, least significant nibble. For Arm Limited, this field is 0b0100.

This field has an implementation defined value.

Access to this field is **RO**.

## Accessing CTIPIDR4

**CTIPIDR4 can be accessed through the external debug interface:**

Component	Offset	Instance
CTI	0xFD0	CTIPIDR4

Accesses on this interface are **RO**.

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