# GICC_AIAR, CPU Interface Aliased Interrupt Acknowledge Register

The GICC_AIAR characteristics are:

## Purpose

Provides the INTID of the signaled Group 1 interrupt. A read of this register by the PE acts as an acknowledge for the interrupt.

## Configuration

This register is present only when FEAT_GICv3_LEGACY is implemented. Otherwise, direct accesses to GICC_AIAR are res0.

When GICD_CTLR.DS==0, this register is an alias of the Non-secure view of GICC_IAR. A Secure access to this register is identical to a Non-secure access to GICC_IAR.

## Attributes

GICC_AIAR is a 32-bit register.

## Field descriptions

| 31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---|---|
| RES0 | INTID |

### Bits [31:24]

Reserved, res0.

### INTID, bits [23:0]

The INTID of the signaled interrupt.

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**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

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When affinity routing is not enabled:

- Bits [23:13] are res0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are res0.

## Accessing GICC_AIAR

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_AIAR can be accessed through the memory-mapped interfaces:**

| Component | Offset | Instance |
|---|---|---|
| GIC CPU interface | 0x0020 | GICC_AIAR |

This interface is accessible as follows:

- When GICD_CTLR.DS == 0, accesses to this register are **RO**.
- When an access is Secure, accesses to this register are **RO**.
- When an access is Non-secure, accesses to this register are **RO**.

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