## **ELR\_EL3, Exception Link Register (EL3)**

The ELR EL3 characteristics are:

#### **Purpose**

When taking an exception to EL3, holds the address to return to.

## **Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to ELR EL3 are undefined.

#### **Attributes**

ELR EL3 is a 64-bit register.

### Field descriptions

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

Return address

Return address

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

#### Bits [63:0]

Return address.

An exception return from EL3 using AArch64 makes ELR\_EL3 become unknown.

The reset behavior of this field is:

• On a Warm reset, this field resets to an architecturally unknown value.

## **Accessing ELR\_EL3**

Accesses to this register use the following encodings in the System register encoding space:

# MRS <Xt>, ELR\_EL3

op0	op1	CRn	CRm	op2
0b11	0b110	0b0100	0b0000	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ELR_EL3;
```

## MSR ELR EL3, <Xt>

op0	op1	CRn	CRm	op2
0b11	0b110	0b0100	0b0000	0b001

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    if IsFeatureImplemented(FEAT_GCS) &&
GetCurrentEXLOCKEN() && !Halted() && PSTATE.EXLOCK
== '1' then
        EXLOCKException();
else
        ELR_EL3 = X[t, 64];
```

AArch32 Registers AArch64 Registers AArch32 Instructions AArch64 Instructions Index by Encoding

External Registers

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