ERXGSR_EL1, Selected Error Record Group Status Register

The ERXGSR_EL1 characteristics are:

Purpose

Shows the status for the records in a group of error records.

Accesses ERRGSR for the group of error records <n> selected by ERRSELR_EL1.SEL[15:6].

Configuration

This register is present only when FEAT_RASv2 is implemented. Otherwise, direct accesses to ERXGSR_EL1 are undefined.

Attributes

ERXGSR_EL1 is a 64-bit register.

Field descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	
S63	S62	S61	S60	S59	S58	S57	S56	S55	S54	S53	S52	S51	S50	S49	S48	S47	S46	S45	S44	S43	S42	S41	S40	S39	S
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	

S<q>, bit [q], for q = 63 to 0
When error record <m> is implemented and error record <m> supports this type of reporting:

The status for error record <m>, where m = q + (UInt(ERRSELR_EL1.SEL[15:6])Ã—64). A read-only copy of ERR<m>STATUS.V.

S<q>	Meaning
0b0	No error.
0b1	One or more errors.

Otherwise:

Reserved, res0.

Accessing ERXGSR_EL1

If ERRIDR_EL1.NUM is 0x0000 or ERRSELR_EL1.SEL[15:6] is greater than or equal to ERRIDR_EL1.NUM, then one of the following occurs:

- An unknown group of error records are selected.
- ERXGSR_EL1 is RAZ.
- Direct reads of ERXGSR_EL1 are NOPs.
- Direct reads of ERXGSR_EL1 are undefined.

Accesses to this register use the following encodings in the System register encoding space:

MRS <Xt>, ERXGSR_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0101	0b0011	0b010

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) && HaveEL(EL3) &&
SCR_EL3.FGTEn2 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() &&
IsFeatureImplemented(FEAT_FGT2) &&
HFGRTR2_EL2.nERXGSR_EL1 == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        X[t, 64] = ERXGSR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1'
&& boolean IMPLEMENTATION_DEFINED "EL3 trap priority
when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
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    else
        X[t, 64] = ERXGSR_EL1;
elsif PSTATE.EL == EL3 then
    X[t, 64] = ERXGSR_EL1;
```

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