External

Registers

AMDEVAFF1, Activity Monitors Device Affinity Register 1

The AMDEVAFF1 characteristics are:

Purpose

AArch32

Registers

Copy of the high half of the PE <u>MPIDR_EL1</u> register that allows a debugger to determine which PE in a multiprocessor system the AMU component relates to.

Configuration

It is implementation defined whether AMDEVAFF1 is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is optional.

This register is present only when FEAT_AMUv1 is implemented.

Attributes

AMDEVAFF1 is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 MPIDR EL1hi

MPIDR EL1hi, bits [31:0]

MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented Exception level.

Accessing AMDEVAFF1

AMDEVAFF1 can be accessed through the memory-mapped interfaces:

Component	Offset	Instance
AMU	0xFAC	AMDEVAFF1

Accesses on this interface are **RO**.

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