PMDEVID, Performance Monitors Device ID register

The PMDEVID characteristics are:

Purpose

Provides information about features of the Performance Monitors implementation.

Configuration

This register is present only when FEAT_PMUv3_EXT32 is implemented. Otherwise, direct accesses to PMDEVID are res0.

If FEAT_DoPD is implemented, this register is in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required from Armv8.2 and in any implementation that includes FEAT_PCSRv8p2. Otherwise, its location is res0.

Note

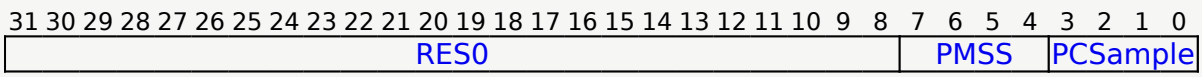
Before Armv8.2, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

Attributes

PMDEVID is a 32-bit register.

This register is part of the PMU block.

Field descriptions



Bits [31:8]

Reserved, res0.

PMSS, bits [7:4]

PMU Snapshot extension. Defined values are:

PMSS	Meaning
0b0000	PMU snapshot extension not implemented.
0b0001	PMU snapshot extension implemented.

All other values are reserved.

FEAT_PMUv3_SS implements the functionality identified by the value 0b0001.

PCSample, bits [3:0]

Indicates the level of PC Sample-based Profiling support using Performance Monitors registers.

PCSample	Meaning
0b0000	PC Sample-based Profiling Extension is not implemented in the Performance Monitors register space.
0b0001	PC Sample-based Profiling Extension is implemented in the Performance Monitors register space.
0b0010	As 0b0001, and adds support for PMU.PMPCSCTL.

All other values are reserved.

FEAT_PCSRv8p2 implements the functionality identified by the value 0b0001.

FEAT_PCSRv8p9 implements the functionality identified by the value 0b0010.

If FEAT_PCSRv8p2 is not implemented, then the only permitted value is 0b0000.

From Armv8.2, when FEAT_PCSRv8p2 is implemented, the value 0b0000 is not permitted.

From Armv8.9, when FEAT_PCSRv8p9 is implemented, the value 0b0001 is not permitted.

Accessing PMDEVID

Accesses to this register use the following encodings:

```
Accessible at offset 0xFC8 from PMU
```

- When FEAT_DoPD is implemented and !IsCorePowered(), accesses to this register generate an error response.
- Otherwise, accesses to this register are **RO**.

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