GICR_VSGIR, Redistributor virtual SGI pending state request register

The GICR_VSGIR characteristics are:

Purpose

Requests the pending state of virtual SGIs for a specified vPE.

Configuration

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICR_VSGIR are res0.

A copy of this register is provided for each Redistributor.

Attributes

GICR_VSGIR is a 32-bit register.

Field descriptions

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RES0	vPEID

Bits [31:16]

Reserved, res0.

vPEID, bits [15:0]

ID of target vPE

Writing this field is constrained unpredictable when GICR_VSGIPENDR.Busy == 1, with either the write ignored or a new query started.

Writing a value greater than the configured vPEID width behaviur is constrained unpredictable, with either:

- vPEID is treated as having an unknown valid value.
- The write is ignored.

The size of this field is implementation defined, and is specified by the GICD_TYPER2.VIL and GICD_TYPER2.VID fields. Unimplemented bits are res0.

Accessing GICR_VSGIR

GICR_VSGIR can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Redistributor	VLPI_base	0x0080	GICR_VSGIR

Accesses on this interface are **WO**.

28/03/2023 16:02; 72747e43966d6b97dcbd230a1b3f0421d1ea3d94