
PMCNTENCLR_EL0, Performance Monitors Count Enable Clear Register

The PMCNTENCLR_EL0 characteristics are:

Purpose

Disables the Cycle Count Register, PMU.PMCCNTR_EL0, and any implemented event counters [PMEVCNTR<n>](#). Reading this register shows which counters are enabled.

Configuration

External register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch64 System register [PMCNTENCLR_EL0\[31:0\]](#) when FEAT_PMUv3_EXT32 is implemented, FEAT_PMUv3p9 is not implemented and FEAT_PMUv3_ICNTR is not implemented.

External register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch64 System register [PMCNTENSET_EL0\[31:0\]](#) when FEAT_PMUv3_EXT32 is implemented, FEAT_PMUv3p9 is not implemented and FEAT_PMUv3_ICNTR is not implemented.

External register PMCNTENCLR_EL0 bits [63:0] are architecturally mapped to AArch64 System register [PMCNTENCLR_EL0\[63:0\]](#) when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMCNTENCLR_EL0 bits [63:0] are architecturally mapped to AArch64 System register [PMCNTENSET_EL0\[63:0\]](#) when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented.

External register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register [PMCNTENCLR\[31:0\]](#).

External register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register [PMCNTENSET\[31:0\]](#).

This register is present only when FEAT_PMUv3_EXT is implemented. Otherwise, direct accesses to PMCNTENCLR_EL0 are res0.

PMCNTENCLR_EL0 is in the Core power domain.

Attributes

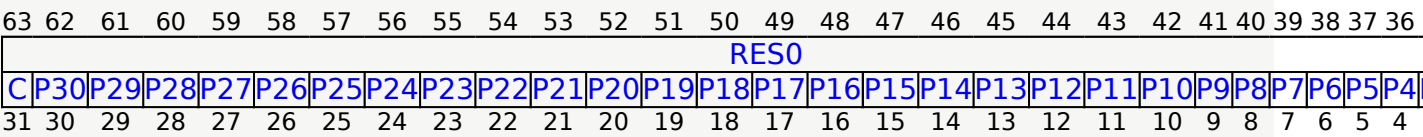
PMCNTENCLR_EL0 is a:

- 64-bit register when FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented
- 32-bit register otherwise

This register is part of the [PMU](#) block.

Field descriptions

When FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3p9 is implemented or FEAT_PMUv3_ICNTR is implemented:



Bits [63:33]

Reserved, res0.

F0, bit [32]

When FEAT_PMUv3_ICNTR is implemented:

PMU.PMICNTR_EL0 disable. On writes, allows software to disable PMU.PMICNTR_EL0. On reads, returns the PMU.PMICNTR_EL0 enable status.

F0	Meaning
0b0	PMU.PMICNTR_EL0 disabled.
0b1	PMU.PMICNTR_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **W1C**.

Otherwise:

Reserved, res0.

C, bit [31]

PMU.PMCCNTR_EL0 disable. On writes, allows software to disable PMU.PMCCNTR_EL0. On reads, returns the PMU.PMCCNTR_EL0 enable status.

C	Meaning
0b0	PMU.PMCCNTR_EL0 disabled.
0b1	PMU.PMCCNTR_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **W1C**.

P<m>, bit [m], for m = 30 to 0

[PMEVCNTR<m>_EL0](#) disable. On writes, allows software to disable [PMEVCNTR<m>_EL0](#). On reads, returns the [PMEVCNTR<m>_EL0](#) enable status.

P<m>	Meaning
0b0	PMEVCNTR<m>_EL0 disabled.
0b1	PMEVCNTR<m>_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When $m \geq \text{NUM_PMU_COUNTERS}$, access to this field is **RAZ/WI**.
- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **W1C**.

Otherwise:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
C	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4

C, bit [31]

PMU.PMCCNTR_EL0 disable. On writes, allows software to disable PMU.PMCCNTR_EL0. On reads, returns the PMU.PMCCNTR_EL0 enable status.

C	Meaning
0b0	PMU.PMCCNTR_EL0 disabled.
0b1	PMU.PMCCNTR_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **W1C**.

P<m>, bit [m], for m = 30 to 0

[PMEVCNTR<m>_EL0](#) disable. On writes, allows software to disable [PMEVCNTR<m>_EL0](#). On reads, returns the [PMEVCNTR<m>_EL0](#) enable status.

P<m>	Meaning
0b0	PMEVCNTR<m>_EL0 disabled.
0b1	PMEVCNTR<m>_EL0 enabled.

The reset behavior of this field is:

- On a Warm reset, this field resets to an architecturally unknown value.

Accessing this field has the following behavior:

- When m >= NUM_PMU_COUNTERS, access to this field is **RAZ/WI**.
- When SoftwareLockStatus(), access to this field is **RO**.
- Otherwise, access to this field is **W1C**.

Accessing PMCNTENCLR_EL0

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

Accesses to this register use the following encodings:

When FEAT_PMUv3_EXT64 is implemented, or FEAT_PMUv3_ICNTR is implemented or FEAT_PMUv3p9 is implemented

[63:0] Accessible at offset 0xC20 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When FEAT_PMUv3_EXT32 is implemented and SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

When FEAT_PMUv3_EXT32 is implemented, FEAT_PMUv3_ICNTR is not implemented and FEAT_PMUv3p9 is not implemented

[31:0] Accessible at offset 0xC20 from PMU

- When DoubleLockStatus(), or !IsCorePowered(), or OSLockStatus() or !AllowExternalPMUAccess(), accesses to this register generate an error response.
- When SoftwareLockStatus(), accesses to this register are **RO**.
- Otherwise, accesses to this register are **RW**.

[AArch32
Registers](#)

[AArch64
Registers](#)

[AArch32
Instructions](#)

[AArch64
Instructions](#)

[Index by
Encoding](#)

[External
Registers](#)

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