GICR_INMIR<n>E, Non-maskable Interrupt Registers for Extended PPIs, x = 1 to 2., n = 1 - 2

The GICR_INMIR<n>E characteristics are:

Purpose

Controls whether the corresponding Extended PPI has the non-maskable property.

Configuration

This register is present only when FEAT_GICv3p1 is implemented and FEAT_GICv3_NMI is implemented. Otherwise, direct accesses to GICR_INMIR<n>E are res0.

When GICR_TYPER.PPInum is `0b0000` or GICD_TYPER.NMI is 0, these registers are res0.

A copy of this register is provided for each Redistributor.

Attributes

GICR_INMIR<n>E is a 32-bit register.

Field descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	1
nmi31	nmi30	nmi29	nmi28	nmi27	nmi26	nmi25	nmi24	nmi23	nmi22	nmi21	nmi20	nmi19	nmi18	nmi17	nm

nmi<x>, bit [x], for x = 31 to 0

Non-maskable property.

nmi<x>	Meaning
`0b0`	Interrupt does not have the non-maskable property.
`0b1`	Interrupt has the non-maskable property.

This bit is res0 when the corresponding interrupt is configured as Group 0.

The reset behavior of this field is:

- On a GIC reset, this field resets to `0`.

If affinity routing is disabled for the Security state of an interrupt, the bit is res0.

Accessing GICR_INMIR<n>E

Bits corresponding to unimplemented interrupts are RAZ/WI.

When GICD_CTLR.DS==0, bits corresponding to Group 0 and Secure Group 1 interrupts are RAZ/WI to Non-secure accesses.

Note

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

GICR_INMIR<n>E can be accessed through the memory-mapped interfaces:

Component	Frame	Offset	Instance
GIC Redistributor	SGI_base	`0x0F80` + (4 * n)	GICR_INMIR<n>E

Accesses on this interface are **RW**.

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