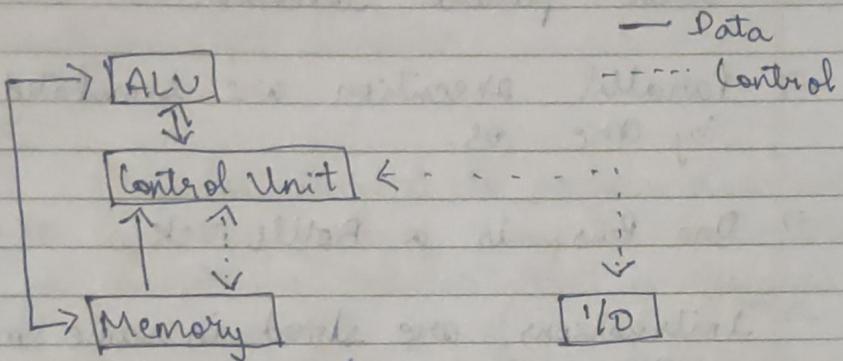


Assignment - 1

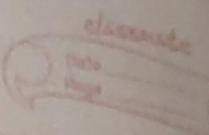
1) Von-Niemann Architecture



- All parts are controlled by control unit CPU & connected together by Bus.
- Data can pass through bus in Half Duplex mode To and from CPU.
- Memory holds programs & data known as stored program concept.
- Memory is split to small cells with the same size. Their original numbers are called address numbers.

Advantages:

- Control Unit gets data & instruction in the same way from one memory. It simplifies design & development of the control unit.



Dissadvantages:-

- Serial instructions processing does not allow parallel execution.
- Parallel execution are simulated later by one OS.
- One Bus is a Bottleneck.
- Instructions are stored in same memory as one data can be accidentally overwritten by an error in a program.

2) Difference between CISC & RISC

CISC :-

CISC was developed to make compiler development easier & simple. CISC is Complex Instruction set Computer.

RISC:-

RISC is designed to perform a smaller number of a types of computer instructions. It is a Micro Processor that is designed to perform smaller no of computer instructions. RISC is Reduced Instruction Set Computer.

C1SC

RISC

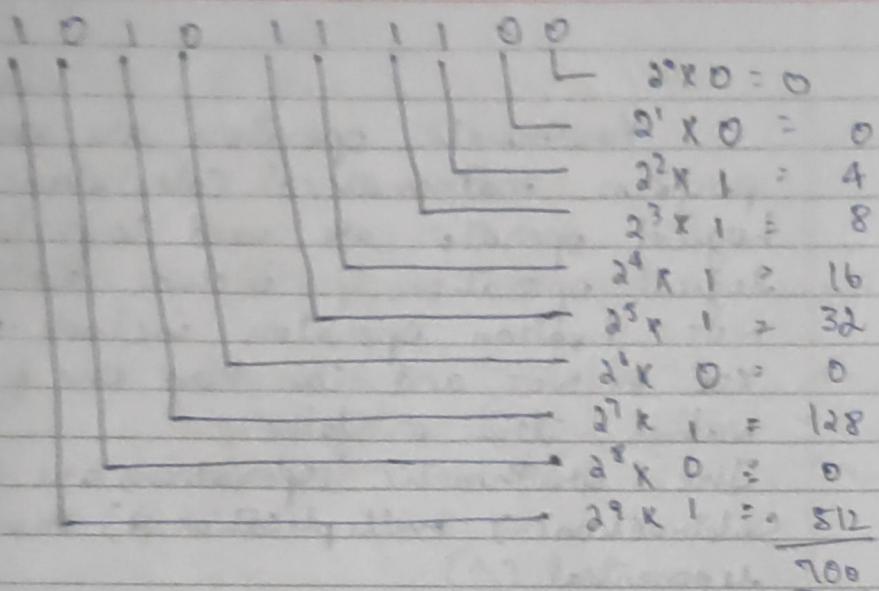
- More set of Instructions Lesser set of Instructions.
 - More addressing mode Lesser addressing mode.
 - Minimum amount of RAM More amount of RAM.
 - Focus is on hardware to optimise. Focus is on software to optimise.
 - High Power Consumption Low Power Consumption
 - Single Register Set Multiple Register Set.
 - Less Pipelined Highly Pipelined.

3) List the numbering systems available & explain briefly.

- Binary Number system (Base-2)
 - Octal Number system (Base - 8)
 - Decimal Number system (Base - 10)
 - Hexadecimal number system (Base - 16)
-
- The Binary number system is used to store one data in computer.
 - Octal number system is that it has fewer digits when compared to other systems. Hence fewer computational errors.
 - Decimal number system is one system that we use in daily life.
 - The hexadecimal number system is used in computers to reduce one large sized strings of binary system.

Conversion :

To convert a number from one system to another number system, we first convert it to decimal system. & then one following process is done.



$$1010111100_2 = 700_{10}$$

$$\begin{array}{r}
 16 \boxed{700} \\
 16 \boxed{43} - \boxed{12} \uparrow - (c) \\
 \hline
 \boxed{2} - \boxed{11} \quad - (b)
 \end{array}$$

$$700_{(10)} = 2BC_{(16)}$$

$$\begin{array}{r}
 2 \boxed{700} \\
 2 \boxed{350} - 0 \\
 2 \boxed{175} - 0 \\
 2 \boxed{87} - 1 \\
 2 \boxed{43} - 1 \\
 2 \boxed{21} - 1 \\
 2 \boxed{10} - 1 \\
 2 \boxed{5} - 0 \\
 2 \boxed{2} - 0 \\
 1 - 0
 \end{array}$$

$$(1010111100)_2$$

Arithmetic operators are used to perform mathematical calculations.

Logical operators are used to perform logical operations & include AND, OR or NOT. Boolean operators include AND, OR, XOR or NOT and can have one of 2 values, true or false.

The arithmetic operations are Addition (+), Subtraction (-), multiplication (*) or division (/) and exponential (^).

The 3 common logical operators are:-

&& - AND

|| - OR

! - NOT

The logical operators are often used to create a test expression that controls program flow. This type of expression is also known as Boolean expression because they create a Boolean answer or value when evaluated.

TRUTH Tables

Logical relations:-

x	y	$x \text{ and } y$	$x \text{ or } y$
false	false	false	false
false	true	false	true
true	false	false	true
true	true	true	true

x	not x
false	true
true	false

Operator	Meaning	Example	Result
& &	Logical AND	$(5 > 2) \& \& (5 > 3)$	false
	Logical OR	$(5 > 2) (5 > 3)$	true
!	Logical NOT	!(5 > 2)	true

- 3) Explain ARM-7 architecture.
- ARM processor is a 32 bit architecture.
 - 16 bit Thumb instruction set.
 - It is load/store architecture.
 - Fixed length 32 bit inst.

Data Types

- 8 bits signed & unsigned bytes.
- 16 bits signed & unsigned half word.
- aligned on 2 byte boundaries.
- 32 bit signed & unsigned words, aligned on 4 byte boundaries.
- ARM inst are all 32 bit words.
- ARM inst support floating-point values.
- Internally all RAM op's are on 32-bit operands, hence shorter data types are only supported by data transfer inst. When a byte is loaded from memory it is zero or extended to 32 bit.

- 4) Write a neat diagram explain programming model for Thumb.

A)

Processor modes

CPSR [4:0]	mode	use	register
10000	User	Normal user mode	user
10001	F10	Processing fast int	- f10
10010	IRQ	Processing std int	- irq
10011	SVC	→ 11 → SW → 11 ←	- svc
10111	Abort	P Memory fault	- abt
11011	Undf	Handling undefinst	- und
11111	System	Running privileged	- user

- Privileged mode

- Most programs operate in user mode. ARM has other privileges operating modes which are used to handle exceptions, supervisor calls and system mode.

- Supervisor mode

- Having some protective privileges.
- System level function can be accessed through specified supervisor calls.
- Usually implemented by software interrupt.

ARM has 37 reg all of which are 32 bits

- Prog counter
- Current prog status reg.
- 5 dedicated saved prog status reg.
- 50 general purpose reg.

User	FIQ	IRQ	Svc	Undefined	Abort
R0					
R1	User				
R2	modes	User mode		User mode	User mode
R3	R0-R7	R0-R12	User mode	R0-R12	R0-R12
R4	R11 &	R11-R12			
R5	Usr	R15	R0-R12	R15 &	R15 &
R6		CPSR	R15 & CPSR	CPSR	CPSR
R7					
R8	R8				
R9	R9				
R10	R10				
R11	R11				
R12	R12	R13 (Sp)	R13 (Sp)	R13 (Sp)	R13 (Sp)
R13	R13 (Sp)	R14 (Sp)	R14 (Sp)	R14 (Sp)	R14 (Sp)
R14	R14 (Sp)	R15 (Sp)	R15 (Sp)	R15 (Sp)	R15 (Sp)
R15					
CPSR		CPSR	CPSR	CPSR	CPSR

- 5) ARM Co-processor Supports floating point value
Programming model for ARM7.
Each instruction can be viewed as performing
a defined transformation of the state.
- (*) Visible Register
 - (*) Invisible Register
 - (*) System Memory
 - (*) User Memory

Processor modes explained in previous page
Most programs operate in user mode
ARM has other privileges operating mode
which are used to handle exceptions, supervisor
calls & system mode.

→ More access rights to memory than
Co-processors.

→ Current access rights to memory
System & Co-processors.

→ Current operating mode is defined
by CPSR [4:0]

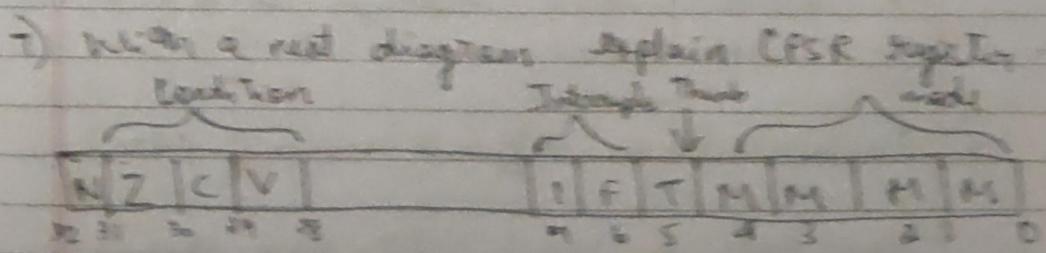
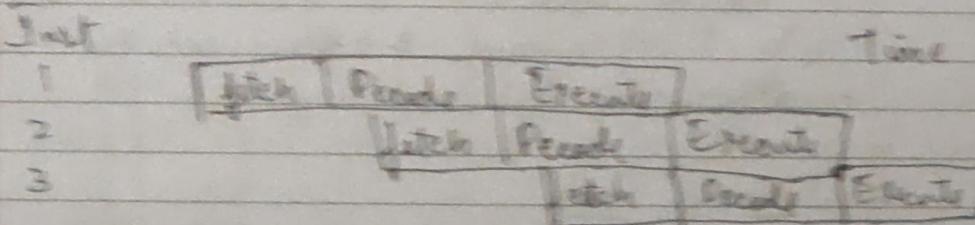
- Q) Explain 3 stage pipeline of RISC
- The process of fetching the next instruction while one current instruction is being executed is called a pipelining.
- Pipelining is supported by forward to forward the speed of the execution.
 - The 3 stage used in pipeline are -
 - fetch, decode & execute.

Fetch - Init. fetched from memory.

Decode - Decoding of the next instruction.

Execute - Execute the inst.

If above 3 stages of execution are overlapped we will achieve higher speed of execution.



Condition Bits.

N = Is set to bit 31 of the result of inst.

If this result is regarded as a 32's complement

complement signed integer, then $N=1$
if result is negative & $N=0$ if it is
positive or zero.

Z : Is set to 1 if the result of int is zero
& to 0 otherwise.

This often indicates an equal result from a
comparison.

C : It is set in one of 4 ways.

- for an addition c is set to 1 if addition
produced a carry & to 0 otherwise
- for subtraction is set to 0, if subtraction
produced a borrow & to 1 otherwise.
- C is set to last bit shifted out of the
value by shifter.

V : Is set in one of 2 ways:

- For an addition or subtraction, V is set
to 1 if signed overflow occurred.
- Otherwise left unchanged.

Interrupt bits

- J - Disables IRQ interrupts when it is set.
- F - Disables F1A interrupts when it is set.
- T - Thumb mode.

2) Explain seven different modes of ARM.

- User mode is usual ARM prog execution
state and is used for executing most app prog.
- Fast interrupt (F1A) - mode supports a data
transfer or channel process.
- Interrupt (IRQ) mode is used for general purpose

Interrupt handling.

- Supervisor mode is protected mode for OS.
- Abort mode is entered after a data or inst prefetch abort.
- System mode is a privileged user mode for OS.
- Undefined mode is entered when an undefined inst is executed.

mode

user	
fast interrupt	
Interrupt	
Supervisor	
Abort	
System	
undefined	

mode identifier

user	
firq	
irq	
IVC	
abt	
bys	
und	

Q) Explain nomenclature in ARM.

A) ARM was originally from Acorn computers Ltd - first RISC processor for commercial use.

ARM7 TDMI processor.

32 bit processor advanced machine

- ↑ → Thumb advanced machine
- ⊕ → Debug extension.
- ⊖ → Enhanced multiplier.
- ⊖ → In circuit Emulation.

ARM {x3}-{y3} - {z3} TDMI {F3}{S3}{C3}{S3}

- x → series
- y → memory management unit
- z → cache

T → thumb 1 bit decoder.

S → JTAG Debugger

M → fast multiplier.

I → Embedded I_C

E → Enhanced Inst for DSP.

J → SART acceleration by Jazelle

S → synthesizeable version.

10) What is JTAG? Explain JTAG's standards.

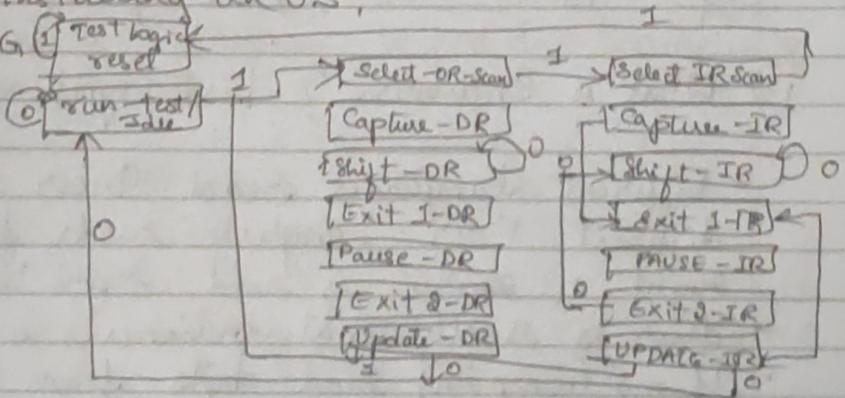
- A) JTAG has become a std in embedded sys and it is available in nearly every microcontroller & FPGA on market.
- If we have programmed a microcontroller, there is a strong chance that we have used JTAG of the emulated std.
 - JTAG is an integrated method for testing interconnects on PCB that are implemented at IC level.
 - It used to be case that testing a board with test bench. However as pin density increased & as ball-grid array (BGA) packaging became more prevalent a new method of testing was required.
 - A solution was needed which tested all interconnects b/w multiple IC's.
 - In 1980's boundary scan was developed and standardized in IEEE. This std which became known to developers and engineer as JTAG.

11 What is Single Tasking? Give Example of processor applications.

A) Single tasking means doing one task at a time with as little distraction & interruption as possible.

Single Microcontroller are known as computer on chip. They are designed to perform a single task only because its processing power as well as memory not suitable for installing an OS.

(10) JTAG (Test logic reset)



ii) What is MMU? Why MMU is required?

- A) i) Memory Management unit is a computer h/w component that handles all memory & caching operations associated with processor.
- In other words the MMU's responsible for all aspects of memory management.
- It is usually integrated into processor although in some systems it uses a separate IC chip.
- The work of MMU can be divided into 3 categories.
 - (i) Hardware memory management
 - (ii) OS memory management
 - (iii) App memory management

MMU required for:-

- Allocate & deallocate memory before and after process execution.
- To keep book of track of used memory space by processes.
- To minimize fragmentation issues.
- To proper utilization of main memory.

Eg:- ARM, VAX, IBM systems.

13) What is Endianess? List types : give ex.

- Different languages read their text in different order. English reads from left to right & Arabic is read right to left.
- This is exactly what endianess is for computers.
- If my computer reads bytes from left to right and other computer reads from right to left were going to have issues when we need to communicate.
- Endianess means that the bytes in computer memory are read in certain order.

There are 2 types

1) Little endianess

: last byte of binary rep. of multi-byte data types are stored first

2) Big endianess

: first byte of binary rep. of multi-byte data type is stored first.

Ex:-

0x01234567 will be stored as.

			0x100 67	0x101 45	0x102 23	0x103 01	

little endian.

			0x100 01	0x101 23	0x102 45	0x103 67	

Big endian

- 14) Write a C program to find the endianess of given number.

n)

```
#include < stdio.h >
```

```
int main()
```

```
{
```

```
    unsigned int x = 0x76543210;  
    char *c = (char *)&x;
```

```
    if (*c == 0x10)
```

```
{
```

```
        printf ("underlying arch is little  
                endian");
```

```
}
```

```
    else
```

```
{
```

```
        printf ("Big endian");
```

```
{
```

```
    return 0;
```

```
}
```

15) Explain following.

- ① Bit :- It is smallest unit of information and can be stored in a computer. Bits in computer are grouped to form a larger unit of information.
- 2) Byte :- A byte is a combination of eight bits. Eight bits represent a character & is called a byte.
- 3) Nibble :- A nibble is a combination of four bits, in other words a nibble is half a byte.
- 4) Word :- A word is a combination of 16 bits, 32 bits or 64 bits depending on computer. 16 is known as quad word.

Q 16) Explain word align & half word in ARM memory.

- A)
- Different processors have different definition of words for 32 bit processors a word is 32 bit.
 - A name implies, a halfword is a 16 bit.
 - Word alignment :-
The stored addresses are adjacent & can be divided by 1, that is last 2 digits are 00.
 - Half word alignment:-
The stored addresses are adjacent & can be divided by 2. last digit is 0

- In the thumb state, the value of R15 is always divisible by 2, which is the lowest bit of R15 register always zero.

18) Explain the following addressing modes in RAM.

A) When data to be read from or store in 2 or more addresses field may have one or more than one address.

- * Three address Instructions.
- * Two address Instructions
- * One - u - u -
- * Zero - u - u -

One address Instructions:-

This uses an implied accumulator or reg for data manipulation & others is in the Register & memory location.

Implied means that the CPU already knows that one operand is in one accumulator so there is no need to specify it.

Eg:- LDR addr.

Acc 2- (addr)

Two address instructions:-

Here 2 address can be specified in one instruction. In the one address instructions the result was stored in the accumulator.

The result can be stored in different location i.e Register or memory location. But requires more number of bit to represent one address.

Eg:- mov R1, R2
R1,L{R2}

Three address Instructions :-

This has 3 address field to a register of memory location.

Program created are much short in size but number of bits per instruction increase. These inst make creation of prog easier but doesn't mean program will run faster.

Eg:- APP , R3 , R1 , R2
 $R_3 = R_1 + R_2$

20) Explain LPC 2148 MC bPIO pins.

bPIO - bPIO A 32 bit register used to select one functions of pins in which one user needs it to operate.

There are 4 functions for each pin of one controller, which one first function is bPIO.

It means that one pin can either act as input or output with no specific function.

* IOPIN

This register provides the value of port pins that are configured to perform only digital functions.

In register until give one logic value of one PIN . regardless of pin is configured for input or output as bPIO of an alternate digital functions.

* IOSET

This register is used to produce a

(ii) high level output at one port pins
configured as GPIO in an output mode.
Writing 1 produces a HIGH level at
corresponding port pins writing 0 has no effect

IOPDR

This word accessible register is used to control one direction of pins when they are configured as GPIO port pins. Direction bit for any pin must be set according to pin function.

IOLCR

This is used to produce a low-level output at port pins configured as GPIO in an output mode.

1 produces low level at PIN
0 has no effect.

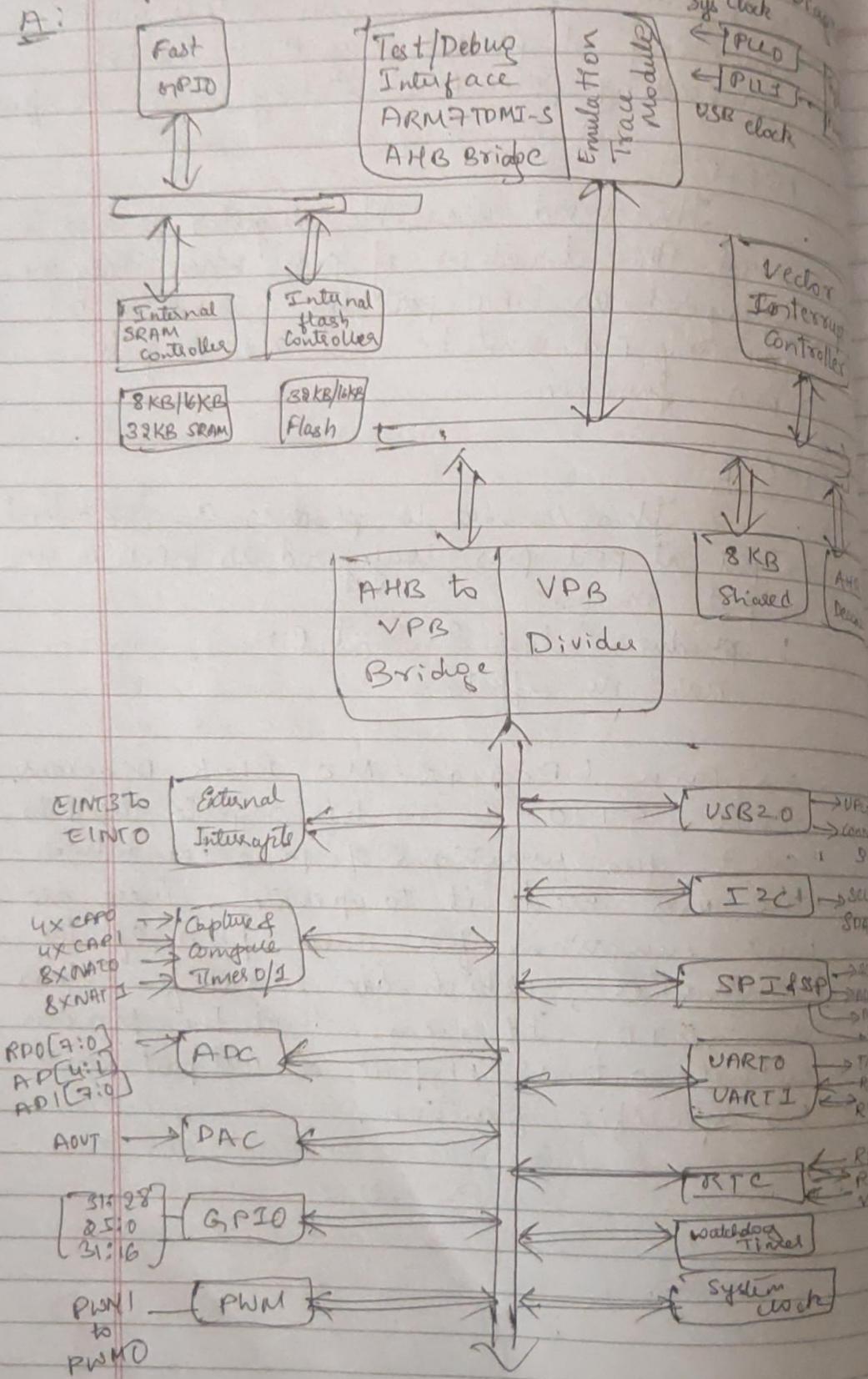
Q2

Explain LPC2148 Mc Block Diagram.
Ans: GPIO - GPIO A 32-bit register used to select the functions of pins in which the user needs it to operate. There are four functions for each pin of the controller, which the first function is GPIO. It means that the pin can either act as input or output with no specific function.

P.T.O.

Ques. Explain LPC 2148 Microcontroller

A:



- Q1) Write a neat diagram & explain band rate & bit rate. Explain calculations.

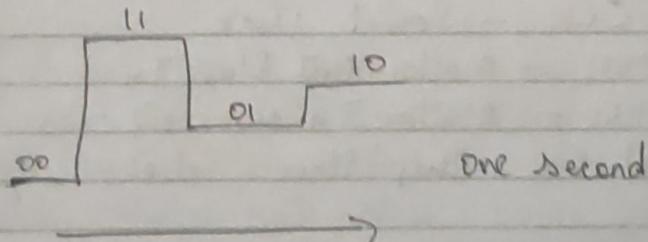
Band :- signal change per second.

Bit :- How many bits can be sent per unit time.

Bit rate is controlled by band & no. of signal levels.

Band rate:

- No. of times lines changed per second.
- Let Band rate be 4.
- Bit rate = 8 bits / sec
- ∴ Bit rate = $\times 2$ Band rate in this eg.



1000 signal units are sent per second, find Band rate & Bit rate.

1 bit \rightarrow 1 symbol

Bit rate = Band rate

1000 = Band rate.

$$\text{Bit rate} = 1000 \times 1 = 1000 \text{ bps.}$$

∴ Bit rate is 'b'

Band rate is 's'

General formula

$$b = s \times n$$

If $n=1$, Band rate = Bit rate
 $n=4$, Bit rate = $4 \times$ Band rate

22) With neat diagram, Explain one working & features of SPI protocol.

A) SPI is serial communication interface specification used for short distance communication, primarily in embedded system.

SPI is full duplex with master-slave architecture usually with single master.

SPI is 4 wire serial bus.

SCLK - Serial Clock

MOSI - Master Out Slave In

MISO - Master In Slave out

CS/SS - Chip/Slave Select.

23) In SPI neat timing diagram, explain CPHA & CPOL wage.

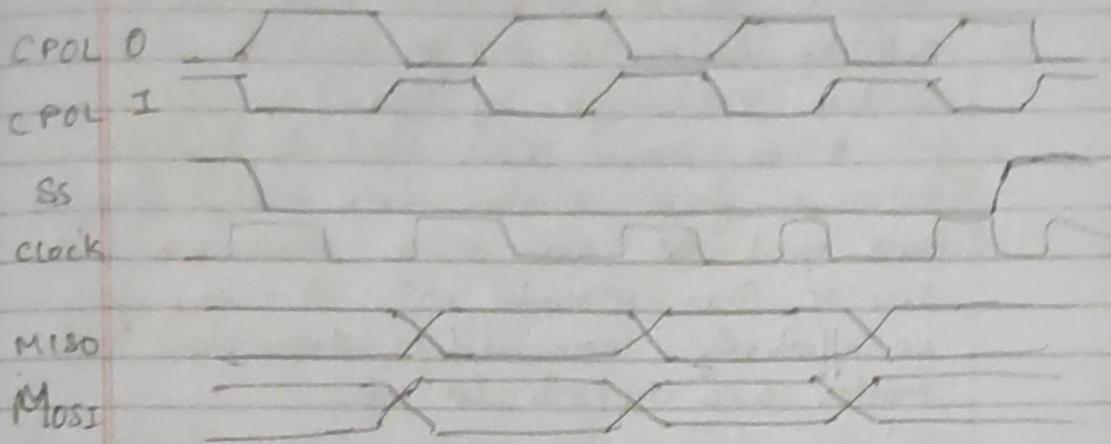
A) CPOL determines the polarity of clk clock

CPOL = 0 pulse of 1

CPOL = 1 pulse of 0

CPHA = 0. But change data on trailing edge of preceding clock cycle. in capturing data in the leading edge of clock cycle

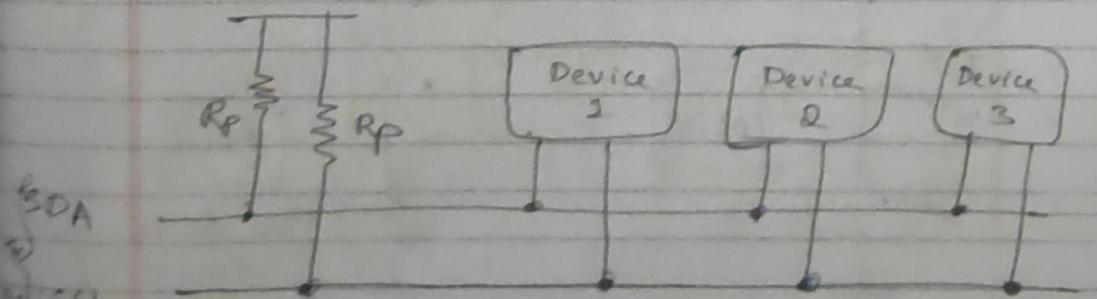
$CPHA=1$ Out side changes data, in leading edge of clock cycle, while In side captures data on trailing edge of clock cycle.



24) Explain working of I₂C with neat diagram.

- A) + Half duplex serial communication.
- + Synchronous communication protocol
- + Only 2 common bus lines.
- + Adjustable data rate speeds.
- + Simple mechanism for validation of data transfer.
- + Uses 7 bit addressing system to target specific device on Bus.

+ V_{CC}



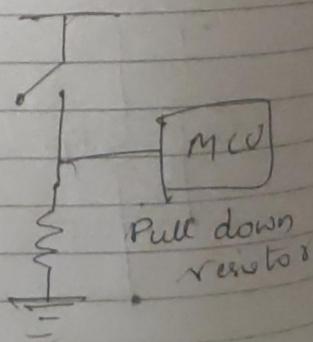
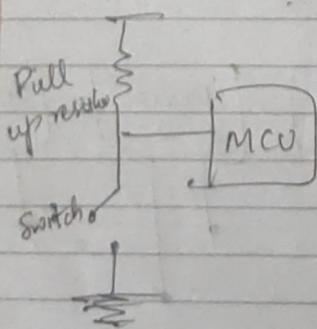
Both I₂C bus line (SDA, SCL) are open drain drivers. It means that a driver on I₂C network can drive SDA & SCL high, so a pull up resistor is need for each bus line to keep them high by default.

When master device wants to transfer data or from a slave device it specifies particular slave device address on the line & then proceeds with the transfer so effectively communication takes place between master device & particular slave.

- 25) Explain pull up & pull down resistor.

A) Pull up Resistor

It is used to establish an additional loop over the critical components while making sure that voltage is well defined even when switch is open. It is used to ensure that a wire is pulled to a high logical level in absence of an input signal. Pull up resistor with a fixed value was used to connect voltage supply & a particular pin in digital circuit.



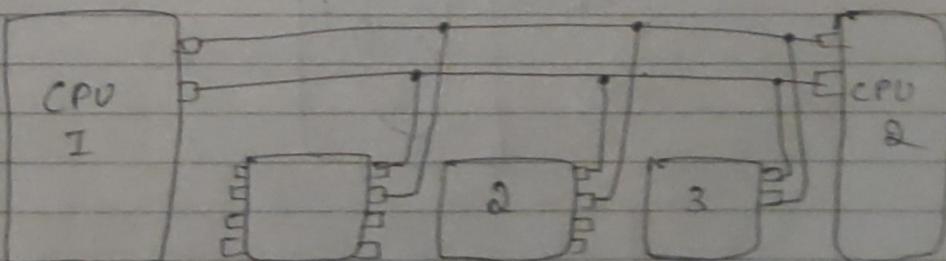
Pull-down Resistor

It is used to ensure that input to logic systems settle at expected logic level whenever the external device are disconnected or of high impedance.

It ensures that the wire is at a defined low logic level when there are no active connections with other device is connected.

a) Arbitration in I₂C

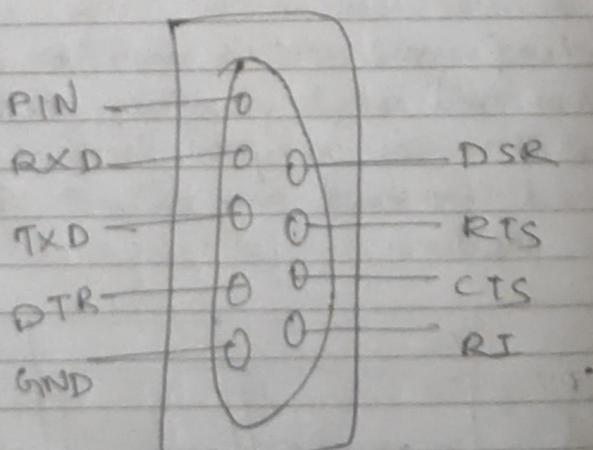
- A) → Bus arbitration occurs when 2 or more master start a transfer at same time.
- + More than one devic can be active in this system.
- + When MC VI gives a start condition & sends address are slave will listen. If the address does not match the CPU 2, this device has to hold back any activity too until the bus becomes idle again after a stop condition.
- + As long as 2 MCUs monitors what is going on bus and as long as they are aware that a transaction is going on because that last issued command was not a stop there is no problem.



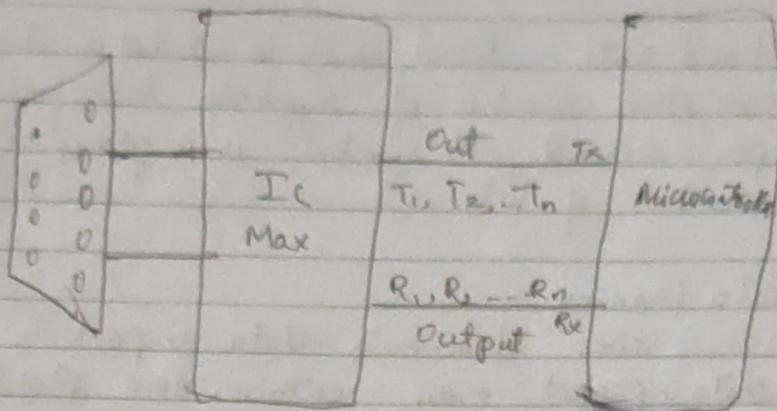
Q8) Explain working of DB9 pins & handshaking w/ an modem

<u>PIN</u>	<u>Signal</u>	<u>Signal Name</u>	<u>DB9 pin number</u>
1	RxD	Data came directed	In
2	TxD	Receiver data + Txdata	In
3	DTR	Data terminal ready.	Out
5	GND	Ground	-
6	DSR	Data set ready	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

Handshaking modem is what occurs when one receiving modem answers one phone call and 2 modems begin to communicate



Ques. Explain RS 232 connection with microcontroller



Several devices collect data from sensors & need to send it to another unit like a computer for further processing.

Serial communication on other hand use only one or 2 data lines transfer data is generally used for long distance communication - In serial communication one data is sent as one bit at a time.

An important parameter considered while interfacing signal port is Band rate which is speed at which data is transmitted serially.

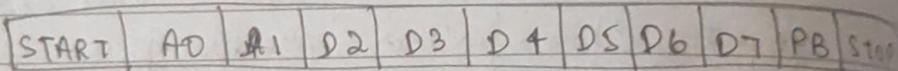
Microcontrollers can be set to transfer and receive signal data at different band rate using software int.

30) Explain frame format in UART communication

- i) Band rate - Band rate is a data transfer rate to one number of symbols transferred per second. A symbol is a group of a fixed number of bits.

Data framing :-

UART transmits data in packets. Each data packet may contain one start bit followed by 8 to 9 data bits, an optional parity bit & 1 or 2 stop bits.



The UART receives the data from the data bus and this data are being sent by CPU, memory or microcontroller.

Start bit:-

When there is no data transmission the UART Tx line is held at high voltage. This transition acts as start bit. When the receiving UART detects one TTL voltage transition, it begins reading the data frame at freq of band rate.

Data frame:-

The data bits are usually 8 bits in number. If no parity bit is used it can be a bit long. In general case the LSB of data is transmitted first.

Parity bits:-

This is used to indicate the change in data during tx. The reasons from one change in data is mismatched baud rates, electro magnetism of long distance data transfer.

Stop bits:-

To mark one end of data packet the sending UART drives the data transmission line from a low voltage to high voltage from a minimum of 2 bit duration.

- 3) Explain difference between

Serial

- Data is transmitted bit after bit in a single line
- Data congestion takes place
- Low speed transmission
- Implementation of serial links is not an easy task
- No cross talk problem

Parallel

- Data is transmitted simultaneously through group of lines

- No data congestion place

- High speed transmission

- Parallel data links are easily implemented as hardware

- Cross talk creates interference between parallel lines

Analog

- Tx modulated signal is analog in nature
 - Noise immunity is poor for FM & PM
 - Coding is not possible
 - FDM is used for multiplexing
 - Analog modulation system are AM, FM, PM, PAM, PWM
- Tx signal is digital i.e. Train of pulses
- Noise immunity is excellent.
- Locking technique is used to detect & correct error.
- TDM is used for multiplexing
- Digital modulation system are PCM, DPCM, ADM, PCM

Digital

Synchronous

- Communicated in real time
- Creates interrupts in a working
- Faster
- No overhead of extra start & stop bit
- Uses constant time interval

Asynchronous

- Communicated in non-real time
- Eliminates Interrupts
- Slower
- User starts by start bit
- User generates irregular time intervals

- Used in chat rooms used in emails.