27 DIBL effect compensation of self-biased CMOS voltage reference using adaptive V_{GS} control

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Abstract

Design and issues in the composition of ultra-low-power CMOS voltage references (CVRs) are needed for energy constrained micro-systems like brilliant sensors, wearable gadgets, and embed chips. Whereas conventional band gap voltage references (BGRs) are based on bipolar junction transistors (BJTs) that delay the reduction of the supply voltage (VDD) and the power consumption and usually require large resistors, which extend the size of the chip. That's why CVRs are much more appropriate for ultra-low-power applications; however, they must resolve a wide range of (V_{DD}) and noise, having good line sensitivity (LS) and power supply rejection ratio (PSRR). These strategies can create a more complicated design, which is to be stressed, power consumption, or result in circuit overhead. The self-biased CVR (SBCVR) is the result of a business idea that is being refreshed, where the bias current (I_B) is conducted from the reference voltage. However, the SBCVR's performance could be influenced by the gate leakage current (I_G), which short-circuits the source and substrate terminals of the transistor under biasing, which can lead to linearity loss and noise performance degradation. The study introduces a new technique for addressing the DIBL effect by means of adaptive gate-source voltage (V_{GS}) control. This solution not only reduces power consumption and complexity in design, but also promises to push performance in ultra-low-power up toward their full potential.

Keywords: Adaptive VGS control, drain induced barrier lowering with adjustment, line variation response, power supply noise rejection

Introduction

In modern ultra-low-power electronic systems like Internet of Things (IoT) devices [1, 5–13], wearables and energy-limited sensors, the coefficient reference voltage is of utmost importance for the device to operate stably and efficiently. Conventional voltage references, such as bandgap voltage references (BGRs) [1–4] and self-biased CMOS voltage references (SBCVRs), tend to suffer from low power efficiency, compactness, and fluctuation in performance due to varied supply voltages. The barrier lowering effect (DIBL) is also a significant factor in the de termination of LS [14] and PSRR, which limit their efficiency in environments with unstable supply voltages. This study dictates a low-power CMOS voltage reference (CVR) that in degrades a DIBL compensation method by which these issues can be solved. The suggested topological structure is characterized by controlling the gate source voltage (V_{GS}) adaptively to guide the bias transistor dynamically, thus reducing the bias current dependency on the supply voltage fluctuations.

A. Effects of DIBL

Effects of drain-induced barrier lowering are quite substantial to a circuit since they produce unstable reference volt ages, high sensitivity to the line and lower values for PSRR. DIBL is an effect encountered in MOSFET transistors; an increase in (V_{DS}) has its effect of bringing down (V_{TH}). Without DIBL compensation Figure 27.1(a), the (V_{TH}) of transistor M1 de creases as the supply voltage (V_{DD}) increases,

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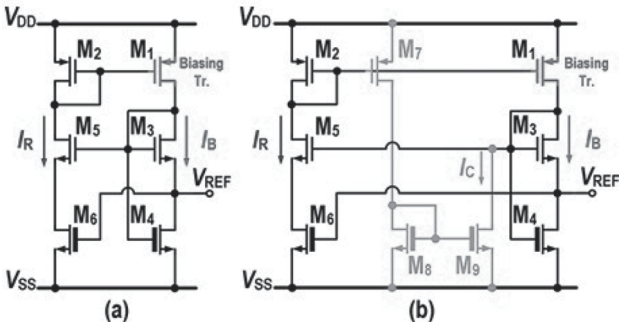

Figure 27.1 (a) Circuit without DIBL compensation. (b) Circuit with DIBL Compensation performance of the circuit [10, 11]
Source: Author

thus causing variations in the bias current (I_B), which affects overall performance.

This may also lead to an unstable reference voltage that is difficult to maintain as well. While the increased line sensitivity may make the circuit more prone to noise and interference, reduced PSRR would lead to a decrease in the circuit's power supply noise rejection. This may become serious issues with lower accuracy, increased errors, and decreased reliability. However, with DIBL compensation Figure 27.1(b), a compensation transistor (M8) senses the (V_{DD}) variations and generates a compensation current (I_C) that stabilizes the bias current (I_B) by adjusting the gate-source voltage (V_{GS}) of M1. The compensation mechanism will help the circuit to achieve a stable reference voltage, decrease line sensitivity [14], and improve PSRR, hence making it less susceptible to power supply noise and interference. The compensation circuit of DIBL monitors the (V_{DD}) voltage and generates a compensation current (I_C) proportional to the 2 (V_{DD})voltage. This compensation current is used to adjust the (V_{GS}) voltage of M1, which in turn stabilizes the (I_B) current. Therefore, by stabilizing the I_B current, the circuit maintains a stable reference voltage even with the presence of (V_{DD}) variations. Consequently, the circuit has better performance overall, and the output will remain stable regardless of power supply variation. Therefore, the circuit becomes more reliable, accurate, and robust, which is a very critical parameter in many applications such as these mentioned elements.

Literature Review

The BGRs for energy harvesting IoT devices, authors proposed a 58-ppm/°C 40-nW BGR that operates at a power supply volt age as low as 0.5 V which is a prototype for energy harvesting IoT devices [1]. This design is aimed mainly at curbing power consumption without compromising the temperature stability feature that it gives. Besides, it can specifically be useful for energy mismatched devices to the battery pro duction line that need both low power and low voltage. The authors made this possible by improving the bandgap-core and especially by carefully selecting the necessary energy hungry components to minimize their use and hence reduce the amount of energy consumed power.

An all-in-one bandgap voltage and current reference, that consumes less power and does not need amplifiers which is less than 200 nW, was designed [2]. This design is a solution that eliminates the need for amplifiers, and in addition to that, it is energy-saving. It is best used for applications that require both voltage and current references where low power and low voltage are equally important. The authors achieved this by using subthreshold operation, which is the mode between cutoff, and employing careful transistor sizing.

The bandgap voltage reference was designed and had a temperature range from 40°C to 125°C and an ultra-low noise of 0.4 µm with a load driving capability at 0.8 mA which was made using shared feedback resistors [3]. As a study, the focus of this design was on the load driving ability of reference and the noise performance, which make it suitable for applications requiring constant voltage references even under variable load conditions. The rest of the authors used the technique of sharing feedback resistors for implementing order of this reference, which reduces space and power consumption.

Proposed a voltage source with linear-temperature-qualified superpower consumption [4]. The design focalizes on achieving linear-temperature-dependent power wasting disease, which can be useful in applications where king intake needs to scale with temperature. The authors attain this by utilize a temperature-dependent biasing scheme.

A small temperature-compensated voltage reference made by a group of authors and supported by two transistors was designed [5]. The voltage that is created is as low as 0.5 V. Long-term circuit stability was the only issue that was not met. The design is distinguished by the loss of complexity and the consumption of low power to a very high degree, which is perfectly suitable for the portable and

energy-harvesting industry. The unique operation of the authors was thinking of only three transistors, the rest of the operation was under subthreshold because of the third transistor's behavior.

Zhu et al. research also gave thrust to the making of MOSFET only handheld voltage reference on nano-watt scale without the inclusion of an amplifier, which means that telecommunication networks could do without an amplifier too if it is so designed [6]. It is hype that is 0.00% lines sensitive. Details: The new reference removes the need for amplifiers, thereby decreasing complexity as well as power consumption. It forms well on-line sensitivity, so you have the flexibility to use it at different voltage levels. The signature hand of DNS was MOSFETs in the subthreshold region and the optimization of the transistor sizes.

Created a picowatt, 0.45-0.6 V self-biased subthreshold CMOS voltage reference [7]. The bias current of the system is the one which originates from the reference voltage itself; therefore, it is the one that leads to a decrease in power consumption and the simplification of the circuit. In addition to this, the writers have devised a self-biased structure and a semiconductor size optimization, to reach this aim.

Existing Methods

Their capability to offer temperature compensated reference voltages is the reason for their high popularity. However, the BGRs are still making use of use of the bipolar junction transistors (BJTs) which in turn boost up the power dissipated and set the lowest required voltage channel [1–4].

Generally clamping amplifiers are incorporated into current generators so that they can make the bias current less dependent on the supply voltage. The effectiveness of the bias current in linking the emitter areas, the area of the diode, the value of resistor, and the gain and power of the amplifier. Hence, it can possess excellent low sensitivity performance even if the complexity of chip area and power consumption of the design are increased [10–13].

Self-regulating techniques can improve LS and PSRR when the supply voltage is automatically adjusted in order not to upset the regulators performance [14]. Nevertheless, it is a common cause to elevate the minimum operating voltage and circuit overheard.

Current bias based on the reference voltage is given to the diode, which forms a smaller circuit and, therefore, has lower power consumption. However, their effectives are weakened by DIBL effect that has consequences on LS and PSRR [14]. proposes a forced air (positive air pressure) solution to the problem.

Proposed Methods

Below are some of the existing methods that are improved. The proposed method can be:

A. Adaptive (V_{GS}) control for DIBL effect compensation.

1. The implemented the DIBL effect is a situation that happens when the threshold voltage of the transistors decreases as the voltage increases [13]. This results in the diminishing of Line sensitivity and PSRR.
2. Proposed circuit based on a universal (V_{GS}) control element can effectively shift the gate source voltage (V_{GS}) of the biasing semiconductor (M1) and limit (V_{DD}) affecting (I_B), making the bias current constant almost all the time.
3. The basic principle M8 taps (V_{DD}) for feedback and adjusts output current to compensate for LS variations. In the course of this modification, the DIBL effect is counteracted, and the gate-biasing transistor (M1) becomes stable, thus LS and PSRR are increased [14].

B. CMOS Voltage reference design

The design for the suggested SBCVR had been divided into two parts, the first one is the start circuit and the next one is the main circuit which is shown below Figure 27.2. In these circuit we have the thickness is different for some transistors is in Figure 27.2, whenever is turned on that means when we apply supply voltage to circuit then the transistor of Ms1-Ms4(PMOS) is turned on (in digital design '0' means the PMOS id turned on) to power up the node B. Afterwards the Ms6 is turned on then charge will we passed on to the node A to the GND (V_{SS}). The main circuit will be operated normally. Then the reference voltage is arranged, simultaneously Ms5 will be activated, while Ms6 is power-down to confirm the normal implementation of the SBCVR circuit. Here the M8 is the compensation transistor which automatically detect any variations in the supply voltage, which will

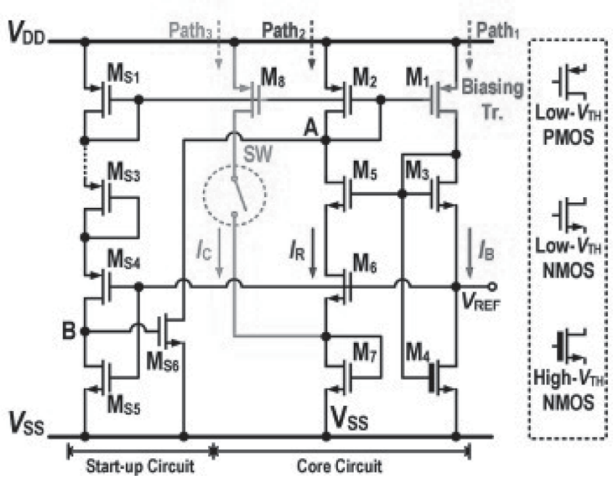

Figure 27.2 Diagram shown here is of the suggested SBCVR with short channel compensation effect
Source: Author

be connected to a Switch. These switches play an important role in which they will be able to activate or deactivate compensation transistor. In the M1-M2 are the current-mirrors methods which generate the bias current. The (V_{REF}) is connected to the M5-M6 which are in cascode [12] connection which will be generated the current (IR), these (IR) current will be passed on to the (I_B). When the SW is turned on, then the compensation transistor M8 will detect the (V_{DD}) variations, then the M6 and M7 will be used to adjust the (I_R). The adaptive (V_{GS}) control of M1 is used for the DIBL effect compensation [14], and this method can reduce the LS [13] and frequency PSRR to a very low value.

Simulation Tool

The Cadence tool is a computer-aided design (CAD) program that is used broadly in electronics (ICs, PCBs, SoCs) to simulate and design them. The Cadence tool enabling designers to create, verify and simulate complex electronic systems has had a significant impact on design times and the overall quality of the design accomplishing the goals.

Simulation process

Do the right click on the desktop and create your own folder. After creating a folder right click on that and select the open in terminal option. Type the command "csh" and then type the "source/home/cad/cshrc", then welcome to the cadence tools window will be appeared. Type the command "virtuoso &" then the virtuoso will be opened. In that click "File→Create→New Library" to create new library, then the library form will be opened then give name to the library, click "ok". Select the technology file the attach to an existing technology library (ex: gpdk045 (or) gpdk180 etc...). To create a schematic window for that in the virtuoso "File→Create→New cell view", then the cell view will be opened, after that name cell view, then onwards the schematic window will be appeared.

In the schematic window we can create→Instance (or) "I" then the add instance will be appeared in the browse the library manager to select the required transistors the click hide in the bottom. Then inputs and outputs will display neither the symbols nor pin. Then do the wiring to the schematic, after that check and save if there is any error go to the virtuoso tab and rectify the errors otherwise circuit will be designed.

Simulation Results

A piece of work on the design and simulation of the SBCVR with the DIBL phenomenon compensation making use of adaptive (V_{GS}) regulation in a 0.18 um CMOS process were presented. The dimensions of the transistor (length and width) are shown in Figure 27.3 below. The occupied area of the SBCVR is 0.0014 mm^2. The average temperature coefficient being 61.85 ppm/°C. The average power consumption at 100°C is 391 pW. The measured (VREF) at 27°C is 106.6 mV is shown at Figure 27.6.

The Figure 27.4. is the way of PSRR determination. It has the value of -41.03 at 10 k. It is indeed the most efficient when comparing it to other works [8].

There is a calculated LS value of 0.013, this is an 87% reduction in comparison to the work [8] that was done previously is shown in Figure 27.5. The measured (VREF) at 27°C is 106.6 mV and it is reduced compared [8] to other work is shown at Figure 27.6. The measured temperature coefficient at 0.6 is 263.4n and at 1.8 is 61.85n. A greater LS (0.013% / V) is reached by the suggested design over the majority of other designs, nevertheless, it uses a mix of both self-regulating and cascode structures [11] to get the high LS and PSRR, respectively. At the same time, this improvement makes it necessary to have at least a level of volt age, which is nearly twice as high as it would be in other designs. The below Table 27.1 shows the comparison outcomes for the suggested SBCVR with DIBL effect Compensation

Tr.	W/L	Tr.	W/L
M_1,M_2	2µm/10µm	M_5,M_6	5µm/10µm
M_3	3×12µm/2µm	M_7	1µm/2µm
M_4	5.4µm/10µm	M_8	0.22µm/1.1µm

Figure 27.3 The dimensions of the transistor
Source: Author

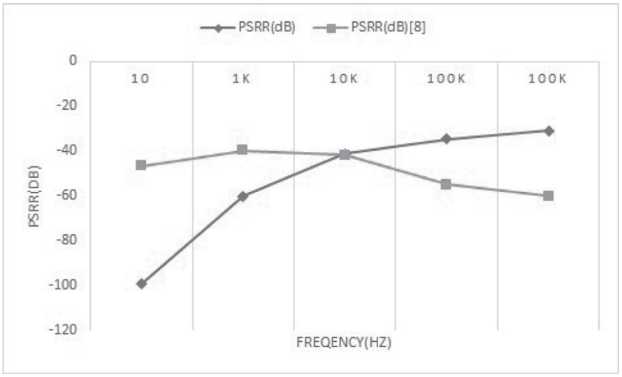

Figure 27.4 Measured PSR
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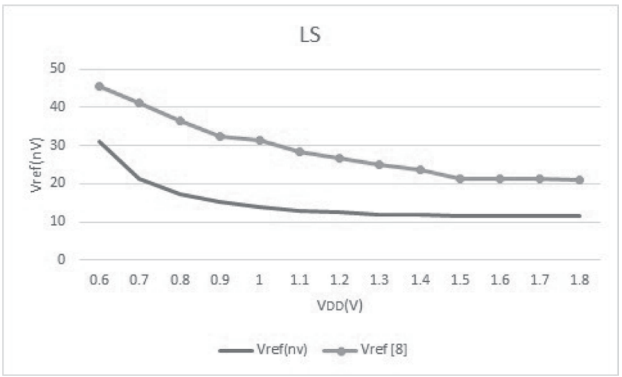

Figure 27.5 Measured LS
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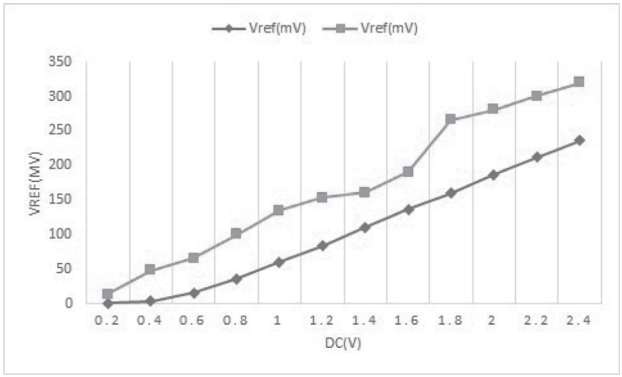

Figure 27.6 Calculated voltage reference
Source: Author

Table 27.1 Comparison of different designs.

Parameter	This Work	TCAS-I'19 [8]
Process (nm)	180	180
Type	CMOS	CMOS
Techniques	DIBL Compensation	Clamping Amplifiers
Power (nW)	0.067 @ 270℃ 3.9 @ 1000℃	22.7
VREF (mV)	106.6	160.
TC (ppm/◦C)	61.85	90.95
LS (%/V)	0.013	0.017
PSRR (dB)	-60.5 @ 1kHz -41.03 @ 10KHz	-46.73
Area (mm^2)	0.0014	0.0148

Source: Author

using adaptive VG control. The other work with the clamping amplifiers between the DIBL compensation. However, the suggested method obtains the low line sensitivity and power consumption.

Conclusion

Finally, the document demonstrates the feasibility of an ultra-low power, self-compensated CMOS voltage reference in the presence of the DIBL effect compensated processor. Through the application of a proposed gate-source voltage regulator, the basic job of biasing the transistor is achieved, which leads to a significant improvement in line sensitivity (LS) and power supply rejection ratio (PSRR) at low frequencies. Experimental data obtained from a 0.18µm

CMOS process indicates that in LS from 0.013%/V (87%) of the standard designs there is a significant decrease. On top of that, this circuit has the lowest power consumption on record of 391 pW and it is also a very small chip area of 0.0014 mm^2. Hence, the obtained outcomes turn it into a highly optimistic alternative to energy-efficient, ultra-low-power Internet of Things applications.

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